SHARP MICROELECTRONICS OF THE AMERICAS

ERRATA

DATE: April 8, 2005 ERRATA REFERENCE NUMBER: SMA03018D

PRODUCT GROUP: SoC

PART NUMBER: LH7A404 System-on-Chip

AFFECTED ITEM(s):		
X	Silicon	LH7A404
X	Document(s)	LH7A404 Data Sheet and User's Guide
	Other	

DESCRIPTION

Summary of Errata

This Errata supersedes all previous errata for this product. For detailed descriptions, please see the following pages.

Key to Status: ✓ = Erratum/documentation fixed in this version of silicon
I = Under Investigation (work around available)
S = Specification Change
o = Erratum (work around available)
● = Erratum (no work around available)

ERRATA NUMBER	BLOCK	SUMMARY	STATUS			
			B0	B1	B1A	B2
404-CHIP-01	Chip	Power up sequence of 1.8 V and 3.3 V power supplies (revised)	S	S	S	S
404-CHIP-02	Chip	Buffer output drive current specification reduced	S	S	S	S
404-CHIP-03	Chip	Pin numbers incorrect in some references within text	✓	✓	✓	✓
404-AC97-01	AC97	Flags RXFE (Receive FIFO Empty) and TXFF (Transmit FIFO Full) function in Compact mode	**o**	**o**	**o**	**o**
404-AC97-02	AC97	Data may be written twice to the Channel 2 FIFO	**I**	**I**	**I**	**I**
404-ADC-01	A/D Converter	Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) do not meet specification	**o**	**o**	**o**	**o**
404-BMI-01	Battery Monitor	Battery Monitor read FIFO empty polling does not work properly for a byte count of 8 or more	**o**	**o**	**o**	**o**
404-BOOT-01	Boot ROM	Boot ROM does not function properly with B.0 silicon	●	✓	✓	✓
404-BOOT-02	Boot ROM	Bit order in the Boot Log at address 0xB0013FFC is incorrect in Table 4-3	✓	✓	✓	✓
404-CSC-01	Clock/State Controller	Only even-numbered divisor values and 1 may be used for PGMCLK	**o**	**o**	**o**	**o**
404-CSC-02	Clock/State Controller	The main processor clock may run faster than programmed	**o**	**o**	S	✓
404-DMA-01	DMA	DMA CONTROL register write operation requires settling time	**o**	**o**	**o**	**o**
404-GPIO-01	GPIO	Port E Data Direction register (PEDD) definition correction	✓	✓	✓	✓
404-LCD-01	LCD Controller	Vertical and horizontal scan mode bits (UBL and LBR) omitted from the User's Guide	✓	✓	✓	✓
404-MMC-01	SD/MMC	MMC Buffer Partially Full register defeatured	**o**	**o**	**o**	**o**
404-MMC-02	SD/MMC	SPI Mode is not supported	S	S	S	S
404-MMC-03	SD/MMC	SD/MMC EMPTY flag lags final read from FIFO	S	S	S	S
404-MMC-04	SD/MMC	Interrupt Mask register documented incorrectly	✓	✓	✓	✓

SHARP MICROELECTRONICS OF THE AMERICAS

ERRATA

DATE: April 8, 2005 ERRATA REFERENCE NUMBER: SMA03018D

PRODUCT GROUP: SoC

PART NUMBER: LH7A404 System-on-Chip

AFFECTED ITEM(s):			
	X	Silicon	LH7A404
	X	Document(s)	LH7A404 Data Sheet and User's Guide
		Other	

DESCRIPTION

ERRATA NUMBER	BLOCK	SUMMARY	STATUS			
			B0	B1	B1A	B2
404-SCI-01	Smart Card	Smart Card Interface (SCI) in Boundary Scan Mode	●	●	●	●
404-SDRC-01	Synchronous Memory	All 32 data bus bits are driven, regardless of the data bus size of the peripheral	S	S	S	S
404-SMC-01	Static Memory	Function of WST1 and WST2 fields is not correctly documented	S	S	S	S
404-TIM-01	Timer3	Timer3 CONTROL3:CLKSEL bit omitted from User's Guide	o	o	o	o
404-USB-01	USB, All	USB operation not guaranteed	o	o	S	✓
404-USBD-01	USB Device	DMA packet sizes of 8, 24, 40, and 56 bytes do not work from USB Client in certain conditions	o	o	o	o
404-USBH-01	USB Host	The USB reports unrecoverable errors when the clock speed exceeds 37.5 MHz (revised)	I	I	I	I
404-VIC-01	VIC	Interrupt vector may be overwritten when two near-simultaneous interrupts occur in VIC2	I	I	I	I
404-VIC-02	VIC	VIC occasionally reports transient vector address	●	●	●	●
404-WDT-01	VIC	WDTSEL bit does not function as documented	S	S	S	S

DATE:	April 8, 2005	ERRATA REFERENCE NUMBER:	SMA03018D
PRODUCT GROUP:	SoC		
PART NUMBER:	LH7A404 System-on-Chip		

AFFECTED ITEM(s):			
	X	Silicon	LH7A404
	X	Document(s)	LH7A404 Data Sheet and User's Guide
		Other	

DESCRIPTION

Chip Function and Operation Errata

General Chip Function

404-CHIP-01 Power up sequence of 1.8 V and 3.3 V power supplies

Description: SHARP recommends that the 1.8 V power supply be energized before the 3.3 V supply. If this is not possible, the 1.8 V supply may not lag the 3.3 V supply by more than 100 μs. If longer delay time is needed, it is recommended that the voltage difference between the two power supplies be within 1.5 V during power supply ramp up.

Work Around: Power-up sequencing must follow above guidelines.

Solution: Change in specification; LH7A404 Data Sheet updated. (note that the wording on this erratum is revised)

404-CHIP-02 Buffer output drive current specification reduced

Description: The drive currents listed in the Data Sheet have been reduced to reflect typical lot characteristics.

Work Around: None; use revised values. The revised drive currents appear in the Addendum of this Errata document.

Solution: The Data Sheet has been updated to reflect the new values.

404-CHIP-03 Pin numbers incorrect in some references within text

Description: Some of the pin numbers listed in text and tables within the User's Guide have PBGA pin numbers rather than the correct CABGA pin numbers. The Functional Pin Listing table in Chapter 1 of the User's Guide, and the Functional Pin Listing and Numerical Pin Listing in the Data Sheet have correct pin numbers.

Work Around: Use only the pin numbers listed in the Data Sheet or Chapter 1 until the User's Guide is updated.

Solution: This erratum has been corrected in the next release of the LH7A404 User's Guide.

AC97

404-AC97-01 Flags RXFE (Receive FIFO Empty) and TXFF (Transmit FIFO Full) function in Compact mode

Description: In Compact mode, data from two slots is compacted into a single 32-bit word. The RXFE is set when the FIFO is empty, and then cleared when *one* or more 16-bit entry exists in the FIFO. In Compact mode, the RXFE should not be cleared until *two* 16-bit entries are made (one compacted word). This applies in the converse to TXFF. The RXFE and TXFF operate normally when not in Compact mode.

Work Around: When polling in Compact mode, use the Receive Interrupt Status bit (RIS) instead of RXFE status, and the Transmit Interrupt Status bit (TIS) instead of TXFF to determine when the FIFO should be read or written.

Solution: Permanent erratum; no fix is planned.

DATE:	April 8, 2005	ERRATA REFERENCE NUMBER:	SMA03018D
PRODUCT GROUP:	SoC		
PART NUMBER:	LH7A404 System-on-Chip		

AFFECTED ITEM(s):			
	X	Silicon	LH7A404
	X	Document(s)	LH7A404 Data Sheet and User's Guide
		Other	

DESCRIPTION

404-AC97-02 Data may be written twice to the Channel 2 FIFO

Description: Occasionally, a second write cycle may be executed to the Channel 2 FIFO, resulting in data being written to the FIFO twice. The erroneous data cannot be detected. This problem only exists in B.0 and B.1 silicon.

Work Around: Do not use Channel 2 in version B.0 or B.1 silicon.

Solution: This erratum is under investigation.

ADC/Touch Screen Controller

404-ADC-01 Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) do not meet specification

Description: The DNL and INL for B.0 and B.1 silicon do not meet the specification. See Table Table 10-16. 1 for results.

Table 10-16. ADC/TSC DNL and INL Specification

SPECIFICATION	SPECIFIED		MEASURED		UNITS
	MIN.	MAX.	MIN.	MAX.	
Differential Non-Linearity	-0.99	2.00	-0.99	4.50	LSB
Integral Non-Linearity	-3.0	+3.0	-4.5	+4.5	LSB

Work Around: Ensure that application designs can tolerate the actual non-linearity. Performance of the TSC is not affected.

Solution: The Data Sheet will be updated to include revised values.

Battery Monitor Interface

404-BMI-01 Battery Monitor read FIFO empty polling does not work properly for a byte count of 8 or more

Description: Polling to determine when the RXFE (Receive FIFO Empty) bit is set, indicating that data is available to be read from the Read FIFO, does not work properly when the byte count is programmed to 8 or more. If the byte count is 8 or more, only the first 7 bytes are read. However, when using the Receive FIFO Empty Interrupt, all valid byte counts (1 to 31) can be used.

Work Around: There are two work arounds. The most efficient is to use the interrupt method since all functions operate properly. If polling is required, do not set the byte count to a value greater than 7.

Solution: Permanent erratum; no fix is planned.

Boot ROM

404-BOOT-01 Boot ROM does not function properly with B.0 silicon

Description: Boot ROM does not work in burst mode. Consequently, the B.0 silicon implementation does not function properly.

Work Around: None; use B.1 or later silicon.

Solution: Will be fixed in B.1 silicon.

DATE:	April 8, 2005	ERRATA REFERENCE NUMBER:	SMA03018D
PRODUCT GROUP:	SoC		
PART NUMBER:	LH7A404 System-on-Chip		

AFFECTED ITEM(s):			
	X	Silicon	LH7A404
	X	Document(s)	LH7A404 Data Sheet and User's Guide
		Other	

DESCRIPTION

404-BOOT-02 Bit order in the Boot Log at address 0xB0013FFC is incorrect in Table 4-3

Description: The contents of the Boot Log at address 0xB0013FFC (Latched MEDCHG, WIDTH0, WIDTH1, PA7) is listed in the incorrect order in Table 4-3 of the LH7A404 User's Guide.

Work Around: Refer to the table excerpt, shown below.

Solution: User's Guide will be updated for the next release.

Table 4-3. Boot Log Memory Map

ADDRESS	CONTENTS
0xB0013FFF	Top of Internal SRAM
0xB0013FFC	Latched state of pins GPIO PA7, MEDCHG, WIDTH1, and WIDTH0, in that order, right justified.

Clock and State Controller

404-CSC-01 Only even-numbered divisor values and 1 may be used for PGMCLK

Description: Only even divisor values and 1 may be programmed into the PWRCNT:PGMCLK field. Odd divisors may cause unpredictable behavior.

Work Around: Use only even divisor values or 1 for this field.

Solution: User's Guide has been updated.

404-CSC-02 The main processor clock may run faster than programmed

Description: High voltages and low temperatures can cause a race condition with the two Phased Lock Loops (PLLs). PLL1 determines the SoC operating frequency, and PLL2 determines the USB Clock frequency. This Erratum is related to #404-USB-01.

While these race conditions can occur at room temperature, such failures are rare. They are more likely to occur at low temperatures and/or high voltages. Either PLL or both can exhibit the problem. When PLL1 is programmed for a nominal 200 MHz by programming the CLKDIV register parameters for: MAINDIV1 = 0xC, MAINDIV2 = 0x1D, PCLKDIV = 0xE, and PS = 1, the error is approximately +7%. This extra speed is not an issue for the LH7A404 nor its onboard peripherals. A possibility does exist that the faster clock, if used to supply the clock to external peripherals, (via SCLK), could affect their performance.

Work Around: Sharp has developed a test to screen parts and verify proper PLL operation down to 0°C and maximum voltage. Screened parts will be available to fill pending orders and sample requests. All screened parts will have the letter 'A' appended to the revision number stamped on the part (i.e. LH7A404N00B1A). These screened parts are guaranteed to operate at programmed speed to 0°C. Any parts without the 'A' suffix are susceptible to running faster than programmed at any operating temperature and the exact frequency cannot be guaranteed.

Solution: The PLL problem is well understood and a fix has been found and thoroughly simulated for both PLL1 and PLL2. This fix will be implemented in revision B.2 of the LH7A404.

DATE:	April 8, 2005	ERRATA REFERENCE NUMBER:	SMA03018D
PRODUCT GROUP:	SoC		
PART NUMBER:	LH7A404 System-on-Chip		

AFFECTED ITEM(s):			
	X	Silicon	LH7A404
	X	Document(s)	LH7A404 Data Sheet and User's Guide
		Other	

DESCRIPTION

DMA Controller

404-DMA-01 DMA CONTROL register write operation requires settling time

Description: Writing the CONTROL register in successive clock cycles can send the state machine to an unknown condition.

Work Around: Software should immediately read the CONTROL register following a write. This eliminates any potential for erroneous states.

Solution: This erratum has been corrected in the next release of the LH7A404 User's Guide.

GPIO Configuration

404-GPIO-01 Port E Data Direction register (PEDD) definition correction

Description: The description in the User's Guide of the Port E Data Direction register (PEDD) is incorrect.

Work Around: Use the tables below instead of the definition in User's Guides dated prior to March 2005. Table numbers refer to the new tables in the User's Guide.

Solution: The User's Guide will be corrected for future releases.

Table 17-14. PEDD Register

BIT	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FIELD	///															
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
TYPE	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIELD	///								PE7DIR	PE6DIR	PE5DIR	PE4DIR	PE3DIR	PE2DIR	PE1DIR	PE0DIR
RESET	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
TYPE	RO	RO	RO	RO	RO	RO	RO	RO	RW	RW	RW	RW	RW	RW	RW	RW
ADDR	0x8000.0E24															

DATE:	April 8, 2005	ERRATA REFERENCE NUMBER:	SMA03018D
PRODUCT GROUP:	SoC		
PART NUMBER:	LH7A404 System-on-Chip		

AFFECTED ITEM(s):		
X	Silicon	LH7A404
X	Document(s)	LH7A404 Data Sheet and User's Guide
	Other	

DESCRIPTION

Table 17-15. PEDD Fields

BITS	NAME	DESCRIPTION
31:8	///	**Reserved** Reading returns 0. Write the reset value.
7	PE7DIR	**PE7DIR** 1 = Output 0 = Input
6	PE6DIR	**PE6DIR** 1 = Output 0 = Input
5	PE5DIR	**PE5DIR** 1 = Output 0 = Input
4	PE4DIR	**PE4DIR** 1 = Output 0 = Input
3	PE3DIR	**PE3DIR** 1 = Output 0 = Input
2	PE2DIR	**PE2DIR** 1 = Output 0 = Input
1	PE1DIR	**PE1DIR** 1 = Output 0 = Input
0	PE0DIR	**PE0DIR** 1 = Output 0 = Input

DATE:	April 8, 2005	ERRATA REFERENCE NUMBER:	SMA03018D
PRODUCT GROUP:	SoC		
PART NUMBER:	LH7A404 System-on-Chip		

AFFECTED ITEM(s):			
	X	Silicon	LH7A404
	X	Document(s)	LH7A404 Data Sheet and User's Guide
		Other	

DESCRIPTION

LCD Controller

404-LCD-01 Vertical and horizontal scan mode bits (UBL and LBR) omitted from the User's Guide

Description: The bits that control the direction of the horizontal and vertical scanning mode when the ALI is enabled are missing from the User's Guide.

Work Around: Use Table 11-39 to configure ALISETUP[3:2]:

Table 11-39. ALISETUP Register Bits

BITS	FIELD	DESCRIPTION
3	UBL	**Upper Before Lower** This bit selects the vertical scan mode. This bit is only functional when the ALI is enabled. 1 = Normal scanning; top to bottom 0 = Reverse scanning
2	LBR	**Left Before Right** This bit selects the horizontal scan mode. This bit is only functional when the ALI is enabled. 1 = Normal scanning; left to right 0 = Reverse scanning

Solution: This erratum has been corrected in the LH7A404 User's Guide.

Secure Digital/MultiMediaCard Controller

404-MMC-01 MMC Buffer Partially Full register defeatured

Description: Programming the BUF_PART_FULL bit in this register to 1 does not cause the MMC Controller to fill the buffer to the 512-byte capacity as documented. Instead, spurious bytes can be written to the MMC.

Work Around: Do not write a 1 to this bit.

Solution: Permanent erratum; no fix is planned.

404-MMC-02 SPI Mode is not supported

Description: The LH7A400 User's Guide and Datasheet describe the SPI Mode of the MMC. The SPI mode is not supported and use of this mode is not recommended.

Work Around: Do not use SPI mode; use the more efficient MMC Native mode.

Solution: This erratum has been corrected in the LH7A404 User's Guide.

DATE:	April 8, 2005	ERRATA REFERENCE NUMBER:	SMA03018D
PRODUCT GROUP:	SoC		
PART NUMBER:	LH7A404 System-on-Chip		

AFFECTED ITEM(s):			
	X	Silicon	LH7A404
	X	Document(s)	LH7A404 Data Sheet and User's Guide
		Other	

DESCRIPTION

404-MMC-03 SD/MMC EMPTY flag lags final read from FIFO

Description: The EMPTY flag in the STATUS register lags the final read from the FIFO by 2 PREDIV clocks and 1 PCLK. If PREDIV is 1, and software reads the last entry in the FIFO, then immediately reads the STATUS register, the FIFO may still report that it is not EMPTY. Larger PREDIV values result in a longer delay from FIFO read to EMPTY flag update.

Work Around: Software must delay at least two PREDIV clocks between reading the last entry in the FIFO and reading the STATUS register.

Solution: This erratum has been corrected in the LH7A404 User's Guide.

404-MMC-04 Interrupt Mask register documented incorrectly

Description: The SD/MMC Interrupt Mask register (INT_MASK) is documented incorrectly in the User's Guide. The correct function is that programming a 1 to a bit *ENABLES* the interrupt, and programming a 0 *MASKS* the interrupt.

Work Around: The correct function table for the INT_MASK register is:

Table 18-30. INT_MASK Fields

BITS	NAME	DESCRIPTION
31:6	///	**Reserved** Reading returns 0. Write the reset value.
5	SDIO_INT	**SD Interrupt Mask** 1 = Interrupt not masked 0 = Interrupt masked
4	BUS_CLOCK_STOPPED	**Bus Clock Stopped Interrupt Mask** Controller has stopped sending out data 1 = Interrupt not masked 0 = Interrupt masked
3	BUF_READY	**Buffer Ready Interrupt Mask** 1 = Interrupt not masked 0 = Interrupt masked
2	END_CMD	**End Command Response Interrupt Mask** 1 = Interrupt not masked 0 = Interrupt masked
1	DONE	**Program Done Interrupt Mask** 1 = Interrupt not masked 0 = Interrupt masked
0	DATA_TRAN	**Data Transfer Done Interrupt Mask** 1 = Interrupt not masked 0 = Interrupt masked

Solution: Table 18-30 has been corrected in the LH7A404 User's Guide.

DATE:	April 8, 2005	ERRATA REFERENCE NUMBER:	SMA03018D
PRODUCT GROUP:	SoC		
PART NUMBER:	LH7A404 System-on-Chip		

AFFECTED ITEM(s):			
	X	Silicon	LH7A404
	X	Document(s)	LH7A404 Data Sheet and User's Guide
		Other	

DESCRIPTION

SDRAM Controller

404-SDRC-01 All 32 data bus bits are driven, regardless of the data bus size of the peripheral

Description: The SDRAM Controller has one enable line, which enables all 32 bits of the data bus. If the SDRAM Controller is addressing 8-bit (or 16-bit) peripherals, the other bits on the data bus will be driven with the last data to appear on those bits.

Work Around: The application design must take into account that the unused data pins will be driven with the last valid data presented to those pins. If not, additional current can be drawn due to the state of those pins.

Solution: This erratum has been corrected in the LH7A404 User's Guide.

Smart Card Interface

404-SCI-01 Smart Card Interface (SCI) in Boundary Scan Mode

Description: The SCI I/O pad is always tristated in JTAG mode. Therefore, the SCI pin is not tested in JTAG boundary SCAN mode and cannot be used for connectivity testing on a board. In Normal mode, the SCI pin operates properly.

Work Around: None.

Solution: Permanent erratum; no fix is planned.

Static Memory Controller

404-SMC-01 Function of WST1 and WST2 fields is not correctly documented

Description: Current documentation describes WST1 as setting the SRAM Read and Write wait state value, ROM read access time, and the first access for burst ROM accesses. The WST2 field is described as setting the burst access time for burst ROM. These descriptions are not correct. The actual function is that WST1 is used for both read and write wait state insertion, and results in identical numbers of wait states for both operations. In addition, WST2 behaves differently than described.

With Page Mode enabled, burst reads timing behaves as follows:

A. The first transfer cycle duration is WST1 + 1 clocks
B. The second and third transfer cycle durations are WST2 + 1 clocks
C. The fourth transfer cycle is WST2 + 2 clocks
D. For 16-bit accesses only:
   a. The fifth transfer is repeat of the address in the third transfer but for a duration of WST1 + 1 clocks
   b. The sixth transfer is a repeat of the fourth transfer
   c. The seventh transfer is the one that should have occurred as the fifth, is the first of a new burst and timed at WST1 + 1 clocks.
E. For 32-bit accesses only, the fourth transfer is timed at WST2 + 5 clocks
F. For 8-bit accesses only, the third access is timed at WST2 + 2 clocks

Note: For D.a. and D.b., the duplicate data is discarded. The requested data is presented correctly, but the additional overhead cycles may cause lower than expected throughput in Page Mode.

With Page Mode disabled, program WST2 to 0x0.

Work Around: Use the above description when writing software for the SMC.

Solution: The has been corrected in the LH7A404 User's Guide.

DATE:	April 8, 2005	ERRATA REFERENCE NUMBER:	SMA03018D
PRODUCT GROUP:	SoC		
PART NUMBER:	LH7A404 System-on-Chip		

AFFECTED ITEM(s):			
	X	Silicon	LH7A404
	X	Document(s)	LH7A404 Data Sheet and User's Guide
		Other	

DESCRIPTION

Timer3

404-TIM-01 Timer3 CONTROL3:CLKSEL bit omitted from User's Guide

Description: There are two selectable clock sources for Timer3: an internal 3.6864 MHz clock, and an external clock that is input through the CTCLKIN pin. The selection of the clock source is made through the CONTROL3 register, bit 3 (CLKSEL). This bit was omitted from the User's Guide description of CONTROL3.

Work Around: This is the correct description of CONTROL3, bit 3:

BIT	NAME	DESCRIPTION
3	CLKSEL	**Clock Source Select** This bit allows selection of the internal nominal 3.6864 MHz clock as the time base for Timer3, or a clock from an external source input on the CTCLKIN pin. 1 = Use external clock on the CTCLKIN pin 0 = Use internal clock

Solution: This erratum has been corrected in the LH7A404 User's Guide.

USB Host and Device

404-USB-01 USB operation not guaranteed

Description: High voltages and low temperatures can cause a race condition with the two Phased Lock Loops (PLL). PLL1 determines the operating frequency of the SoC, and PLL2 determines the USB Clock frequency. This Erratum is related to erratum #404-CSC-02.

While these race conditions can occur at room temperature, such failures are rare. They are more likely to occur at lower temperatures and/or higher voltages. Either PLL or both can exhibit the problem. When PLL2 locks at a higher frequency, it locks at 13.5 MHz rather than 12 MHz and this is outside the tolerance for USB.

Work Around: Sharp has developed a test to screen parts and verify proper PLL operation down to 0°C and maximum voltage. Screened parts will be available to fill pending orders and sample requests. All screened parts will have the letter 'A' appended to the revision number stamped on the part (i.e. LH7A404N00B1A). These screened parts are guaranteed to operate at programmed speed to 0°C. Any parts without the 'A' suffix are susceptible to running faster than programmed at any operating temperature and USB operation cannot be guaranteed on these parts.

Solution: The PLL problem is well understood and a fix has been found and thoroughly simulated for both PLL1 and PLL2. This fix will be implemented in revision B.2 of the LH7A404.

DATE:	April 8, 2005	ERRATA REFERENCE NUMBER:	SMA03018D
PRODUCT GROUP:	SoC		
PART NUMBER:	LH7A404 System-on-Chip		

AFFECTED ITEM(s):			
	X	Silicon	LH7A404
	X	Document(s)	LH7A404 Data Sheet and User's Guide
		Other	

DESCRIPTION

USB Device

404-USBD-01 DMA packet sizes of 8, 24, 40, and 56 bytes do not work from USB Client in certain conditions

Description: Packets may be dropped when the following environment exists:

- MAXP register for Bulk IN endpoint set to 8, 24, 40, or 56 bytes
- Endpoint configured for DMA transfers
- Very large transmit buffer (e.g. packet size > 1,200 bytes for MAXP = 56 bytes) assigned to DMA channel

Work Around: Configure MAXP for 16, 32, 48, or 64 bytes if the USB Client must transfer packets larger than 1,000 bytes. If MAXP is configured to 8, 24, 40, or 56 bytes, restrict the USB Client to packets smaller than 1,000 bytes.

Solution: Permanent erratum; no fix is planned.

USB Host

404-USBH-01 The USB reports unrecoverable errors when the clock speed exceeds 37.5 MHz (revised)

Description: USB host reports unrecoverable errors during isochronous transfers and multiple control transfers (by plugging multiple devices simultaneously). These errors only occur when the AHB bus clock speed exceeds 37.5 MHz.

Work Around: If the AHB bus clock exceeds 37.5 MHz, valid data can be guaranteed by reading the register two consecutive times, with the second read being valid.

Solution: This erratum is under investigation.

Vectored Interrupt Controller

404-VIC-01 Interrupt vector may be overwritten when two near-simultaneous interrupts occur in VIC2

Description: If a VIC2 interrupt occurs followed by a vectored VIC1 interrupt, there is a two-HCLK window when the address read will be the VIC1 default handler address, not the VIC2 or vectored VIC1 address.

Work Around: In the VIC1 default interrupt handler routine, check whether there are any non-vectored VIC1 interrupts pending. If none, return immediately. Upon return, an interrupt will immediately occur, but this time with the correct vector address.

Solution: Permanent erratum; no fix is planned.

404-VIC-02 VIC occasionally reports transient vector address

Description: Occasionally, the VECTADDR1 register reports an out of range value. This only occurs for MMC interrupts.

Work Around: No work around currently exists.

Solution: This erratum is under investigation.

DATE:	April 8, 2005	ERRATA REFERENCE NUMBER:	SMA03018D
PRODUCT GROUP:	SoC		
PART NUMBER:	LH7A404 System-on-Chip		

AFFECTED ITEM(s):			
	X	Silicon	LH7A404
	X	Document(s)	LH7A404 Data Sheet and User's Guide
		Other	

DESCRIPTION

Watchdog Timer

404-WDT-01 WDTSEL bit does not function as documented

Description: The WDTSEL bit in the PWRCNT register was designed to allow software to select between a Reset0 (Power-on reset) and a Reset1 (System reset) upon expiration of the WDT. Programming this bit to 0 does result in a Reset0 being executed if the WDT times out. However, Programming the bit to 1 does not result in a Reset1 when the WDT times out.

Work Around: Always program this bit to 0.

Solution: This bit should always be programmed to 0. The User's Guide has been corrected.

Table 7-8. PWRCNT Fields

BITS	FIELD	DESCRIPTION
0	WDTSEL	**Watchdog Timer Reset Select** This bit must always be programmed to 0. 1 = Invalid 0 = WDT generates a Power-on reset (Reset0).

DATE: April 8, 2005 ERRATA REFERENCE NUMBER: SMA03018D

PRODUCT GROUP: SoC

PART NUMBER: LH7A404 System-on-Chip

AFFECTED ITEM(s):			
	X	Silicon	LH7A404
	X	Document(s)	LH7A404 Data Sheet and User's Guide
		Other	

DESCRIPTION

ADDENDUM: Buffer Output Drive Current

The following table provides the corrected drive current available on each of the output pins of the LH7A404. These values replace the values in Data Sheets dated prior to July 2004.

CABGA	SIGNAL	DESCRIPTION	OUTPUT DRIVE
P17	A0	Asynchronous Address Bus	12 mA
N16	A1	Asynchronous Address Bus	12 mA
N17	A2/SA0	Asynchronous Address Bus and Synchronous Address Bus	12 mA
M19	A3/SA1		
M20	A4/SA2		
L20	A5/SA3		
M17	A6/SA4		
K18	A7/SA5		
K20	A8/SA6		
K19	A9/SA7		
J20	A10/SA8		
H20	A11/SA9		
J17	A12/SA10		
H18	A13/SA11		
F20	A14/SA12		
G18	A15/SA13		
H16	A16/SB0	• Asynchronous Address Bus • Synchronous Device Bank Address 0	12 mA
F18	A17/SB1	• Asynchronous Address Bus • Synchronous Device Bank Address 1	12 mA
G17	A18	Asynchronous Address Bus	12 mA
F17	A19	Asynchronous Address Bus	12 mA
D19	A20	Asynchronous Address Bus	12 mA
E17	A21	Asynchronous Address Bus	12 mA
C19	A22	Asynchronous Address Bus	12 mA
D17	A23	Asynchronous Address Bus	12 mA
B19	A24	Asynchronous Address Bus	12 mA
A16	A25	Asynchronous Address Bus	12 mA
D15	A26	Asynchronous Address Bus	12 mA
B14	A27	Asynchronous Address Bus	12 mA

DATE: April 8, 2005 ERRATA REFERENCE NUMBER: SMA03018D

PRODUCT GROUP: SoC

PART NUMBER: LH7A404 System-on-Chip

AFFECTED ITEM(s):			
	X	Silicon	LH7A404
	X	Document(s)	LH7A404 Data Sheet and User's Guide
		Other	

DESCRIPTION

CABGA	SIGNAL	DESCRIPTION	OUTPUT DRIVE
N19	D0	Data Bus	12 mA
P20	D1		
N18	D2		
N20	D3		
M16	D4		
M18	D5		
L18	D6		
L17	D7		
L19	D8		
J19	D9		
K17	D10		
J18	D11		
H19	D12		
G20	D13		
G19	D14		
H17	D15		
F19	D16		
E20	D17		
E19	D18		
D20	D19		
E18	D20		
C20	D21		
D18	D22		
B20	D23		
C18	D24		
A20	D25		
B18	D26		
C16	D27		
B17	D28		
A18	D29		
A17	D30		
B15	D31		
C7	ACBITCLK	• Audio Codec (AC97) Clock • Audio Codec (ACI) Clock	8 mA

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PRODUCT GROUP: SoC

PART NUMBER: LH7A404 System-on-Chip

AFFECTED ITEM(s):			
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	X	Document(s)	LH7A404 Data Sheet and User's Guide
		Other	

DESCRIPTION

CABGA	SIGNAL	DESCRIPTION	OUTPUT DRIVE
B6	ACIN	• Audio Codec (AC97) Input • Audio Codec (ACI) Input	8 mA
B7	ACOUT	• Audio Codec (AC97) Output • Audio Codec (ACI) Output	8 mA
A6	ACSYNC	• Audio Codec (AC97) Synchronization • Audio Codec (ACI) Synchronization	8 mA
U12	BATCNTL	Battery Control for A/D controller battery monitor.	12 mA
T16	CLKEN	External Oscillator Enable Output	8 mA
J2	COL0	Keyboard Interface	8 mA
H4	COL1		
H5	COL2		
J1	COL3		
J3	COL4		
J4	COL5		
J5	COL6		
K2	COL7		
D5	DACK0	DMA Acknowledge 0	12 mA
A2	DACK1	DMA Acknowledge 1	12 mA
C4	DEOT0	DMA End of Transfer 0	12 mA
E5	DEOT1	DMA End of Transfer 1	12 mA
D13	DQM0	Data Mask for Synchronous Memories	12 mA
E13	DQM1		
B12	DQM2		
A12	DQM3		
H3	KMICLK	Keyboard/Mouse Clock	12 mA
H1	KMIDAT	Keyboard/Mouse Data	12 mA
U3	LCDCLS	ALI Clock for Row Drivers	12 mA
Y10	LCDDCLK	LCD Pixel Clock	12 mA
V9	LCDENAB/LCDM	• LCD TFT Data Enable • LCD STN AC Bias	12 mA
T4	LCDFP/LCDSPS	• LCD Frame Pulse • ALI Reset Row Driver Counter	12 mA
V4	LCDLBR	ALI Output for reverse scanning	12 mA
V2	LCDLP/LCDHRLP	• LCD Line Pulse • ALI Latch Pulse	12 mA

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PRODUCT GROUP: SoC

PART NUMBER: LH7A404 System-on-Chip

AFFECTED ITEM(s):		
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X	Document(s)	LH7A404 Data Sheet and User's Guide
	Other	

DESCRIPTION

CABGA	SIGNAL	DESCRIPTION	OUTPUT DRIVE
W2	LCDMOD	ALI MOD Signal used by the row driver	12 mA
V5	LCDPS	ALI Power Save	12 mA
W3	LCDREV	ALI Reverse	12 mA
V3	LCDSPL	ALI Start Pulse Left for reverse scanning	12 mA
W1	LCDSPR	ALI Start Pulse Right for normal scanning	12 mA
U4	LCDUBL	ALI Up, Down signal for reverse scanning	12 mA
Y1	LCDVDDEN	ALI Power Sequence Control	12 mA
V8	LCDVD0	LCD Video Data Interface	12 mA
T8	LCDVD1		
W9	LCDVD2		
Y8	LCDVD3		
A5	MMCCLK	MultiMediaCard Clock (20 MHz MAX.)	8 mA
D7	MMCCMD	MultiMediaCard Command	8 mA
C6	MMCDATA0	MultiMediaCard Data 0	8 mA
B5	MMCDATA1	MultiMediaCard Data 1	8 mA
A4	MMCDATA2	MultiMediaCard Data 2	8 mA
B4	MMCDATA3	MultiMediaCard Data 3	8 mA
A13	nBLE0	Byte Lane Enable 0	12 mA
U9	nBLE1	Byte Lane Enable 1	12 mA
Y7	nBLE2	Byte Lane Enable 2	12 mA
C13	nBLE3	Byte Lane Enable 3	8 mA
C15	nCAS	Synchronous Memory Column Address Strobe	12 mA
V18	nCS0	Asynchronous Memory Chip Select 0	12 mA
R19	nCS1	Asynchronous Memory Chip Select 1	12 mA
R18	nCS2	Asynchronous Memory Chip Select 2	12 mA
P19	nCS3	Asynchronous Memory Chip Select 3	12 mA
R20	nCS6	Asynchronous Memory Chip Select 6	12 mA
R17	nCS7	Asynchronous Memory Chip Select 7	12 mA
C12	nOE	Asynchronous Memory Output Enable	12 mA
D11	nPWME0	DC-DC Converter 0 PWM 0 Enable	8 mA
A10	nPWME1	DC-DC Converter 1 PWM 1 Enable	8 mA
A15	nRAS	Synchronous Memory Row Address Strobe	12 mA
C5	nRESETOUT	Reset Output to external devices. This pin carries the same state as the internal SoC reset signal.	12 mA

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PRODUCT GROUP: SoC

PART NUMBER: LH7A404 System-on-Chip

AFFECTED ITEM(s):		
X	Silicon	LH7A404
X	Document(s)	LH7A404 Data Sheet and User's Guide
	Other	

DESCRIPTION

CABGA	SIGNAL	DESCRIPTION	OUTPUT DRIVE
B11	nSCRESET	Smart Card Interface Reset	12 mA
C17	nSCS0	Synchronous Memory Chip Select 0	12 mA
A19	nSCS1	Synchronous Memory Chip Select 1	12 mA
D16	nSCS2	Synchronous Memory Chip Select 2	12 mA
E16	nSCS3	Synchronous Memory Chip Select 3	12 mA
B16	nSWE	Synchronous Memory Write Enable	12 mA
D12	nWE	Asynchronous Memory Write Enable	12 mA
M2	PA0/LCDVD16	• GPIO Port A0 • LCD Data pin 16	8 mA
L4	PA1/LCDVD17	• GPIO Port A1 • LCD Data pin 17	8 mA
M3	PA2	GPIO Port A[6:2]	8 mA
M4	PA3	GPIO Port A	8 mA
M1	PA4	GPIO Port A	8 mA
N3	PA5	GPIO Port A	8 mA
N2	PA6	GPIO Port A	8 mA
N1	PA7	• GPIO Port A7 • Boot Width Selection	8 mA
N4	PB0/UARTRX1	• GPIO Port B0 • UART1 Receive Data Input	8 mA
P3	PB1/UARTTX3	• GPIO Port B1 • UART3 Transmit Data Out	8 mA
P2	PB2/UARTRX3	• GPIO Port B2 • UART3 Receive Data In	8 mA
P1	PB3/UARTCTS3	• GPIO Port B3 • UART3 Clear to Send	8 mA
R3	PB4/UARTDCD3	• GPIO Port B4 • UART3 Data Carrier Detect	8 mA
N5	PB5/UARTDSR3	• GPIO Port B5 • UART3 Data Set Ready	8 mA
R2	PB6/SWID/SMBD	• GPIO Port B6 • Single Wire Data • Smart Battery Data	8 mA
R1	PB7/ SMBCLK	• GPIO Port B7 • Smart Battery Clock	8 mA
P4	PC0/ UARTTX1	• GPIO Port C0 • UART1 Transmit Data Output	12 mA

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PRODUCT GROUP: SoC

PART NUMBER: LH7A404 System-on-Chip

AFFECTED ITEM(s):		
X	Silicon	LH7A404
X	Document(s)	LH7A404 Data Sheet and User's Guide
	Other	

DESCRIPTION

CABGA	SIGNAL	DESCRIPTION	OUTPUT DRIVE
T1	PC1	GPIO Port C1	12 mA
T2	PC2	GPIO Port C2	12 mA
T3	PC3	GPIO Port C3	12 mA
R4	PC4	GPIO Port C4	12 mA
U1	PC5	GPIO Port C5	12 mA
U2	PC6	GPIO Port C6	12 mA
V1	PC7	GPIO Port C7	12 mA
Y11	PD0/LCDVD8	• GPIO Port D[7:0] • LCD Video Data Interface	12 mA
U10	PD1/LCDVD9		
W12	PD2/LCDVD10		
V11	PD3/LCDVD11		
W11	PD4/LCDVD12		
U11	PD5/LCDVD13		
V12	PD6/LCDVD14		
Y12	PD7/LCDVD15		
Y9	PE0/LCDVD4	• GPIO Port E[3:0] • LCD Video Data Interface	12 mA
W10	PE1/LCDVD5		
V10	PE2/LCDVD6		
T9	PE3/LCDVD7		
D4	PE4/ SCCLKIN	• GPIO Port E4 • Smart Card Push-Pull Mode Clock Input	12 mA
C3	PE5/SCCLKEN	• GPIO Port E5 • Smart Card Push-Pull Mode External Clock Buffer Enable	12 mA
B2	PE6/SCIN	• GPIO Port E6 • Smart Card Push-Pull Mode Data Input	12 mA
A1	PE7/SCDATEN	• GPIO Port E7 • Smart Card Push-Pull Mode Data Out External Buffer Enable	12 mA
A9	PF0/INT0	• GPIO Port F0 • Interrupt 0	8 mA
D9	PF1/INT1	• GPIO Port F1 • Interrupt 1	8 mA
A8	PF2/INT2	• GPIO Port F2 • Interrupt 2	8 mA
C8	PF3/INT3	• GPIO Port F3 • Interrupt 3	8 mA

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PRODUCT GROUP: SoC

PART NUMBER: LH7A404 System-on-Chip

AFFECTED ITEM(s):			
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	X	Document(s)	LH7A404 Data Sheet and User's Guide
		Other	

DESCRIPTION

CABGA	SIGNAL	DESCRIPTION	OUTPUT DRIVE
B8	PF4/INT4	• GPIO Port F4 • Interrupt 4	8 mA
D8	PF5/INT5/SCDETECT	• GPIO Port F5 • Interrupt 5 • Smart Card Interface Card Detect Signal	8 mA
A7	PF6/INT6/PCRDY1	• GPIO Port F6 • Interrupt 6 • Ready for Card 1 for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	8 mA
E8	PF7/INT7/PCRDY2	• GPIO Port F7 • Interrupt 7 • Ready for Card 2 for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	8 mA
Y2	PG0/nPCOE	• GPIO Port G0 • Output Enable for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	8 mA
W4	PG1/nPCWE	• GPIO Port G1 • Write Enable for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	8 mA
Y3	PG2/nPCIOR	• GPIO Port G2 • I/O Read Strobe for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	8 mA
U5	PG3/nPCIOW	• GPIO Port G3 • I/O Write Strobe for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	8 mA
T5	PG4/nPCREG	• GPIO Port G4 • Register Memory Access for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	8 mA
W5	PG5/nPCCE1	• GPIO Port G5 • Card Enable 1 for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode. This signal and nPCCE2 are used by the PC Card for decoding low and high byte accesses.	8 mA
Y4	PG6/nPCCE2	• GPIO Port G6 • Card Enable 2 for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode. This signal and nPCCE1 are used by the PC Card for decoding low and high byte accesses.	8 mA
W6	PG7/PCDIR	• GPIO Port G7 • Direction for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	8 mA
V6	PH0/PCRESET1	• GPIO Port H0 • Reset Card 1 for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	8 mA
Y5	PH1/CFA8/PCRESET2	• GPIO Port H1 • Address Bit 8 for PC Card (CompactFlash) in Single Card mode • Reset Card 2 for PC Card (PCMCIA or CompactFlash) in Dual Card mode	8 mA
W7	PH2/nPCSLOTE1	• GPIO Port H2 • Enable Card 1 for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode. This signal is used for gating other control signals to the appropriate PC Card.	8 mA

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PRODUCT GROUP: SoC

PART NUMBER: LH7A404 System-on-Chip

AFFECTED ITEM(s):			
	X	Silicon	LH7A404
	X	Document(s)	LH7A404 Data Sheet and User's Guide
		Other	

DESCRIPTION

CABGA	SIGNAL	DESCRIPTION	OUTPUT DRIVE
U6	PH3/CFA9/PCMCIAA25/ nPCSLOTE2	• GPIO Port H3 • Address Bit 9 for PC Card (CompactFlash) in Single Card mode • Address Bit 25 for PC Card (PCMCIA) in Single Card mode • Enable Card 2 for PC Card (PCMCIA or CompactFlash) in Dual Card mode. Used for gating other control signals to the appropriate PC Card.	8 mA
W8	PH4/nPCWAIT1	• GPIO Port H4 • WAIT Signal for Card 1 for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	8 mA
Y6	PH5/CFA10/PCMCIAA24/ nPCWAIT2	• GPIO Port H5 • Address Bit 10 for PC Card (CompactFlash) in Single Card mode • Address Bit 24 for PC Card (PCMCIA) in Single Card mode • WAIT Signal for Card 2 for PC Card (PCMCIA or CompactFlash) in Dual Card mode	8 mA
V7	PH6/ nAC97RESET	• GPIO Port H6 • AC97 Reset	8 mA
U7	PH7/nPCSTATRE	• GPIO Port H7 • Status Read Enable for PC Card (PCMCIA or CompactFlash) in Single or Dual Card mode	8 mA
L2	PGMCLK	Programmable Clock (14.7456 MHz MAX.)	8 mA
C11	PWM0	DC-DC Converter 0 Output (Pulse Width Modulated)	8 mA
C10	PWM1	DC-DC Converter 1 Output (Pulse Width Modulated)	8 mA
B9	PWM2	PWM Output 2	8 mA
C9	PWMSYNC	PWM Synchronizing Input for PWM2	8 mA
A11	SCCLK	Smart Card Interface Clock	12 mA
E12	SCIO	Smart Card Interface I/O	12 mA
A14	SCKE0	Clock Enable 0 for Synchronous Memory	12 mA
B13	SCKE1_2	Clock Enable 1 OR 2 for Synchronous Memory	12 mA
C14	SCKE3	Clock Enable 3 for Synchronous Memory	12 mA
D14	SCLK	Synchronous Memory Clock	20 mA sink 12 mA source
B10	SCVCCEN	Smart Card Interface VCC Enable	12 mA
K3	SSPCLK	Synchronous Serial Port Clock	8 mA
K4	SSPFRM	Synchronous Serial Port Frame Sync	8 mA
L1	SSPRX	Synchronous Serial Port Receive	8 mA
L3	SSPTX	Synchronous Serial Port Transmit	8 mA
K1	TBUZ	Timer Buzzer Output (254 kHz MAX.)	8 mA
B1	TDO	JTAG Data Out	4 mA
F2	UARTCTS2	UART2 Clear to Send Signal	8 mA

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PRODUCT GROUP: SoC

PART NUMBER: LH7A404 System-on-Chip

AFFECTED ITEM(s):			
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	X	Document(s)	LH7A404 Data Sheet and User's Guide
		Other	

DESCRIPTION

CABGA	SIGNAL	DESCRIPTION	OUTPUT DRIVE
F1	UARTDCD2	UART2 Data Carrier Detect Signal	8 mA
G2	UARTDSR2	UART2 Data Set Ready Signal	8 mA
G1	UARTIRRX1	IrDA Receive	8 mA
G3	UARTIRTX1	IrDA Transmit	8 mA
G4	UARTRX2	UART2 Receive Data Input	8 mA
H2	UARTTX2	UART2 Transmit Data Output	8 mA
U17	USBDCP	USB Device Full Speed Pull-up Resistor Control	12 mA
U19	USBDN	USB Device Data Negative (Differential Pair)	12 mA
U20	USBDP	USB Device Data Positive (Differential Pair)	12 mA
W20	USBHDN0	USB Data Host Negative 0 (Differential Pair)	12 mA
V20	USBHDN1	USB Data Host Negative 1 (Differential Pair)	12 mA
W19	USBHDP0	USB Data Host Positive 0 (Differential Pair)	12 mA
V19	USBHDP1	USB Data Host Positive 1 (Differential Pair)	12 mA
V17	USBHOVRCURR	USB Host Overcurrent	12 mA
T17	USBHPWR	USB Host Power	12 mA