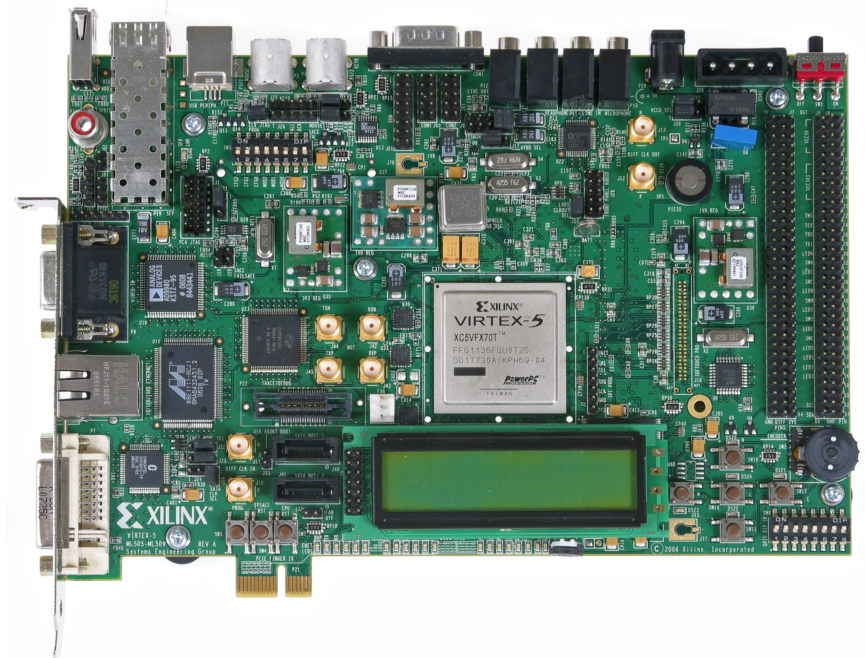




# ML507 QuickStart

October 2008

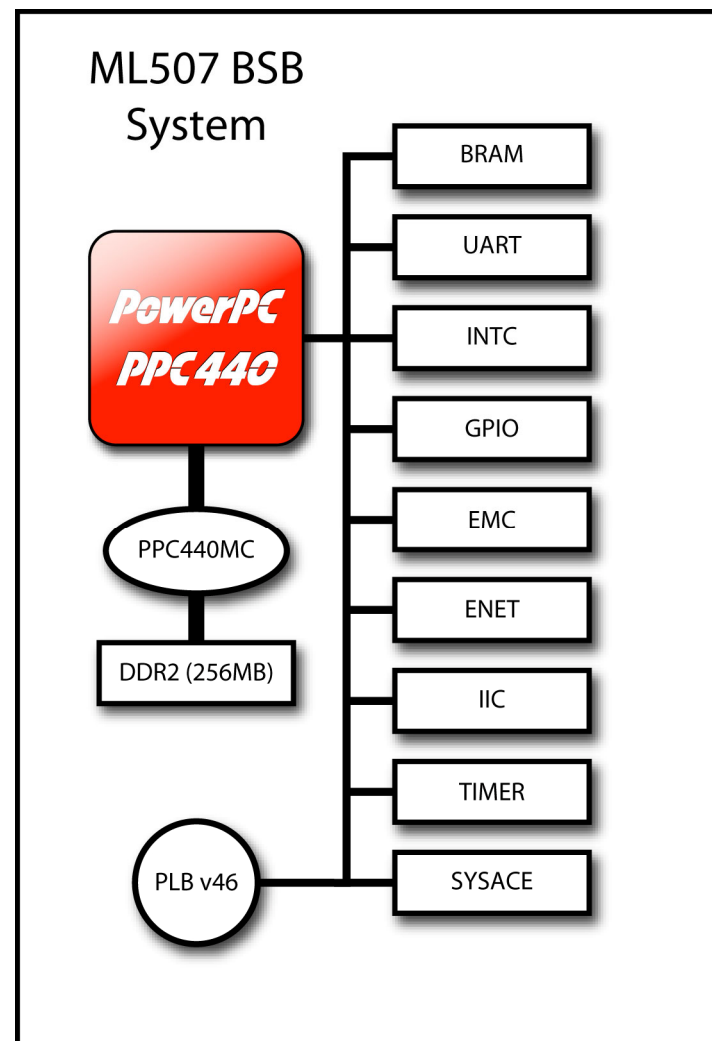


# Overview

- Setup
- Boot with ACE-loader ACE File
- Observe LCD and Terminal messages
- Load new Configuration
- Re-load ACE-loader

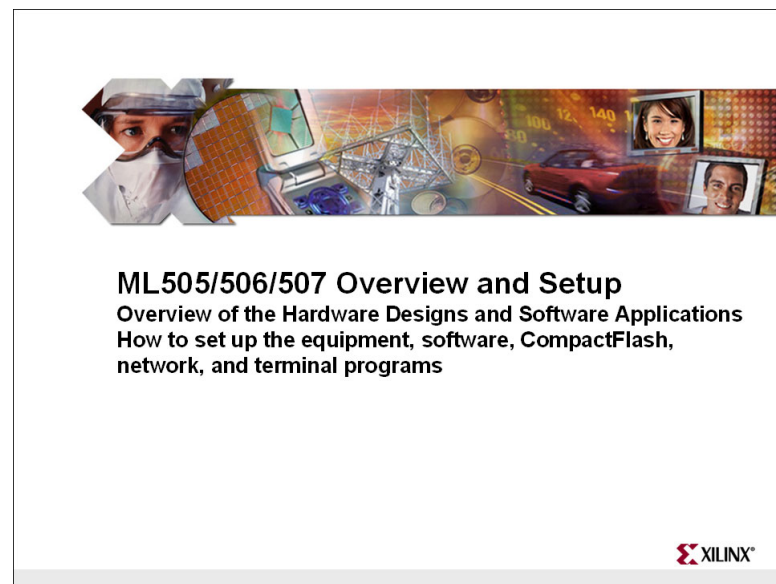
# ML507 BSB Hardware

- The ML507 PPC440 design hardware includes:
  - PPC440MC DDR2 Interface
  - External Memory Controller (EMC)
    - ZBT SRAM
  - BRAM
  - Networking
  - UART
  - Interrupt Controller
  - System ACE CF Interface
  - GPIO (IIC, LEDs and LCD)
  - PLB Arbiter



# Additional Setup Details

- Refer to ml505\_overview\_setup document for details on:
  - Software Requirements
  - ML507 Board Setup
    - **Equipment and Cables**
    - **Software**
    - **Network**
  - Terminal Programs
    - **This presentation requires the 9600-8-N-1 Baud terminal setup**



# Hardware Setup

- Connect the Xilinx Platform Cable USB to the ML507 board
- Connect the RS232 null modem cable to the ML507 board



# Hardware Setup

- The ML507 uses a DVI video interface
- Connect a DVI monitor  
*or*
- Use a DVI/VGA adapter to connect a VGA monitor
  - <http://www.belkin.com>



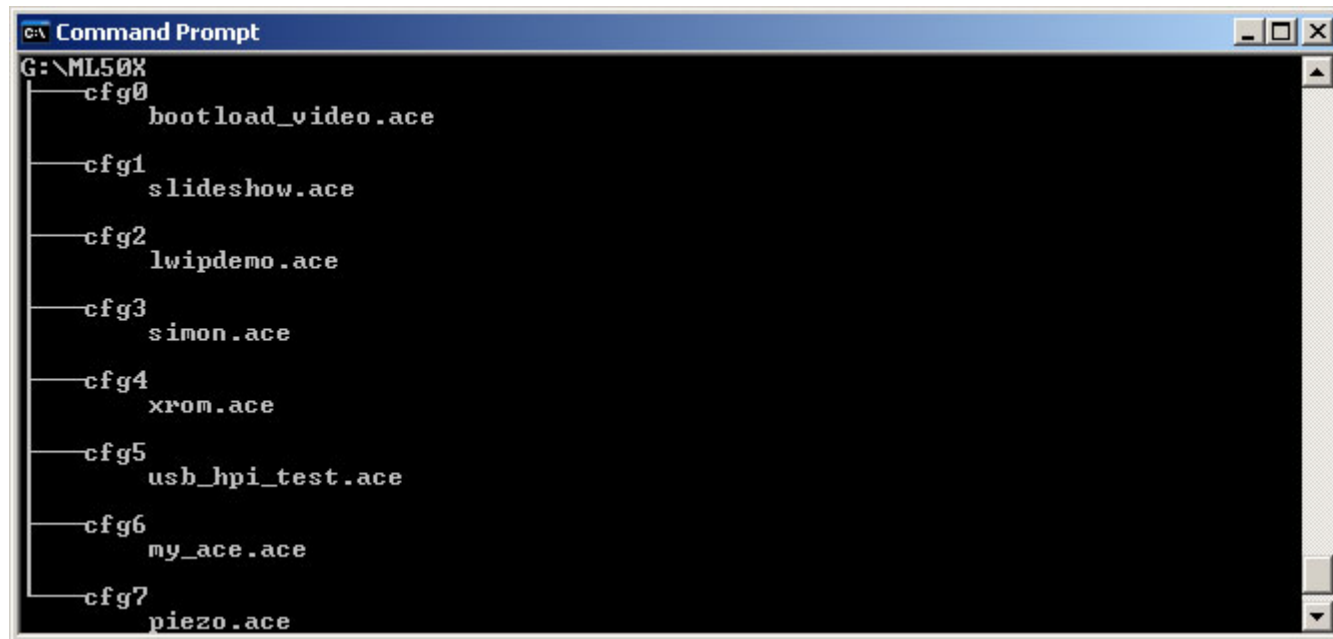
# Hardware Setup

- USB Keyboard
  - [www.dell.com](http://www.dell.com)



# Factory CompactFlash

- The CompactFlash shipped with the ML507 board has the following ace files preloaded:



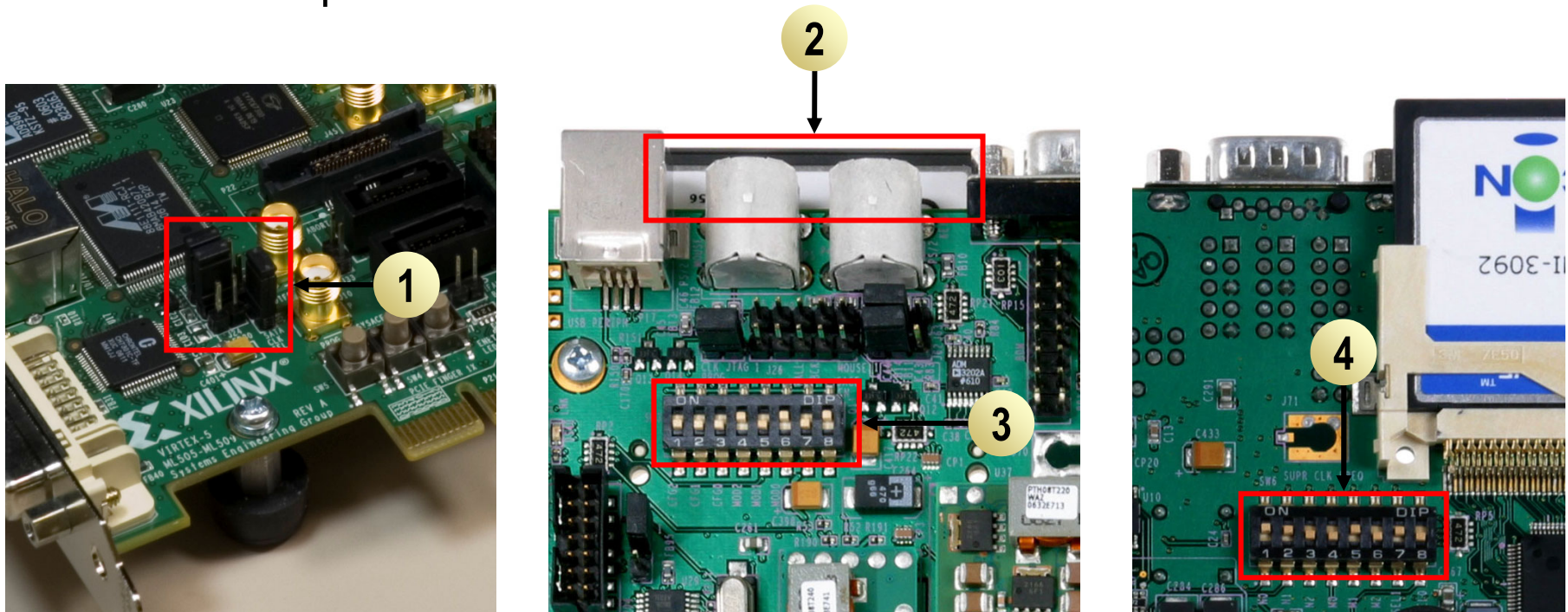
```
G:\ML50X
├── cfg0
│   └── bootload_video.ace
├── cfg1
│   └── slideshow.ace
├── cfg2
│   └── lwipdemo.ace
├── cfg3
│   └── simon.ace
├── cfg4
│   └── xrom.ace
├── cfg5
│   └── usb_hpi_test.ace
├── cfg6
│   └── my_ace.ace
└── cfg7
    └── piezo.ace
```





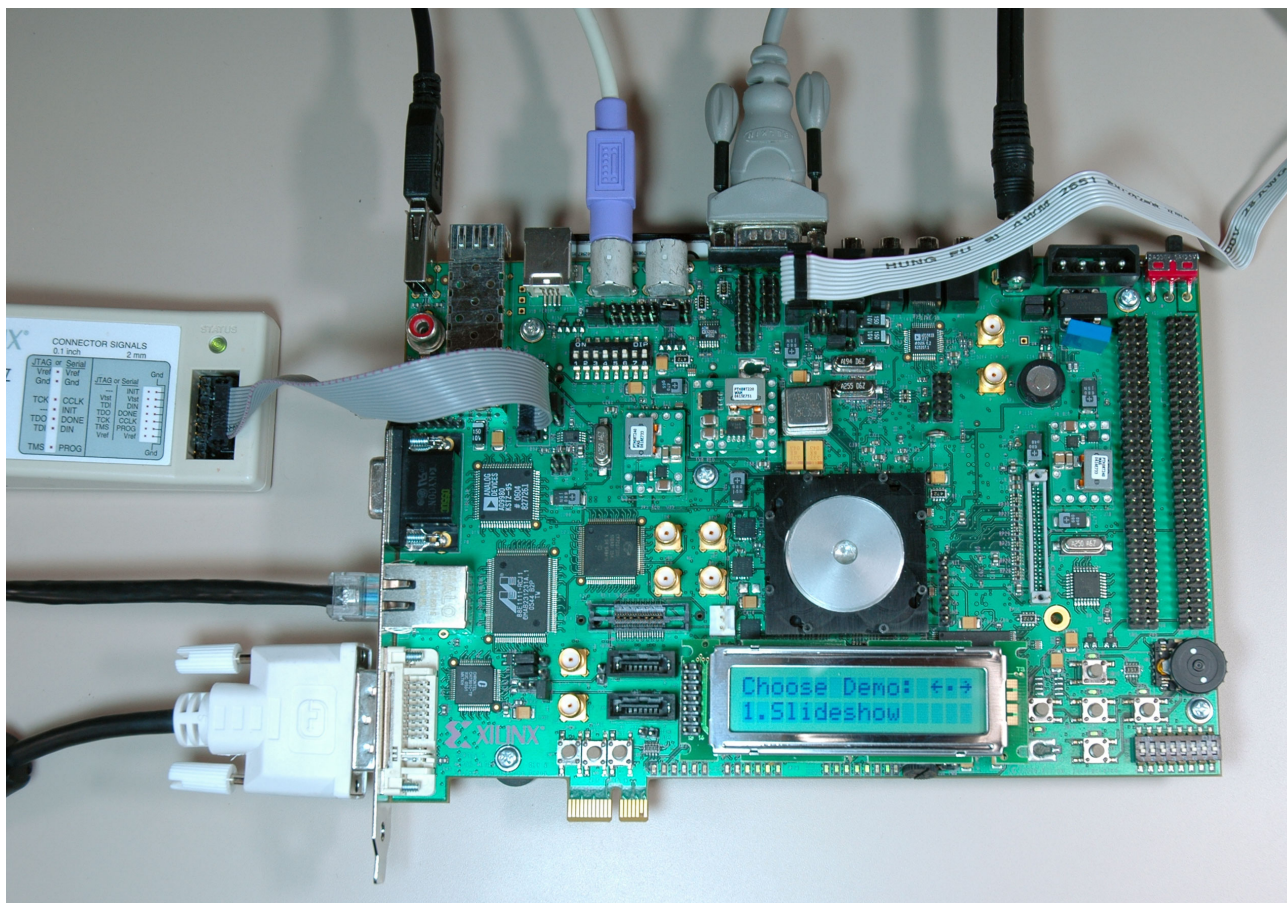
# Verify Factory Default Settings

- Set the Ethernet PHY jumpers, J22, J23 to positions 1-2 (1)
- Insert the Factory CompactFlash into the ML507 board (2)
- Set the Front DIP switches (SW3) to 00010101 (1 = ON) (3)
- Set the Rear DIP switches (SW6) to 11001010 (4)
- Power-up the ML507 board



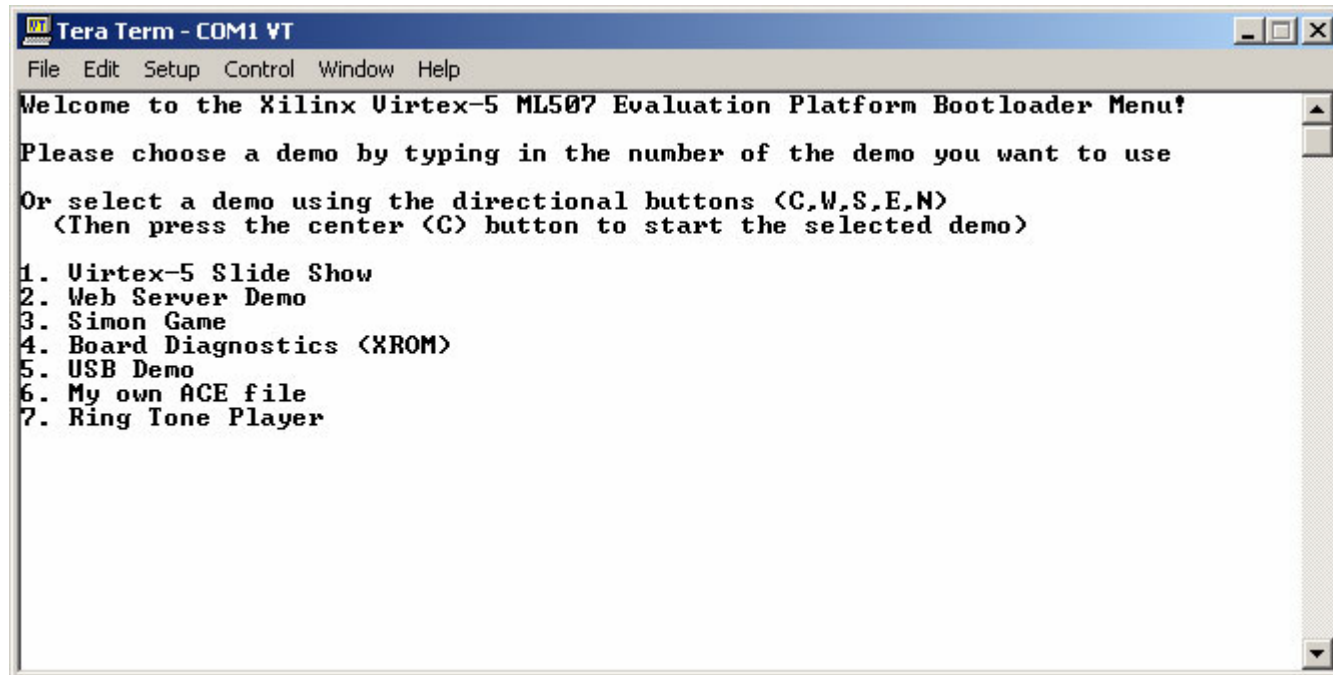
# Bootload

- The bootload\_video.ace loads:



# Bootload

- The terminal window also reflects the bootload application
- Use the left/center/right buttons to choose an application or type a number in the terminal window
- After each demo, push the SysACE reset to return to bootload

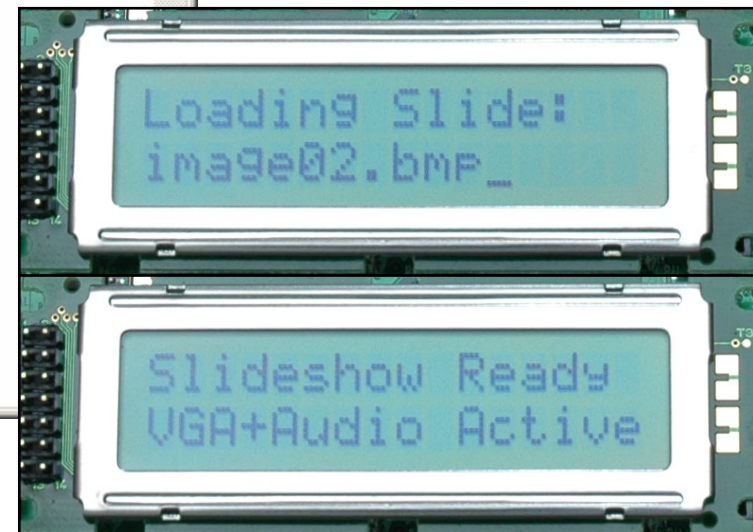


```
Tera Term - COM1 VT
File Edit Setup Control Window Help
Welcome to the Xilinx Virtex-5 ML507 Evaluation Platform Bootloader Menu!
Please choose a demo by typing in the number of the demo you want to use
Or select a demo using the directional buttons (C,W,S,E,N)
(Then press the center (C) button to start the selected demo)
1. Virtex-5 Slide Show
2. Web Server Demo
3. Simon Game
4. Board Diagnostics (XROM)
5. USB Demo
6. My own ACE file
7. Ring Tone Player
```

# Slideshow

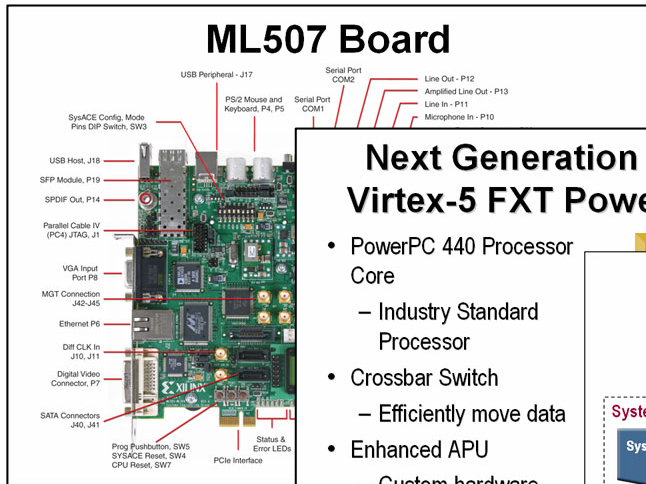
- Type 1, to launch the slideshow application in Configuration 1
- The slideshow loads the presentation into memory then presents it

```
Tera Term - COM1 VT
File Edit Setup Control Window Help
<Then press the center <C> button to start the selected demo>
1. Uirtex-5 Slide Show
2. Web Server Demo
3. Simon Game
4. Board Diagnostics <XROM>
5. USB Demo
6. My own ACE file
7. Ring Tone Player
Rebooting to System ACE Configuration Address 1...
Program running.
Reading file : a:\image01.bmp
Reading file : a:\image02.bmp
Reading file : a:\image03.bmp
Reading file : a:\image04.bmp
Reading file : a:\image05.bmp
Reading file : a:\image06.bmp
Reading file : a:\image07.bmp
Reading file : a:\image08.bmp
Reading file : a:\image09.bmp
Reads done
```



# Slideshow

- The slideshow app will present a series of slides on the Monitor:



### Next Generation of Flexibility: Virtex-5 FXT PowerPC440 Block

- PowerPC 440 Processor Core
  - Industry Standard Processor
- Crossbar Switch
  - Efficiently move data
- Enhanced APU
  - Custom hardware acceleration

*More than just a bet*

### Platform Design Tools Deliver Greater Design Productivity

Third Party EDA Software

DSP

System Generator | PlanAhead ISE

System Design | IP | Planning | HDL Coding | Synthesis | Implementation

High QoR: 30% faster Fmax

HW in the Loop | Veri

### Virtex-5 FPGAs Provide the Right Mix of Memories

- Distributed LUT RAM
  - Fast, localized memories
  - Built-in shift register
  - Great for small FIFOs
- 550 MHz block RAM / FIFO
  - Bigger on-chip memories
  - Built-in FIFO and ECC logic
  - Great for mid-sized FIFOs/buffers
- External memory interfacing
  - Fast connection to popular standards
  - Memory controller cores
  - Ideal for large memory requirements

### LOW-POWER TRANSCIVERS Ultimate Connectivity . . .

Distributed LUT

Low-Power Transceivers 100 Mbps - 3.2 Gbps, < 100 mW

Built-in PCIe Interface

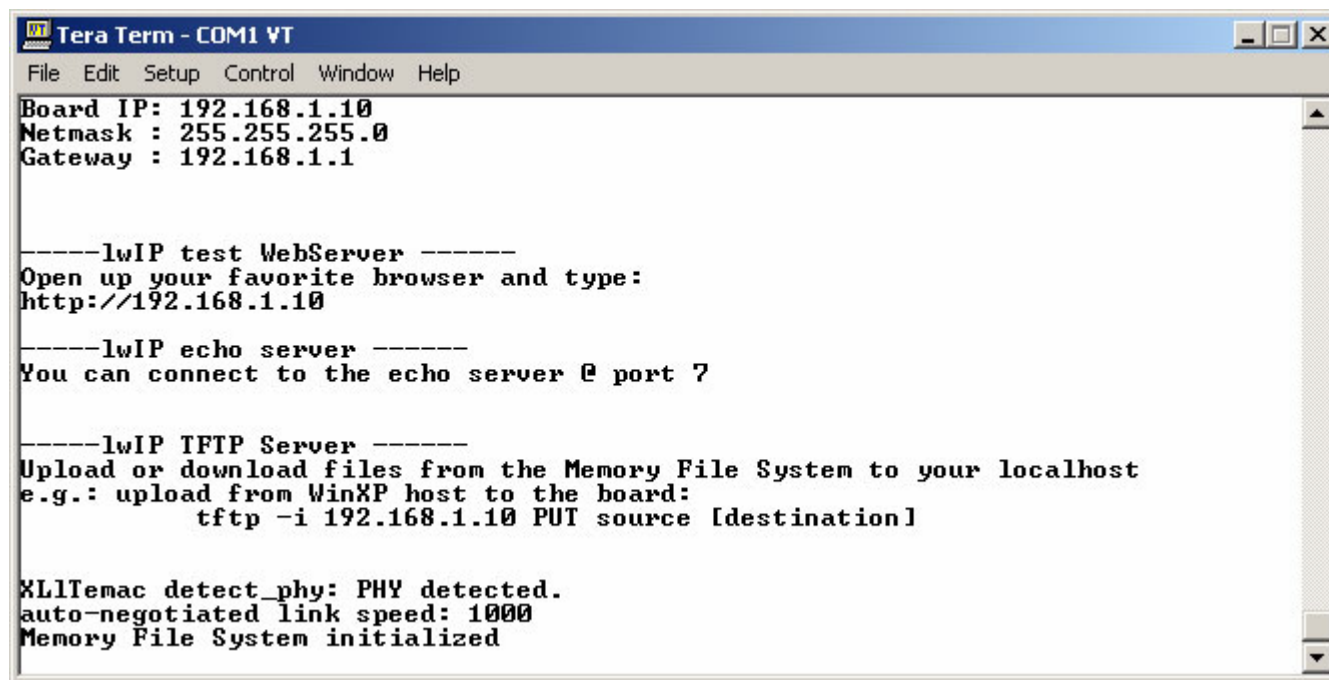
Built-in Ethernet MAC

**VIRTEX 5** Reduce serial I/O power, cost and complexity with the world's first 65nm FPGAs.

With a unique combination of up to 24 low-power transceivers, and built-in PCIe™ and Ethernet MAC blocks, Virtex-5 LXT FPGAs get your system running fast. Whether you are an expert or just starting out, only Xilinx delivers this complete solution to simplify high-speed serial design.

# Web Server

- Type 2, to launch the web server application in Configuration 2
  - **Note:** You may need to turn off your browser's proxy and specify a direct connection to the Internet in your browser options



```
Tera Term - COM1 VT
File Edit Setup Control Window Help
Board IP: 192.168.1.10
Netmask : 255.255.255.0
Gateway : 192.168.1.1

-----lwIP test WebServer -----
Open up your favorite browser and type:
http://192.168.1.10

-----lwIP echo server -----
You can connect to the echo server @ port ?

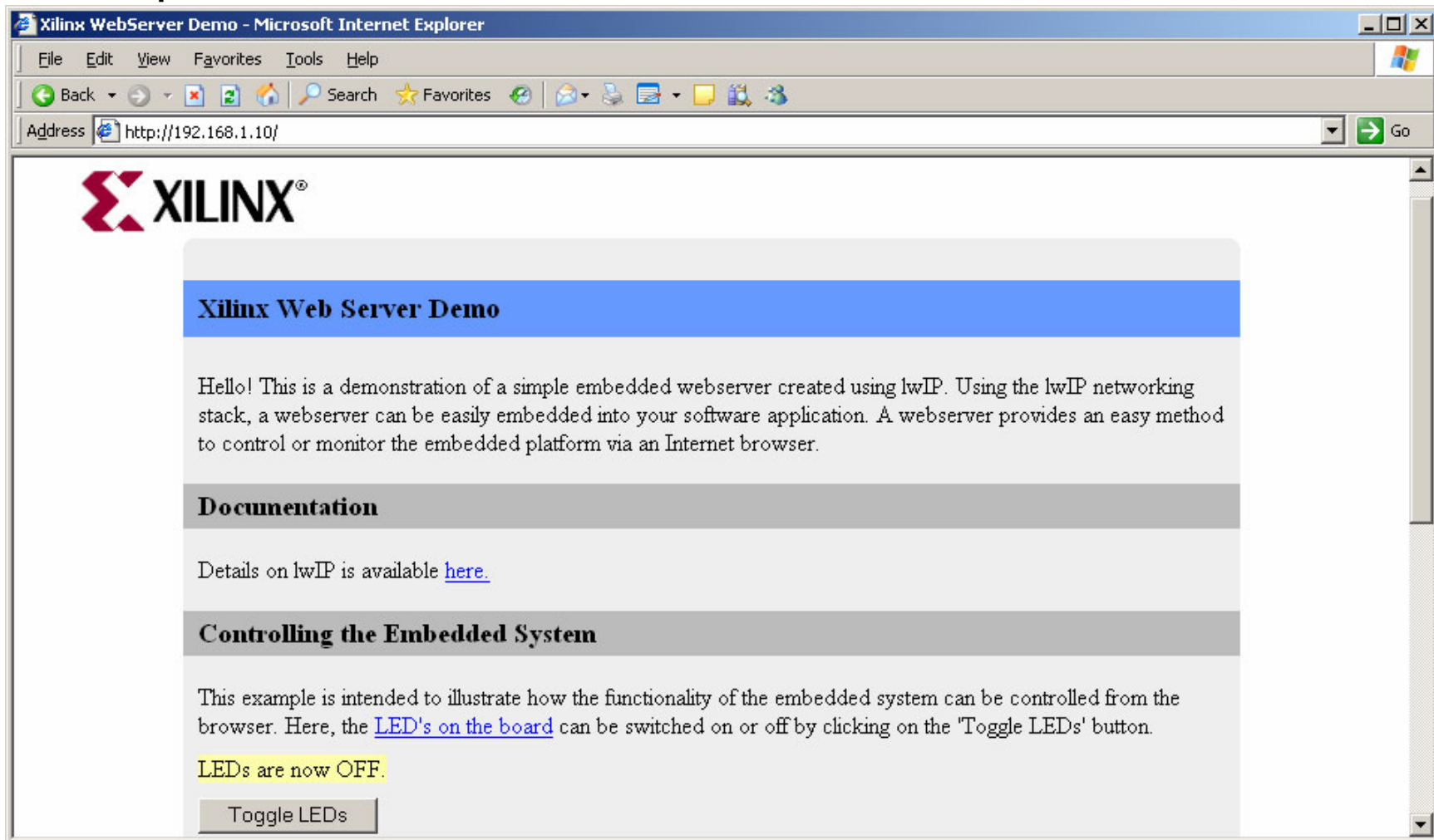
-----lwIP TFTP Server -----
Upload or download files from the Memory File System to your localhost
e.g.: upload from WinXP host to the board:
      tftp -i 192.168.1.10 PUT source [destination]

XLLIemac detect_phy: PHY detected.
auto-negotiated link speed: 1000
Memory File System initialized
```

**Note:** Host IP is 192.168.1.1, subnet mask is 255.255.255.0

# Running the LWIP Demo

- Open a web browser to address 192.168.1.10



The screenshot shows a Microsoft Internet Explorer browser window titled "Xilinx WebServer Demo - Microsoft Internet Explorer". The address bar contains "http://192.168.1.10/". The page content includes the Xilinx logo, a blue header bar with the text "Xilinx Web Server Demo", and a main text area that reads: "Hello! This is a demonstration of a simple embedded webserver created using lwIP. Using the lwIP networking stack, a webserver can be easily embedded into your software application. A webserver provides an easy method to control or monitor the embedded platform via an Internet browser." Below this, there are three sections: "Documentation" with a link to "here", "Controlling the Embedded System" with text about controlling the system via a browser and a link to "LED's on the board", and a status indicator "LEDs are now OFF." followed by a "Toggle LEDs" button.

# Running the LWIP Demo

- Click the Toggle LEDs button; view change on ML507

**Xilinx Web Server Demo**

Hello! This is a demonstration of a simple embedded webserver created using lwIP. Using the lwIP networking stack, a webserver can be easily embedded into your software application. A webserver provides an easy method to control or monitor the embedded platform via an Internet browser.

**Documentation**

Details on lwIP is available [here](#).

**Controlling the Embedded System**

This example is intended to illustrate how the functionality of the embedded system can be controlled from the browser. Here, the [LED's on the board](#) can be switched on or off by clicking on the 'Toggle LEDs' button.

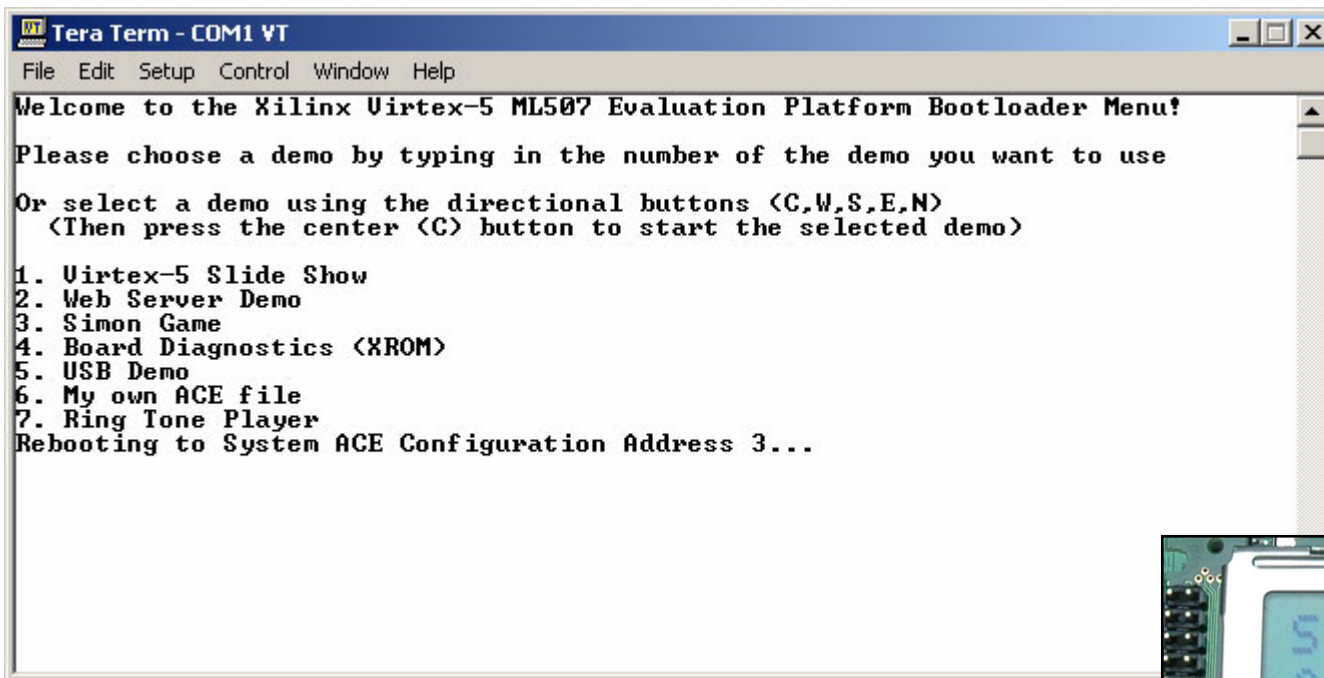
**LEDs are now ON**

Toggle LEDs



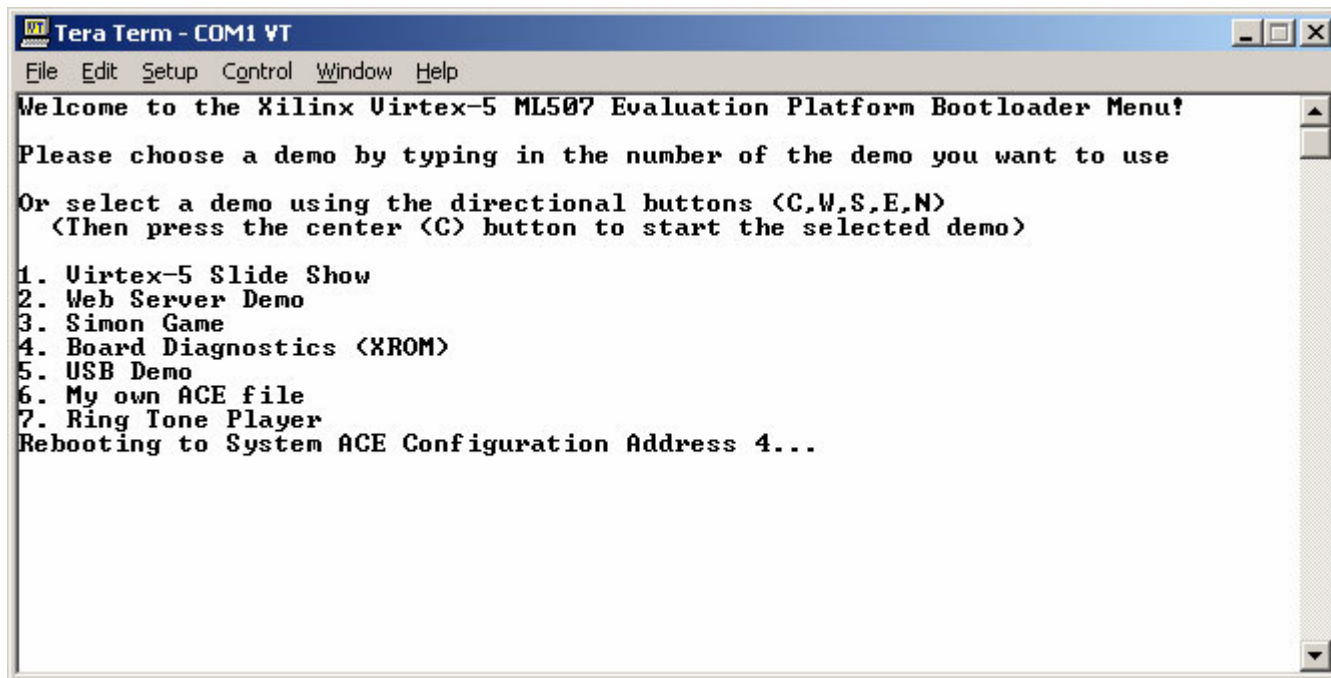
# Simon

- Type 3, to launch the Simon application in Configuration 3



# Board Diagnostics

- Type 4, to launch the XROM application in Configuration 4

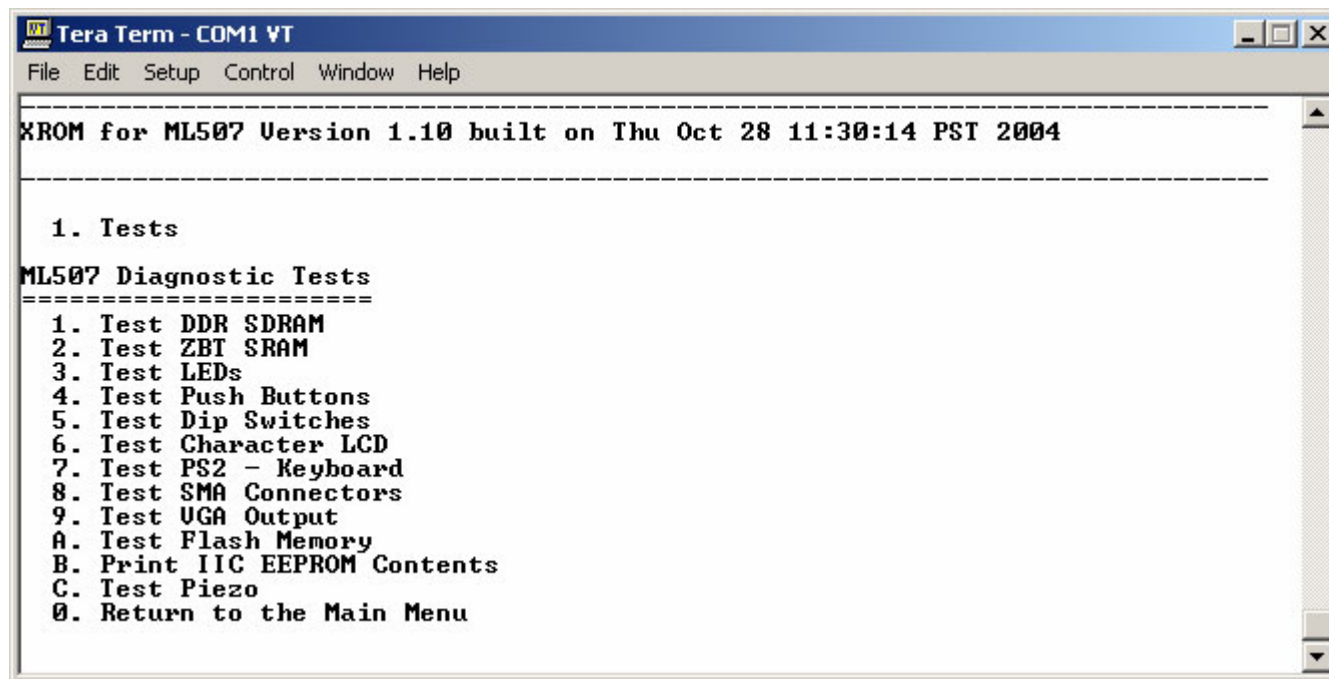


```
Tera Term - COM1 VT
File Edit Setup Control Window Help
Welcome to the Xilinx Virtex-5 ML507 Evaluation Platform Bootloader Menu!
Please choose a demo by typing in the number of the demo you want to use
Or select a demo using the directional buttons (C,W,S,E,N)
(Then press the center (C) button to start the selected demo)
1. Virtex-5 Slide Show
2. Web Server Demo
3. Simon Game
4. Board Diagnostics (XROM)
5. USB Demo
6. My own ACE file
7. Ring Tone Player
Rebooting to System ACE Configuration Address 4...
```



# Board Diagnostics

- XROM includes a series of board test routines

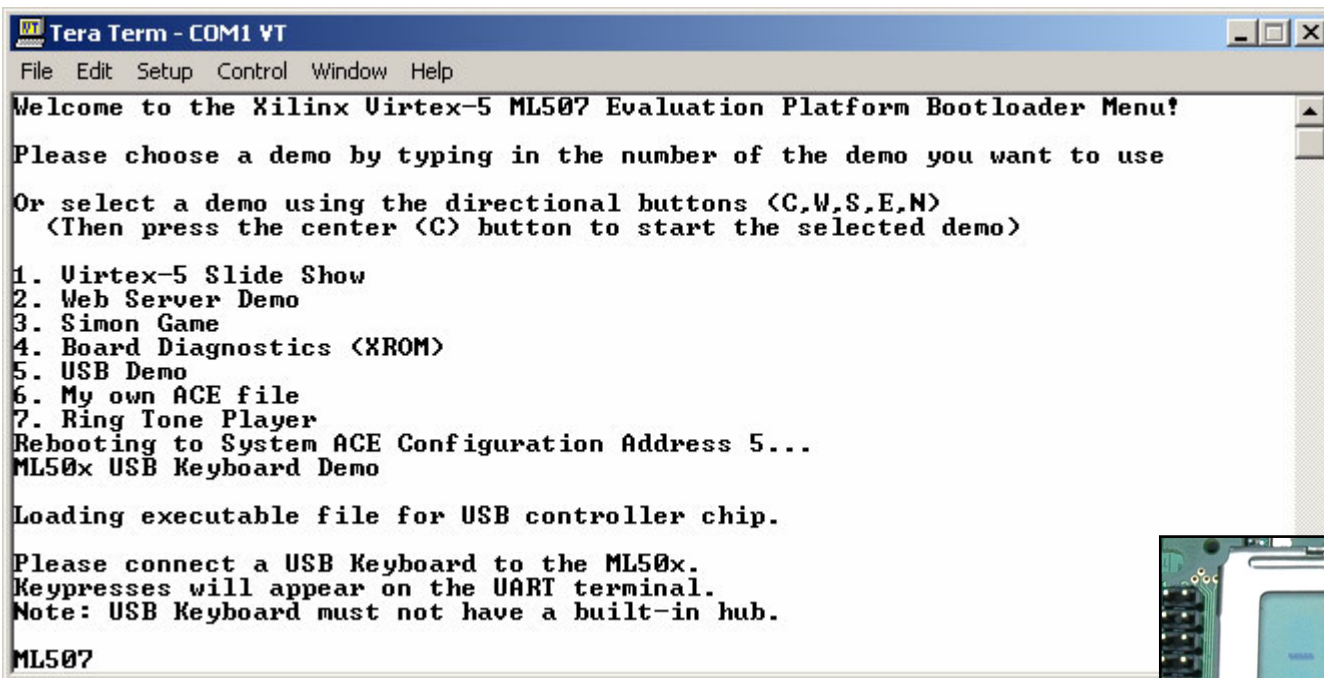


```
Tera Term - COM1 VT
File Edit Setup Control Window Help
-----
XROM for ML507 Version 1.10 built on Thu Oct 28 11:30:14 PST 2004
-----
1. Tests
ML507 Diagnostic Tests
-----
1. Test DDR SDRAM
2. Test ZBT SRAM
3. Test LEDs
4. Test Push Buttons
5. Test Dip Switches
6. Test Character LCD
7. Test PS2 - Keyboard
8. Test SMA Connectors
9. Test UGA Output
A. Test Flash Memory
B. Print IIC EEPROM Contents
C. Test Piezo
0. Return to the Main Menu
```



# USB Keyboard

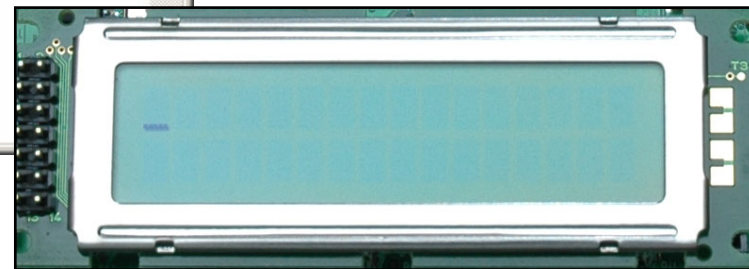
- Type 5, to launch the USB Keyboard application in Configuration 5
- Type **ML507** and view results:



```
Tera Term - COM1 VT
File Edit Setup Control Window Help
Welcome to the Xilinx Virtex-5 ML507 Evaluation Platform Bootloader Menu!
Please choose a demo by typing in the number of the demo you want to use
Or select a demo using the directional buttons <C,W,S,E,N>
<Then press the center <C> button to start the selected demo>
1. Virtex-5 Slide Show
2. Web Server Demo
3. Simon Game
4. Board Diagnostics <XROM>
5. USB Demo
6. My own ACE file
7. Ring Tone Player
Rebooting to System ACE Configuration Address 5...
ML50x USB Keyboard Demo

Loading executable file for USB controller chip.

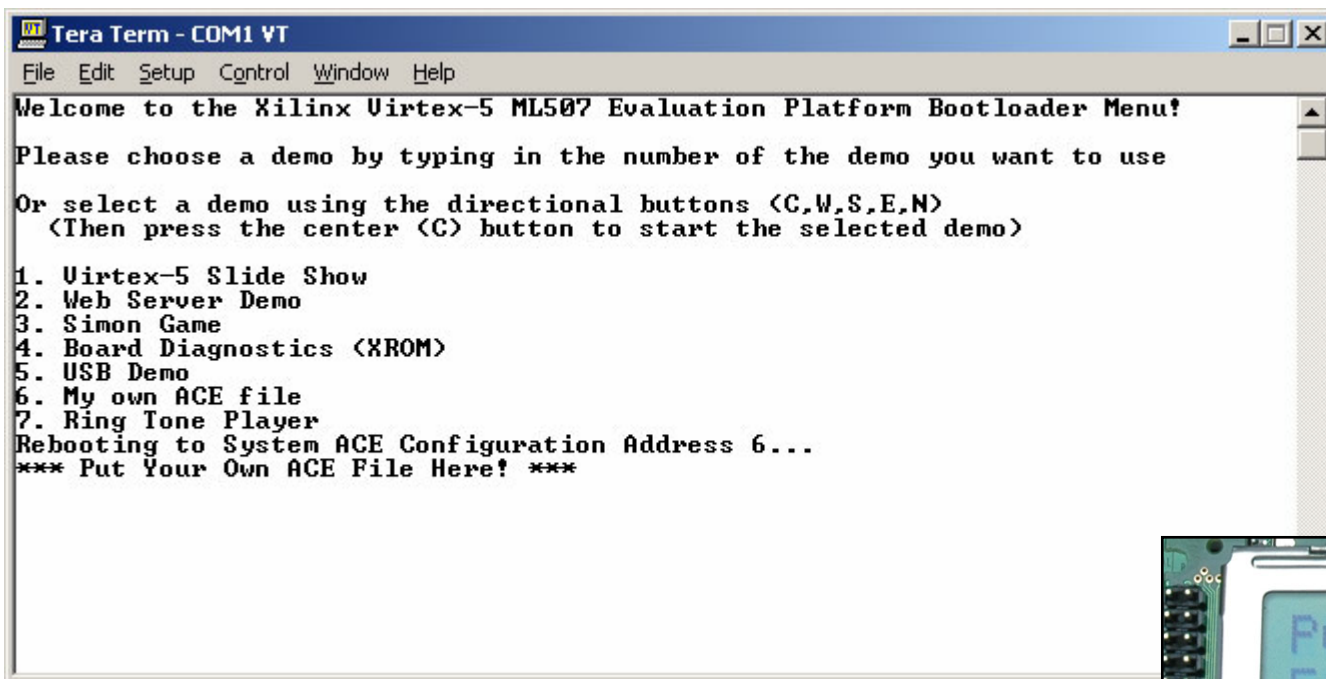
Please connect a USB Keyboard to the ML50x.
Keypresses will appear on the UART terminal.
Note: USB Keyboard must not have a built-in hub.
ML507
```



**Note:** Attach keyboard after demo loads

# My ACE

- Type 6, to launch the My ACE application in Configuration 6

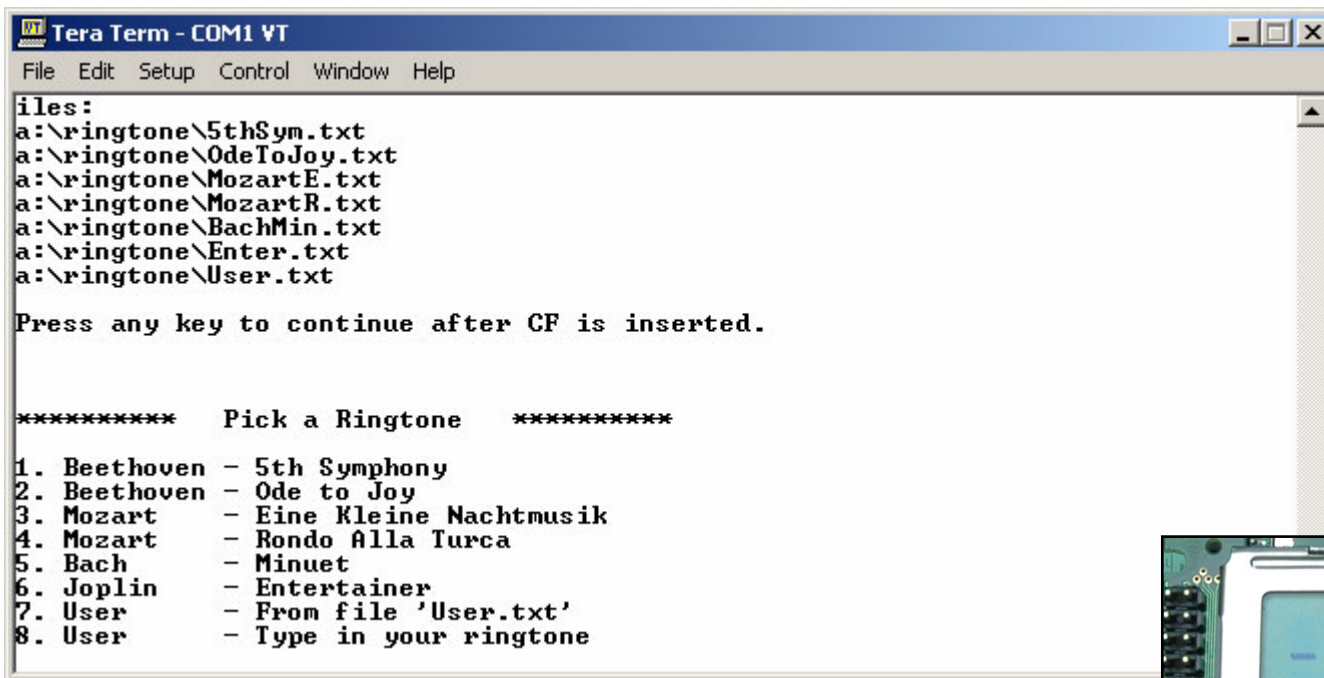


```
Tera Term - COM1 VT
File Edit Setup Control Window Help
Welcome to the Xilinx Virtex-5 ML507 Evaluation Platform Bootloader Menu!
Please choose a demo by typing in the number of the demo you want to use
Or select a demo using the directional buttons <C,W,S,E,N>
(Then press the center <C> button to start the selected demo)
1. Virtex-5 Slide Show
2. Web Server Demo
3. Simon Game
4. Board Diagnostics <XROM>
5. USB Demo
6. My own ACE file
7. Ring Tone Player
Rebooting to System ACE Configuration Address 6...
*** Put Your Own ACE File Here! ***
```



# Ringtone

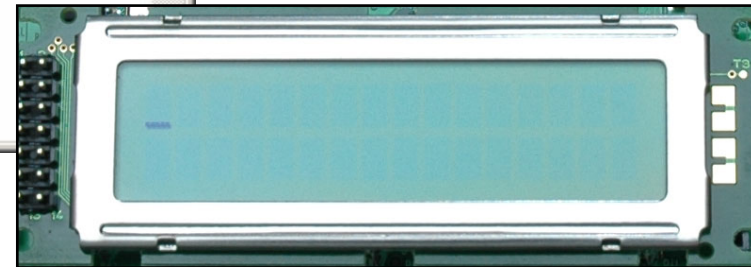
- Type 7, to launch the Ringtone application in Configuration 7
- Press any key then press 1-7 to play a simple melody



```
Tera Term - COM1 VT
File Edit Setup Control Window Help
files:
a:\ringtone\5thSym.txt
a:\ringtone\OdeToJoy.txt
a:\ringtone\MozartE.txt
a:\ringtone\MozartR.txt
a:\ringtone\BachMin.txt
a:\ringtone\Enter.txt
a:\ringtone\User.txt

Press any key to continue after CF is inserted.

***** Pick a Ringtone *****
1. Beethoven - 5th Symphony
2. Beethoven - Ode to Joy
3. Mozart - Eine Kleine Nachtmusik
4. Mozart - Rondo Alla Turca
5. Bach - Minuet
6. Joplin - Entertainer
7. User - From file 'User.txt'
8. User - Type in your ringtone
```



# Documentation

- Virtex-5
  - Silicon Devices  
<http://www.xilinx.com/products/devices.htm>
  - Virtex-5 Multi-Platform FPGA  
<http://www.xilinx.com/products/virtex5/index.htm>
  - Virtex-5 Family Overview: LX, LXT, SXT, and FXT Platforms  
[http://www.xilinx.com/support/documentation/data\\_sheets/ds100.pdf](http://www.xilinx.com/support/documentation/data_sheets/ds100.pdf)
  - Virtex-5 FPGA DC and Switching Characteristics Data Sheet  
[http://www.xilinx.com/support/documentation/data\\_sheets/ds202.pdf](http://www.xilinx.com/support/documentation/data_sheets/ds202.pdf)



# Documentation

- Virtex-5
  - Virtex-5 FPGA User Guide  
[http://www.xilinx.com/support/documentation/user\\_guides/ug190.pdf](http://www.xilinx.com/support/documentation/user_guides/ug190.pdf)
  - Virtex-5 FPGA Configuration User Guide  
[http://www.xilinx.com/support/documentation/user\\_guides/ug191.pdf](http://www.xilinx.com/support/documentation/user_guides/ug191.pdf)
  - Virtex-5 System Monitor User Guide  
[http://www.xilinx.com/support/documentation/user\\_guides/ug192.pdf](http://www.xilinx.com/support/documentation/user_guides/ug192.pdf)
  - Virtex-5 Packaging and Pinout Specification  
[http://www.xilinx.com/support/documentation/user\\_guides/ug195.pdf](http://www.xilinx.com/support/documentation/user_guides/ug195.pdf)





# Documentation

- Virtex-5 RocketIO

- RocketIO GTP Transceivers

<http://www.xilinx.com/products/virtex5/lxt.htm>

- RocketIO GTP Transceiver User Guide – UG196

[http://www.xilinx.com/support/documentation/user\\_guides/ug196.pdf](http://www.xilinx.com/support/documentation/user_guides/ug196.pdf)

- RocketIO GTX Transceivers

<http://www.xilinx.com/products/virtex5/fxt.htm>

- RocketIO GTX Transceiver User Guide – UG198

[http://www.xilinx.com/support/documentation/user\\_guides/ug198.pdf](http://www.xilinx.com/support/documentation/user_guides/ug198.pdf)



# Documentation

- Design Resources

- ISE Development Tools and IP

<http://www.xilinx.com/ise>

- Integrated Software Environment (ISE) Foundation Resources

[http://www.xilinx.com/ise/logic\\_design\\_prod/foundation.htm](http://www.xilinx.com/ise/logic_design_prod/foundation.htm)

- ISE Manuals

[http://www.xilinx.com/support/software\\_manuals.htm](http://www.xilinx.com/support/software_manuals.htm)

- ISE Development System Reference Guide

<http://toolbox.xilinx.com/docsan/xilinx10/books/docs/dev/dev.pdf>

- ISE Development System Libraries Guide

[http://toolbox.xilinx.com/docsan/xilinx10/books/docs/virtex5\\_hdl/virtex5\\_hdl.pdf](http://toolbox.xilinx.com/docsan/xilinx10/books/docs/virtex5_hdl/virtex5_hdl.pdf)



# Documentation

- Additional Design Resources
  - Customer Support  
<http://www.xilinx.com/support>
  - Xilinx Design Services:  
<http://www.xilinx.com/xds>
  - Titanium Dedicated Engineering:  
<http://www.xilinx.com/titanium>
  - Education Services:  
<http://www.xilinx.com/education>
  - Xilinx On Board (Board and kit locator):  
<http://www.xilinx.com/xob>



# Documentation

- Platform Studio
  - Embedded Development Kit (EDK) Resources  
<http://www.xilinx.com/edk>
  - Embedded System Tools Reference Manual  
[http://www.xilinx.com/support/documentation/sw\\_manuals/edk10\\_est\\_rm.pdf](http://www.xilinx.com/support/documentation/sw_manuals/edk10_est_rm.pdf)
  - EDK Concepts, Tools, and Techniques  
[http://www.xilinx.com/support/documentation/sw\\_manuals/edk\\_ctt.pdf](http://www.xilinx.com/support/documentation/sw_manuals/edk_ctt.pdf)



# Documentation

- PowerPC 440
  - Embedded Processor Block in Virtex-5 FPGAs Reference Guide – UG200  
[http://www.xilinx.com/support/documentation/user\\_guides/ug200.pdf](http://www.xilinx.com/support/documentation/user_guides/ug200.pdf)
  - PPC440 Virtex-5 Wrapper – DS621  
[http://www.xilinx.com/support/documentation/ip\\_documentation/ppc440\\_virtex5.pdf](http://www.xilinx.com/support/documentation/ip_documentation/ppc440_virtex5.pdf)
  - DDR2 Memory Controller for PowerPC 440 Processors – DS567  
[http://www.xilinx.com/support/documentation/data\\_sheets/ds567.pdf](http://www.xilinx.com/support/documentation/data_sheets/ds567.pdf)



# Documentation

- MicroBlaze
  - MicroBlaze Processor  
<http://www.xilinx.com/microblaze>
  - MicroBlaze Processor Reference Guide – UG081  
[http://www.xilinx.com/support/documentation/sw\\_manuals/mb\\_ref\\_guide.pdf](http://www.xilinx.com/support/documentation/sw_manuals/mb_ref_guide.pdf)



# Documentation

- ChipScope Pro
  - ChipScope Pro 10.1i Serial IO Toolkit User Manual  
[http://www.xilinx.com/ise/verification/chipscope\\_pro\\_siotk\\_10\\_1\\_ug213.pdf](http://www.xilinx.com/ise/verification/chipscope_pro_siotk_10_1_ug213.pdf)
  - ChipScope Pro 10.1i ChipScope Pro Software and Cores User Guide  
[http://www.xilinx.com/ise/verification/chipscope\\_pro\\_sw\\_cores\\_10\\_1\\_ug029.pdf](http://www.xilinx.com/ise/verification/chipscope_pro_sw_cores_10_1_ug029.pdf)



# Documentation

- Memory Solutions

- Demos on Demand – Memory Interface Solutions with Xilinx FPGAs

[http://www.demosondemand.com/clients/xilinx/001/page\\_new2/index.asp#35](http://www.demosondemand.com/clients/xilinx/001/page_new2/index.asp#35)

- Xilinx Memory Corner

[http://www.xilinx.com/products/design\\_resources/mem\\_corner](http://www.xilinx.com/products/design_resources/mem_corner)

- Additional Memory Resources

<http://www.xilinx.com/support/software/memory/protected/index.htm>

- Xilinx Memory Interface Generator (MIG) 2.1 User Guide

<http://www.xilinx.com/support/software/memory/protected/ug086.pdf>

- Memory Interfaces Made Easy with Xilinx FPGAs and the Memory Interface Generator

[http://www.xilinx.com/support/documentation/white\\_papers/wp260.pdf](http://www.xilinx.com/support/documentation/white_papers/wp260.pdf)





# Documentation

- Ethernet

- Virtex-5 Embedded Tri-Mode Ethernet MAC Wrapper Data Sheet

[http://www.xilinx.com/support/documentation/ip\\_documentation/v5\\_emac\\_ds550.pdf](http://www.xilinx.com/support/documentation/ip_documentation/v5_emac_ds550.pdf)

- Virtex-5 Embedded Tri-Mode Ethernet MAC Wrapper Getting Started Guide

[http://www.xilinx.com/support/documentation/ip\\_documentation/v5\\_emac\\_gsg340.pdf](http://www.xilinx.com/support/documentation/ip_documentation/v5_emac_gsg340.pdf)

- Virtex-5 Tri-Mode Ethernet Media Access Controller User Guide

[http://www.xilinx.com/support/documentation/user\\_guides/ug194.pdf](http://www.xilinx.com/support/documentation/user_guides/ug194.pdf)

- LightWeight IP (lwIP) Application Examples – XAPP1026

[http://www.xilinx.com/support/documentation/application\\_notes/xapp1026.pdf](http://www.xilinx.com/support/documentation/application_notes/xapp1026.pdf)



# Documentation

- PCIe
  - LogiCORE Endpoint Block Plus for PCI Express Data Sheet  
[http://www.xilinx.com/support/documentation/ip\\_documentation/pcie\\_blk\\_plus\\_ds551.pdf](http://www.xilinx.com/support/documentation/ip_documentation/pcie_blk_plus_ds551.pdf)
  - LogiCORE Endpoint Block Plus for PCI Express Designs  
[http://www.xilinx.com/support/documentation/ip\\_documentation/pcie\\_blk\\_plus\\_ug341.pdf](http://www.xilinx.com/support/documentation/ip_documentation/pcie_blk_plus_ug341.pdf)
  - LogiCORE Endpoint Block Plus Getting Started Guide for PCI Express Designs  
[http://www.xilinx.com/support/documentation/ip\\_documentation/pcie\\_blk\\_plus\\_gsg343.pdf](http://www.xilinx.com/support/documentation/ip_documentation/pcie_blk_plus_gsg343.pdf)
  - Virtex-5 Integrated Endpoint Block User Guide for PCI Express Designs  
[http://www.xilinx.com/support/documentation/user\\_guides/ug197.pdf](http://www.xilinx.com/support/documentation/user_guides/ug197.pdf)



# Documentation

- System Generator
  - System Generator for DSP  
<http://www.xilinx.com/sysgen>
  - Xilinx System Generator for DSP User Guides  
[http://www.xilinx.com/support/documentation/sw\\_manuals/sysgen\\_bklist.pdf](http://www.xilinx.com/support/documentation/sw_manuals/sysgen_bklist.pdf)
  - XtremeDSP Design Considerations  
[http://www.xilinx.com/support/documentation/user\\_guides/ug193.pdf](http://www.xilinx.com/support/documentation/user_guides/ug193.pdf)



# Documentation

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- ML505/506/507
  - ML505 Overview  
<http://www.xilinx.com/ml505>
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  - ML505/506/507 Evaluation Platform User Guide – UG347  
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  - ML505/506/507 Getting Started Tutorial – UG348  
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- ML505/506/507
  - ML505/506/507 Schematics  
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