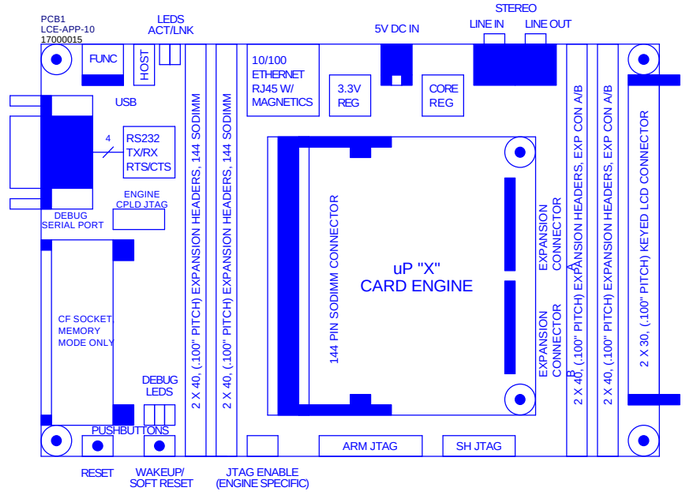
01 - TITLE PAGE

PROJECT:	LCE-APP-10
PART NUMBER:	80000116
ASSEMBLY NAME:	Zoom SDK Application Kit
SCHEMATICS:	ECR

TABLE OF CONTENTS



COLOR LEGEND

NOTE:
NOTES IN GREEN TEXT ARE GENERAL DESIGN OR SCHEMATIC NOTES

LAYOUT NOTE:
NOTES IN RED TEXT ARE PCB LAYOUT RECOMMENDATIONS OR GUIDLINES

NET NAMES

NET NAMES IN GREEN TEXT ARE NETS THAT ARE NOT DIRECTLY CONNECTED WITH A VISIBLE WIRE ON SINGLE SCHEMATIC PAGE, BUT USE THIS CONVENTION TO MAKE THE SCHEMATIC EASIER TO READ

NET NOTE

NET NOTES IN BLACK TEXT INDICATE A PARTICULAR FUNCTIONALITY OF A SPECIFIC NET, IT IS NOT A NET NAME MERELY TEXT AND HAS NO AFFECT ON THE DRC.

REVISIONS A->F:

1. SUBMITTED PART FOR LCE-APP-10 AND UPDATED BLOCK DIAGRAM AND TITLE PAGE

Schematic Modify Date = Friday, April 16, 2004

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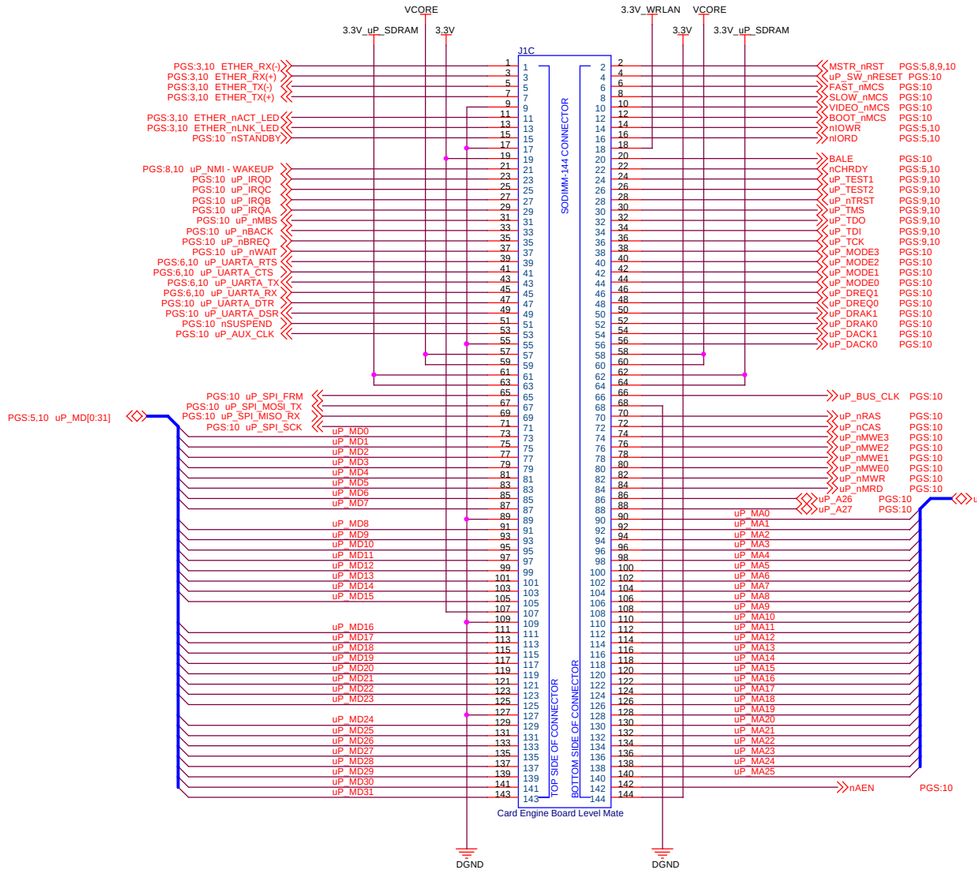
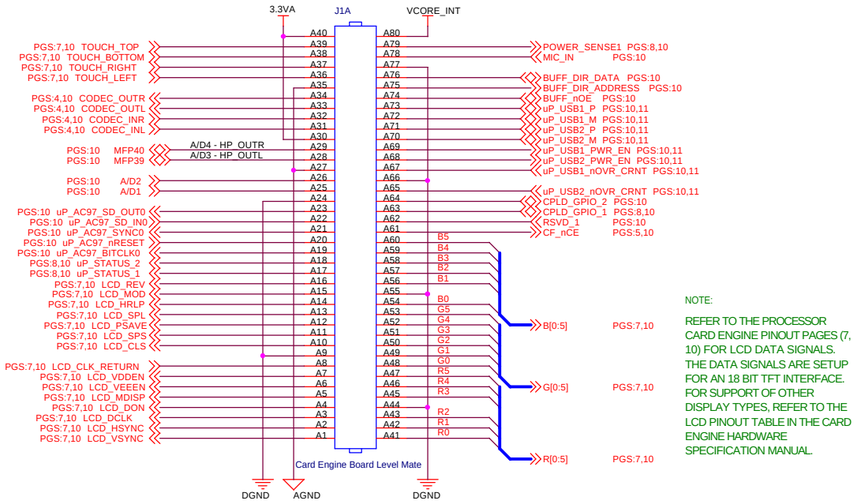
02 - EXPANSION BUS

NOTE:

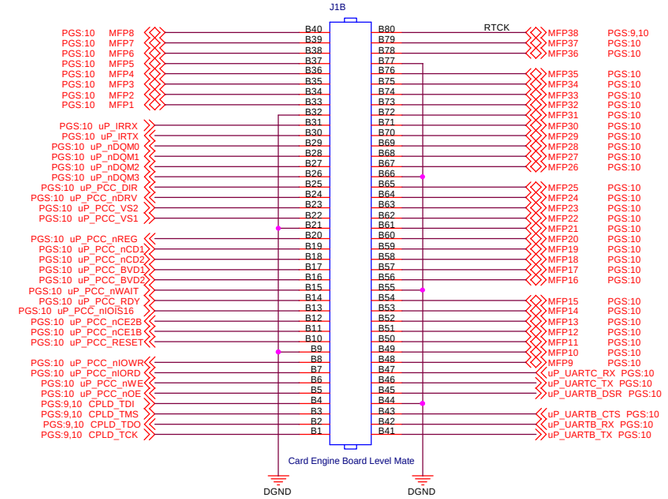
NOT ALL CARD ENGINES WILL HAVE ALL THESE SIGNALS, PLEASE SEE SPECIFIC CARD ENGINE HARDWARE SPEC FOR DETAILED PINOUT AND SIGNAL INFORMATION.

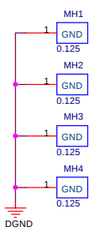




NOTE:

REFER TO THE PROCESSOR CARD ENGINE PINOUT PAGES (7, 10) FOR LCD DATA SIGNALS. THE DATA SIGNALS ARE SETUP FOR AN 18 BIT TFT INTERFACE. FOR SUPPORT OF OTHER DISPLAY TYPES, REFER TO THE LCD PINOUT TABLE IN THE CARD ENGINE HARDWARE SPECIFICATION MANUAL.





REVISIONS C->D:

1. CHANGED NETS
A39 - TOUCH_TOP (was TOUCHX2)
A38 - TOUCH_BOTTOM (was TOUCHX)
A37 - TOUCH_RIGHT (was TOUCHY2)
A36 - TOUCH_LEFT (was TOUCHY)

2. REMOVED THE NET CF_RDYnBSY AND RENAMED THE NET RSVD_1

REVISIONS D->E:

1. CHANGED NET NAME OF uP_NMI (J1C.21) TO uP_NMI - WAKEUP TO ACCOMODATE THE a400 AND A404.

REVISIONS B->C:

1. SEPARATED THE 3.3V AND 3.3V_uP_SDRAM ON PINS 61-64 OF THE SODIMM CON
2. ADDED 3.3V_WRLAN TO THE DIMM CONNECTOR J1C.19
3. CHANGED NET NAMES TO FOLLOW NEW NAMING CONVENTION SHOWING ACTIVE LEVEL IE. MSTR_RST -> MSTR_nRST.
4. ADDED SIGNAL uP_RTCK TO MFG38 FROM THE 20PIN JTAG HEADER
5. SWITCHED THE PINS ON J1A THAT NETS LCD_PSAVE AND LCE_REV GO TO
6. RENAMED NET LCD_CLKIN -> LCD_CLK_RETURN AND NET LCD_CLKOUT -> LCD_DCLK
7. REMOVED R22

REVISIONS A->B:

1. CHANGED DIRECTION OF NETS LCD_CLKIN AND LCD_CLKOUT
2. CHANGED THE NAMES OF THE LCD DATA LINES
3. CHANGED THE NET NAMES OF EVB1 AND EVB2 TO CF_nCE AND CF_BSYnRDY RESPECTIVELY

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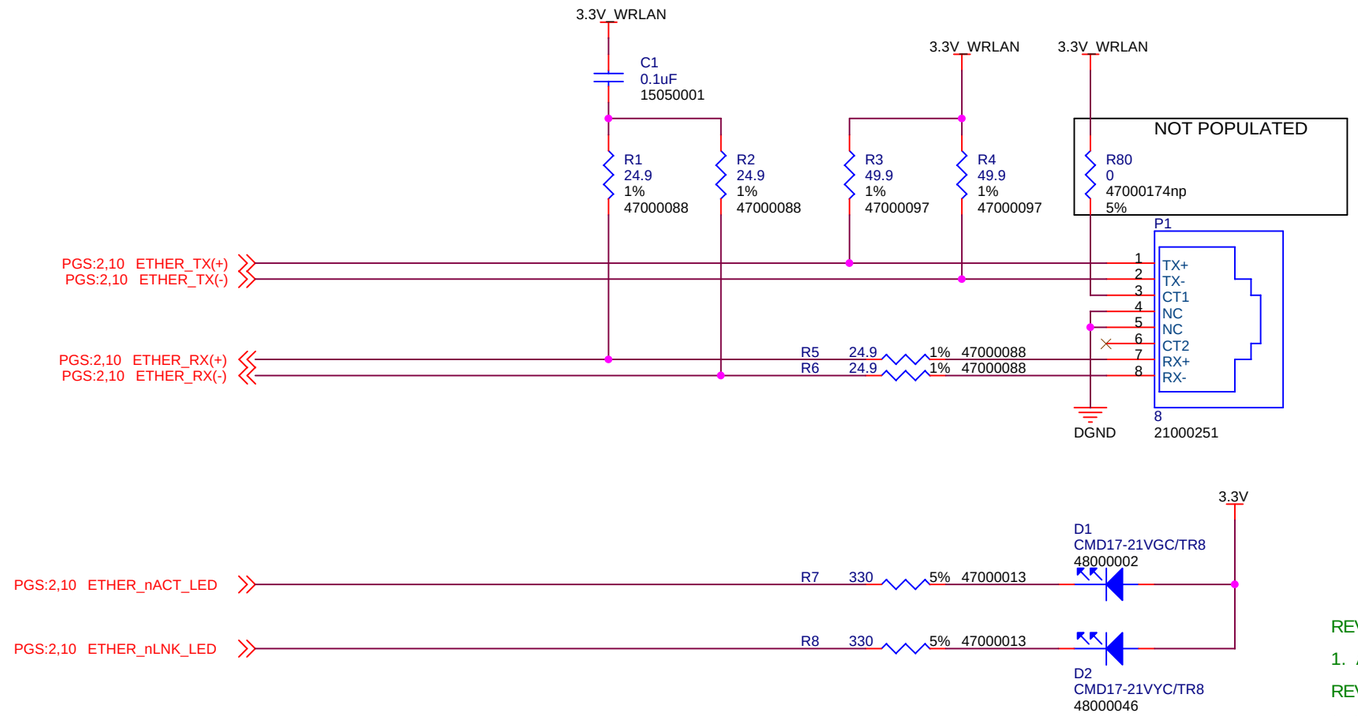
03 - ENGINE ETHERNET



REVISIONS F->G:

1. ADDED BOX AROUND THE NO POP RESISTOR ON ENET CONNECTOR

REVISIONS C->F:

1. CONNECTED CT1 TO 3.3V_WRLAN PER 91C111 SCHEMATIC CHECKLIST PROVIDED BY SMSC
2. CHANGED THE CONNECTION OF CT1 TO 3.3V_WRLAN DIRECTLY TO ONE THAT USES A 0OHM (R80) UNTIL QA HAS BEEN COMPLETED.

REVISIONS B->C:

1. CHANGED THE IMPEDENCE MATCHING VOLTAGE ON THE ENET TX AND RX LINES TO 3.3V_WRLAN
2. CHANGED THE NET NAMES OF THE LNK AND ACT LED NETS TO ETHER_nACT_LED AND ETHER_nLNK_LED
3. CHANGED THE NET NAMES OF THE LNK AND ACT LED NETS TO ETHER_nACT_LED AND ETHER_nLNK_LED
4. CHANGED R3 AND R4 FROM 47 OHM 5%'S TO 49.9 OHM 1%'S
5. GROUNDED PINS 4 AND 5 OF P1, PER PULSE CONNECTOR SPEC
6. CHANGED R1,R2,R5,R6 FROM 24 OHM 5%'S TO 24.9 OHM 1%'S

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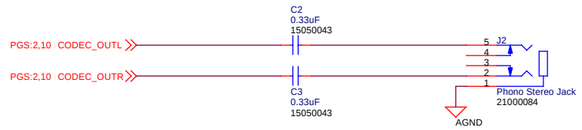
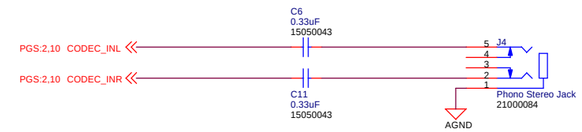
04 - AUDIO

LINE OUT



LINE IN



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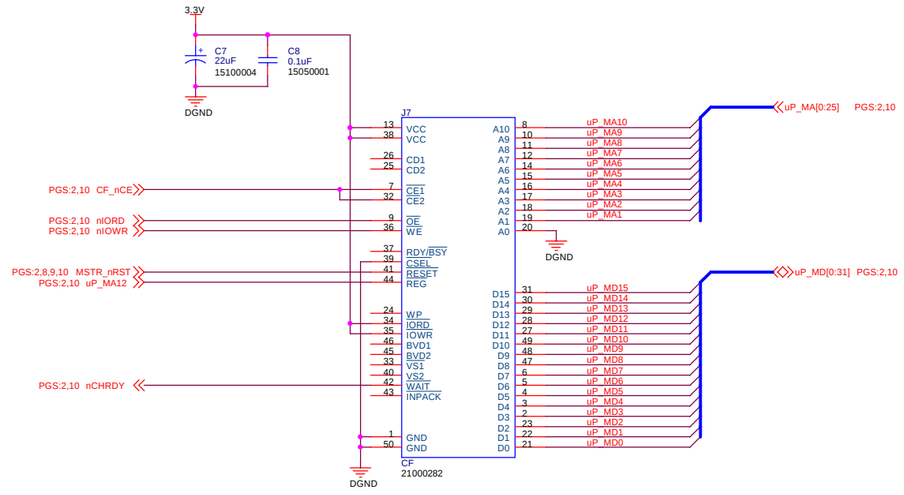
05 - CF CARD

COMPACT FLASH
SOCKET MEMORY
MODE ONLY



REVISIONS F->G:

1. REMOVED A0 FROM CF CONNECTOR FOR COMPATABILITY WITH A400 BSC IN A 16BIT AREA

REVISIONS C->D:

1. CHANGED NET THAT CONNECTS TO REG ON J7.44 FROM uP_MA13 TO uP_MA12
2. REMOVED THE NET CF_RDYnBSY

REVISIONS B->C:

1. CHANGED NET THAT CONNECTS TO REG ON J7.44 FROM uP_MA11 TO uP_MA13
2. REMOVED PULLUP ON CF_RDYnBSY

REVISIONS A->B:

1. ADDED NET uP_MA3 TO J7.17 FOR 16BIT ADDRESSABILITY
2. CHANGED NETS MFP3 AND MFP6 TO EVB1 AND EVB2
3. REMOVED NET uP_MA0 AND TIED THAT PIN ON J7 TO GND
4. REMOVED HOT SWAPPABILITY, DELETED NETS uP_PCCDRV AND CF_3.3V, AND COMPONENTS Q1, C10
5. ADDED ADDRESS LINES uP_MA0,4-9 AND uP_MA11 FOR GREATER FUNCTIONALITY AND USABILITY OF MORE CF CARDS
6. CHANGED THE NET NAMES OF EVB1 AND EVB2 TO CF_nCE AND CF_BSYnRDY RESPECTIVELY

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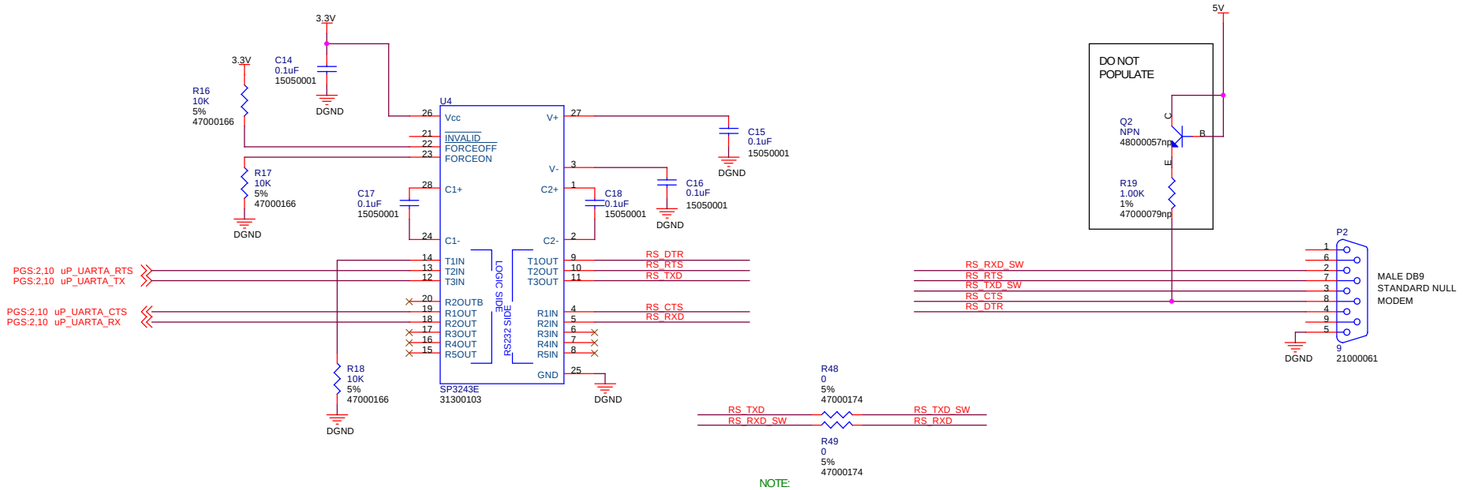
06 - RS232 AND DB9 CONNECTOR

SERIAL PORT



NOTE:

R48 AND R49 PROVIDE THE OPTION FOR SWITCHING RX AND TX AT THE DB9 CONNECTOR

REVISIONS B->C:

1. CHANGED REF DES FOR Q2np and R19np TO Q2 AND R19

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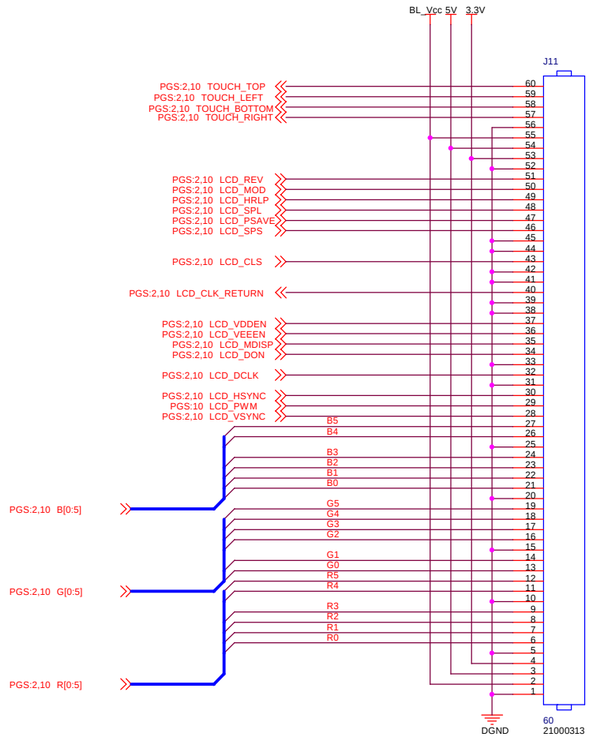
07 - VIDEO

NOTE:

THE NET BL_Vcc IS CONNECTED TO A 2PIN HEADER J40 ON PAGE 8.



NOTE:

REFER TO THE PROCESSOR CARD ENGINE PINOUT PAGES (7, 10) FOR LCD DATA SIGNALS. THE DATA SIGNALS ARE SETUP FOR AN 18 BIT TFT INTERFACE. FOR SUPPORT OF OTHER DISPLAY TYPES, REFER TO THE LCD PINOUT TABLE IN THE CARD ENGINE HARDWARE SPECIFICATION MANUAL.

NOTE:

THIS CONNECTOR IS ACTUALLY A 30X2 DUAL ROW .100" PITCH, .025"SQ POST MALE HEADER. IT IS REPRESENTED SYMBOLICALLY AS A SINGLE ROW CONNECTOR TO ILLUSTRATE HOW THE SIGNALS WILL ROUTE THROUGH THE RIBBON CABLE.

REVISIONS C->D:

1. CHANGED NETS
A39 - TOUCH_TOP (was TOUCHX2)
A38 - TOUCH_BOTTOM (was TOUCHX)
A37 - TOUCH_RIGHT (was TOUCHY2)
A36 - TOUCH_LEFT (was TOUCHY)

REVISIONS B->C:

1. CHANGED THE 60PIN LCD CONNECTOR J11 TO A SHROUDED/KEYEDW EJECTOR TABS TYPE
2. SWITCHED THE PINS ON J11 THAT NETS LCD_PSAVE AND LCE_REV GO TO
3. RENAMED NET LCD_CLKIN -> LCD_CLK_RETURN AND NET LCD_CLKOUT -> LCD_DCLK

REVISIONS A->B:

1. CHANGED DIRECTION OF NETS LCD_CLKIN AND LCD_CLKOUT

2. CHANGED THE NAMES OF THE LCD DATA LINES

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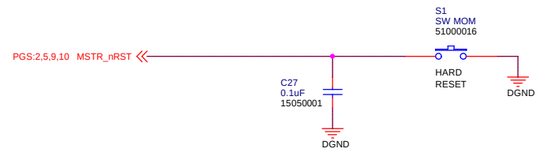
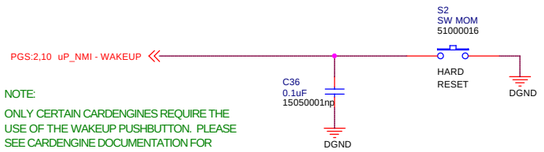
08 - POWER

MASTER RESET



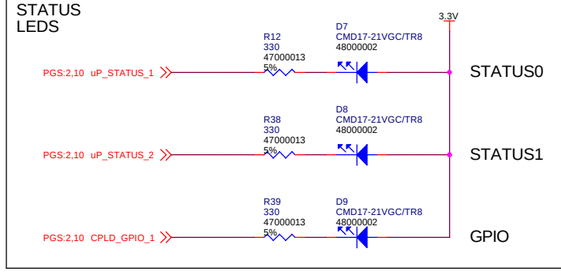
NMI - WAKEUP



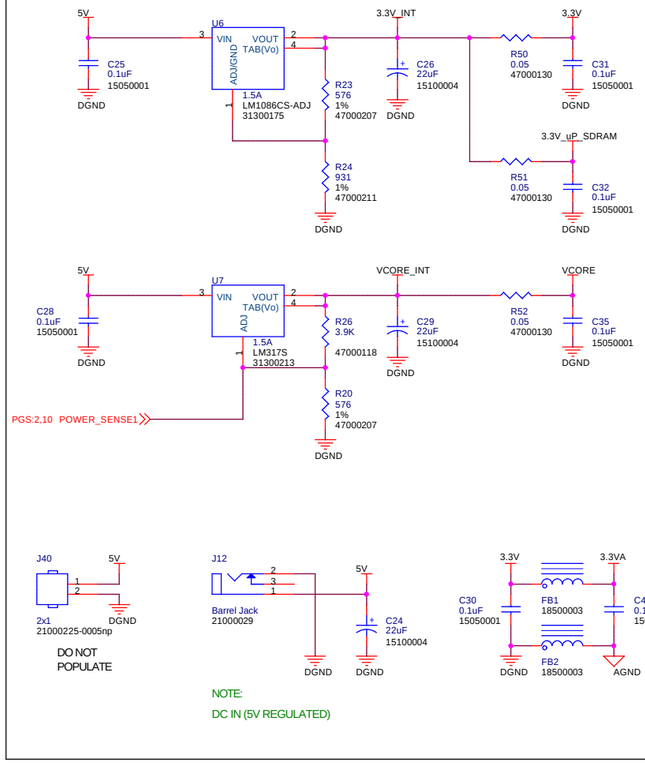
NOTE:

ONLY CERTAIN CARDENGINES REQUIRE THE USE OF THE WAKEUP PUSHBUTTON. PLEASE SEE CARDENGINE DOCUMENTATION FOR DETAILS

STATUS LEDS



POWER



NOTE:

DC IN (5V REGULATED)

REVISIONS E->F:

1. CHANGED J40 FROM BL_VCC TO 5V AND GND
2. MADE C36 A NO POP

REVISIONS D->E:

1. ADDED THE CIRCUIT NMI - WAKEUP AND CHANGED NET uP_NMI TO uP_NMI - WAKEUP

REVISIONS B->C:

1. CHANGED J40 FROM POPULATE TO DO NOT POPULATE
2. SEPARATED THE 3.3V AND 3.3V_uP_SDRAM
3. ADD SENSE RESISTORS AND .1uF CAPS TO THE 3 PLANES VCORE, 3.3V, AND 3.3V_uP_SDRAM
4. CHANGED NET NAMES TO FOLLOW NEW NAMING CONVENTION SHOWING ACTIVE LEVEL IE. MSTR_RST -> MSTR_nRST.
5. CHANGED REF DES J40np TO J40

REVISIONS A->B:

1. CHANGED THE NETS THAT CONTROL THE LED'S FROM MFP11, MFP12, MFP4 TO uP_STATUS1, uP_STATUS2, CPLD_GPIO1
2. CHANGED U6 TO AN LDO REGULATOR

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09 - SH AND ARM JTAGS

SH JTAG

ARM JTAG

ENGINE CPLD

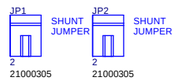
DO NOT
POPULATE

J6 JUMPER SETTINGS FOR NORMAL OPERATION

ENGINE TYPE	J6.1.3.5 uP_TEST2	J6.2.4.6 uP_TEST1	LPD PART NUMBER
LH79520	NO POP	NO POP	80000113
LH75401	NO POP	NO POP	80000132 80000227
LH7A400	NO POP	NO POP	80000126
LH7A404	NO POP	NO POP	80000127
RENESAS	NO POP	NO POP	80000114 80000117 80000115

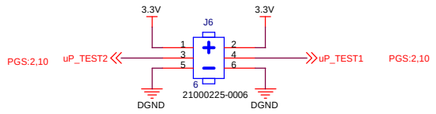
J6 JUMPER SETTINGS FOR JTAG OPERATION

ENGINE TYPE	J6.1.3.5 uP_TEST2	J6.2.4.6 uP_TEST1	LPD PART NUMBER
LH79520	+	-	80000113
LH75401	+	-	80000132 80000227
LH7A400	+	-	80000126
LH7A404	+	-	80000127
RENESAS	+	-	80000114 80000117 80000115



NOTE:

SEE QUICK START GUIDE OR HARDWARE SPEC FOR PICTORAL ILLUSTRATING PROPER JUMPER SETTINGS



REVISIONS F->G:

1. UPDATED JUMPER TABLE FOR NORMAL OPERATION TO INDICATE THAT THE JUMPERS SHOULD BE NOT POPULATED
2. REMOVED NOTE REGARDING 75401, RTCK AND WIGGLER EMULATOR

REVISIONS D->F:

1. REMOVED uP_TEST1 FROM J15.8 AND CONNECTED TO J15.10, GROUNDED J15.8
2. MOVED JUMPER BLOCK J6 OFF OF CIRCUIT FOR J15 FOR CLARITY

REVISIONS C->D:

1. CHANGED STYLE OF JUMPER SETTINGS TABLE AND CORRECTED THE SETTINGS FOR THE LH75401
2. CORRECTED THE SETTINGS FOR THE LH7A400

REVISIONS B->C:

1. CHANGED J6.5, J6.6 TO GND AND REMOVED R50
2. REMOVED JTAG PULLUPS FOR THE PROCESSOR R31 - R37 THESE ARE NOW LOCATED ON ALL CARD ENGINES
3. REMOVED JTAG PULLUPS FOR THE CPLD R43 - R46 THESE ARE NOW LOCATED ON ALL CARD ENGINES
4. CHANGED J36 TO A 20PIN CONNECTOR FOR THE ICE STANDARD 20PIN JTAG
5. ADDED SIGNAL uP_RTCK TO MFP38 FROM THE 20PIN JTAG HEADER
6. CHANGED REF DES J41np TO J41

REVISIONS A->B:

1. CHANGED R34 TO A CONFIG RESISTOR. THIS WILL ALLOW THE SHARP ENGINE TO SWITCH BETWEEN JTAG MODE AND NORMAL MODES OF OPERATION.
2. DELETED CONFIGURATION RESISTORS R34, R37 AND ADDED A JUMPER BLOCK TO SWITCH BETWEEN JTAG MODE AND NORMAL MODE.

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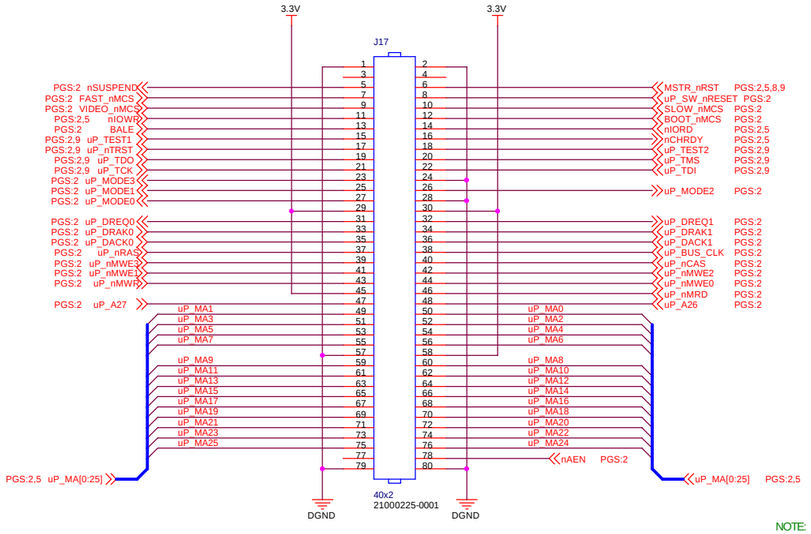
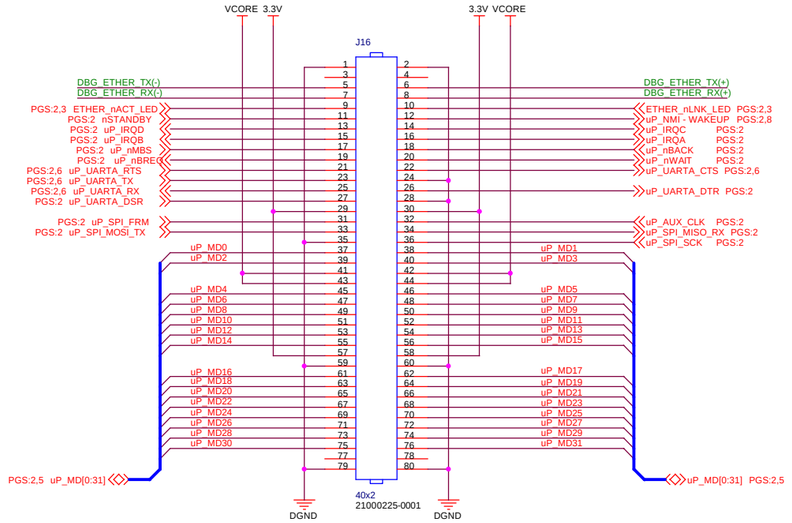
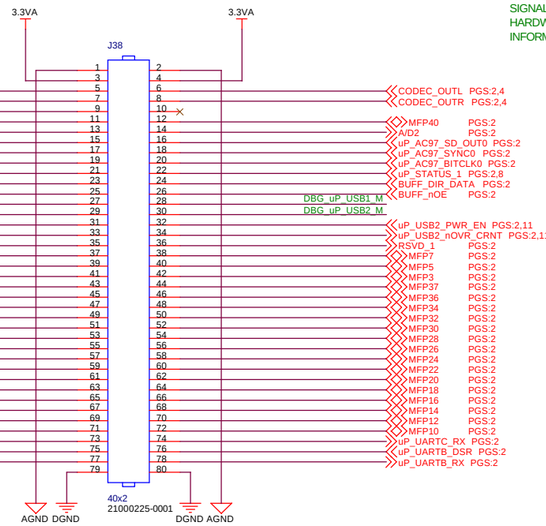
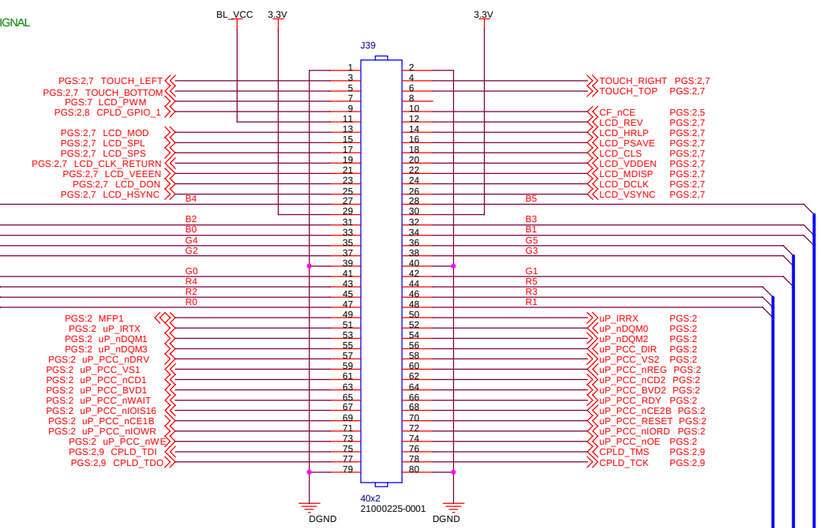
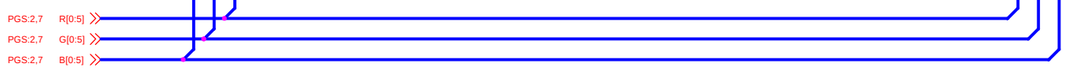
10 - EXPANSION/DEBUG HEADERS











NOTE:

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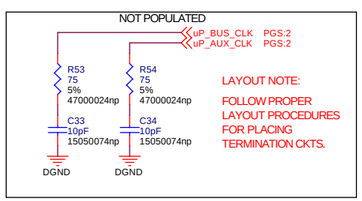
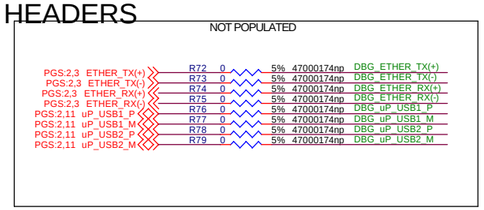
TERMINATIONS



LAYOUT NOTE:

FOLLOW PROPER LAYOUT PROCEDURES FOR PLACING TERMINATION CKTS.

DIFF PAIRS TO DEBUG HEADERS



NOTE:

THE SDK SHIPS STANDARD WITH THESE RESISTORS NOT POPULATED TO MAKE THE CONNECTION FROM THE CARD ENGINE TO THE EXPANSION HEADERS, POPULATE R72 - R79.

REVISIONS C->D:

1. CHANGED NETS
A39 - TOUCH_TOP (was TOUCHX2)
A38 - TOUCH_BOTTOM (was TOUCHX)
A37 - TOUCH_RIGHT (was TOUCHY2)
A36 - TOUCH_LEFT (was TOUCHY)
2. REMOVED THE NET CF_RDYnBSY AND RENAMED THE NET RSVD_1

REVISIONS D->E:

1. CHANGED NET NAME OF uP_NMI (J16.12) TO uP_NMI - WAKEUP TO ACCOMODATE THE a400 AND A404.

REVISIONS E->F:

1. ADDED R72 - R79 TO SEPARATE DIFF PAIRS FROM EXPANSIONHEADERS

REVISIONS B->C:

1. ADDED TERMINATIONS TO uP_AUX_CLK AND uP_BUS_CLK

2. CHANGED NET NAMES TO FOLLOW NEW NAMING CONVENTION SHOWING ACTIVE LEVEL IE. MSTR_RST -> MSTR_nRST.

3. RENAMED NET LCD_CLKIN -> LCD_CLK_RETURN AND NET LCD_CLKOUT -> LCD_DCLK

4. SWITCHED THE PINS ON J39 THAT NETS LCD_PSAVE AND LCE_REV GO TO

5. CHANGED REF DES OF R53np, R54np, C33np, C34np TO R53, R54, C33, C34

REVISIONS A->B:

1. CHANGED THE NAMES OF THE LCD DATA LINES

2. CHANGED THE NET NAMES OF EVB1 AND EVB2 TO CF_nCE AND CF_BSYnRDY RESPECTIVELY

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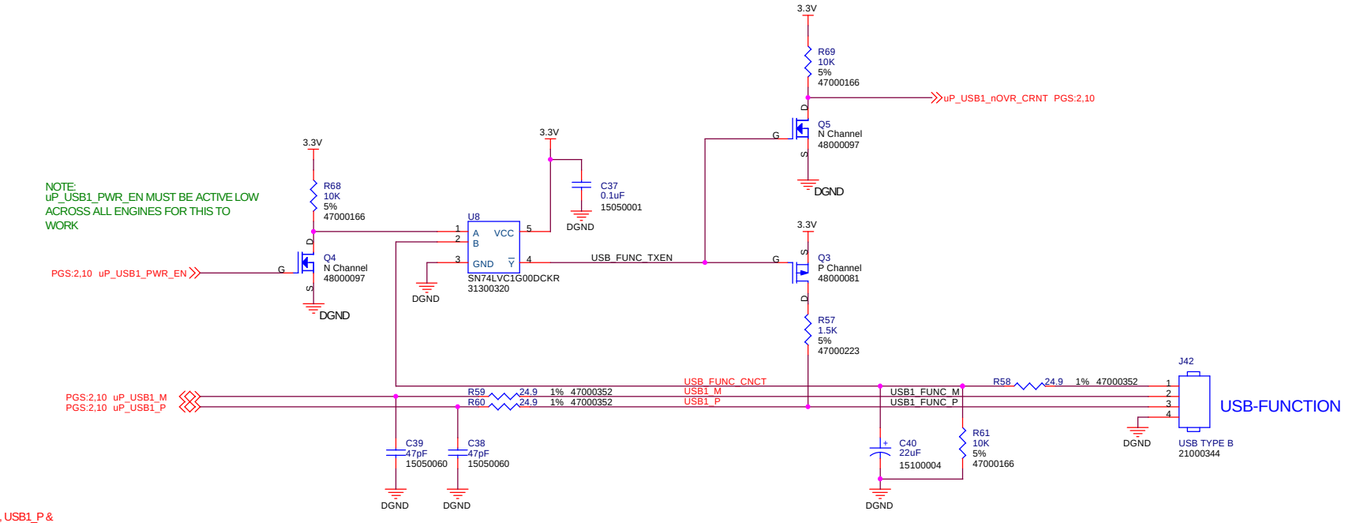
11 - USB HOST/FUNCTION



REVISIONS D->E:

1. ADDED USB HOST AND USB FUNCTION TO DESIGN.

REVISIONS E->F:

1. ADDED USB HOST IMPEDENCE MATCHING DISCRETES TO USB2_M AND USB2_P.
2. CHANGED THE IMPEDENCE MATCHING DISCRETES ON USB FUNCTION TO THE CORRECT CONFIGURATION AND VALUES
3. ADDED LOGIC TO PROPERLY IMPLEMENT USB FUNCTION ACROSS ALL CARD ENGINES. CHANGED THE HOST POWER CONTROLLER TO THE "-1" DEVICE WHICH IS ACTIVE HIGH INSTEAD OF ACTIVE LOW

Schematic Modify Date = Friday, April 16, 2004

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12 - ECO LIST

Revision Control			
ECO Number	Rev	Description of Change	Date
	A	RELEASE FOR PILOT RUN	11/14/02
LCE-APP-10-001		1. CHANGED THE NET NAMES OF THE LCD DATA LINES. PG2,7,10	
LCE-APP-10-002		2. CHANGED THE NET NAMES OF EVB1 AND EVB2 TO CF_nCE AND CF_BSYnRDY RESPECTIVELY. PG2,5	
LCE-APP-10-003		3. REMOVED NET uP_MA0 AND TIED THAT PIN ON J7 TO GND. PG5	
LCE-APP-10-004		4. REMOVED HOT SWAPPABILITY OF CF CARD. DELETED NETS uP_PCCDRV AND CF_3.3V, AND COMPONENTS Q1, C10. PG5	
LCE-APP-10-005		5. ADDED ADDRESS LINES uP_MA3-9 AND uP_MA11 FOR GREATER FUNCTIONALITY AND USABILITY OF MORE CF CARDS. PG5	
LCE-APP-10-006		6. CHANGED THE NETS THAT CONTROL THE LED'S FROM MFP11, MFP12, MFP4 TO uP_STATUS1, uP_STATUS2, CPLD_GPIO1. PG8,2,10	
LCE-APP-10-007		7. CHANGED R34 TO A CONFIG RESISTOR. PG9	
LCE-APP-10-008		8. REPLACED CONFIGURATION RESISTORS R34, R37 W/JUMPER BLOCK TO SWITCH BETWEEN JTAG MODE AND NORMAL MODE. PG9	
LCE-APP-10-009		9. CHANGED U6 TO AN LDO REGULATOR	
	B	RELEASE FOR PRODUCTION	1/6/03
LCE-APP-10-010		10. CHANGED NET THAT CONNECTS TO REG ON J7.44 FROM uP_MA11 TO uP_MA13	2/7/03
LCE-APP-10-011		11. CHANGED J40 FROM POPULATE TO DO NOT POPULATE	2/7/03
LCE-APP-10-012		12. SEPARATED THE 3.3V AND 3.3V_uP_SDRAM ON PINS 61-64 OF THE SODIMM CON	2/7/03
LCE-APP-10-013		13. CHANGED THE IMPEDENCE MATCHING VOLTAGE ON THE ENET TX AND RX LINES TO 3.3V_WRLAN	2/10/03
LCE-APP-10-014		14. ADDED 3.3V_WRLAN TO THE DIMM CONNECTOR J1C.19	2/10/03
LCE-APP-10-015		15. CHANGED THE 60PIN LCD CONNECTOR J11 TO A SHROUDED/KEYEDW EJECTOR TABS TYPE	2/10/03
LCE-APP-10-016		16. ADDED TERMINATIONS TO uP_AUX_CLK AND uP_BUS_CLK, AND DO NOT POPULATE	2/10/03
LCE-APP-10-017		17. CHANGED J6.5, J6.6 TO GND AND REMOVE R50	2/10/03
LCE-APP-10-018		18. REMOVED JTAG PULLUPS FOR THE PROCESSOR R31 - R37 THESE ARE NOW LOCATED ON ALL CARD ENGINES	2/10/03
LCE-APP-10-019		19. REMOVED JTAG PULLUPS FOR THE CPLD R43 - R46 THESE ARE NOW LOCATED ON ALL CARD ENGINES	2/10/03
LCE-APP-10-020		20. CHANGED J36 TO A 20PIN CONNECTOR FOR THE ICE STANDARD 20PIN JTAG	2/25/03
LCE-APP-10-021		21. ADD SENSE RESISTORS AND .1uF CAPS TO THE 3 PLANES VCORE, 3.3V, AND 3.3V_uP_SDRAM	2/25/03
LCE-APP-10-022		22. CHANGED NET NAMES TO FOLLOW NEW NAMING CONVENTION SHOWING ACTIVE LEVEL IE. MSTR_RST -> MSTR_nRST.	2/25/03
LCE-APP-10-023		23. CHANGED THE NET NAMES OF THE LNK AND ACT LED NETS TO ETHER_nACT_LED AND ETHER_nLNK_LED	2/25/03
LCE-APP-10-024		24. CHANGED R3 AND R4 FROM 47 OHM 5%'S TO 49.9 OHM 1%'S	2/25/03
LCE-APP-10-025		25. GROUNDED PINS 4 AND 5 OF P1, PER PULSE CONNECTOR SPEC	2/25/03
LCE-APP-10-026		26. CHANGED R1,R2,R5,R6 FROM 24 OHM 5%'S TO 24.9 OHM 1%'S	2/25/03
LCE-APP-10-027		27. ADDED SIGNAL uP_RTCK TO MFP38 FROM THE 20PIN JTAG HEADER	2/26/03
LCE-APP-10-028		28. REMOVED PULLUP ON CF_RDYnBSY	2/26/03
LCE-APP-10-029		29. IMPLEMENTED CONVERSION TO NEW NET NAMING CONVENTION****	2/26/03
LCE-APP-10-030		30. SWITCHED THE PINS ON J1A THAT NETS LCD_PSAVE AND LCE_REV GO TO	3/05/03
LCE-APP-10-031		31. RENAMED NET LCD_CLKIN -> LCD_CLK_RETURN AND NET LCD_CLKOUT -> LCD_DCLK	3/05/03
LCE-APP-10-032		32. CHANGED REMOVED THE np SUFFIX ON ALL NO POP PARTS AND ADDED A FIELD TO INDICATE THIS IN THE BOM.	3/05/03
LCE-APP-10-033		33. REMOVED R22	3/05/03
	C	RELEASE FOR PROTO RUN	3/05/03
LCE-APP-10-034		34. CHANGED NET THAT CONNECTS TO REG ON J7.44 FROM uP_MA13 TO uP_MA12	3/12/03
LCE-APP-10-035		35. CHANGED STYLE OF JUMPER SETTINGS TABLE AND CORRECTED THE SETTINGS FOR THE LH75401	3/26/03
LCE-APP-10-036		36. CHANGED NETS A39 - TOUCH_TOP (was TOUCHX2), A38 - TOUCH_BOTTOM (was TOUCHX), A37 - TOUCH_RIGHT (was TOUCHY2), A36 - TOUCH_LEFT (was TOUCHY)	3/26/03
LCE-APP-10-037		37. REMOVED THE NET CF_RDYnBSY FROM J7.37 AND RENAMED THIS NET RSVD_1 ON THE EXPANSION HEADERS AND EXPANSIONS BUS	3/29/03
	D	RELEASE FOR PRODUCTION	4/10/03
LCE-APP-10-038		38. CORRECTED THE JUMPER SETTINGS IN THE JTAG TABLE FOR THE LH7A400	4/28/03
LCE-APP-10-039		39. ADDED THE CIRCUIT WAKEUP CONTAINING PARTS: C? AND S?	5/13/03
LCE-APP-10-040		40. ADDED USB HOST AND FUNCTION CIRCUITRY	5/25/03
	E	RELEASE FOR PRODUCTION	5/29/03

Revision Control			
ECO Number	Rev	Description of Change	Date
LCE-APP-10-041		41. ADDED USB HOST IMPEDENCE MATCHING DISCRETES TO USB2_M AND USB2_P.	7/14/03
LCE-APP-10-042a		42a. ADDED LOGIC TO PROPERLY IMPLEMENT USB FUNCTION ACROSS ALL CARD ENGINES.	7/14/03
LCE-APP-10-042b		42b. CHANGED THE HOST POWER CONTROLLER TO THE "-1" DEVICE WHICH IS ACTIVE HIGH INSTEAD OF ACTIVE LOW	7/14/03
LCE-APP-10-043		43. ADDED R72 - R79 TO SEPARATE DIFF PAIRS FROM EXPANSIONHEADERS	7/21/03
LCE-APP-10-044		44. REMOVED uP_TEST1 FROM J15.8 AND CONNECTED TO J15.10, GROUNDED J15.8	7/24/03
LCE-APP-10-045		45. MOVED JUMPER BLOCK J6 OFF OF CIRCUIT FOR J15 FOR CLARITY	7/24/03
LCE-APP-10-046		46. SUBMITTED PART FOR LCE-APP-10 AND UPDATED BLOCK DIAGRAM AND TITLE PAGE	7/24/03
LCE-APP-10-047		47. CHANGED J40 FROM BL_VCC AND GND TO 5V AND GND	7/24/03
LCE-APP-10-048		48. CONNECTED CT1 TO 3.3V_WRLAN PER 91C111 SCHEMATIC CHECKLIST PROVIDED BY SMSC	7/25/03
LCE-APP-10-049		49. CHANGED THE CONNECTION OF CT1 TO 3.3V_WRLAN DIRECTLY TO ONE THAT USES A 0OHM (R80) UNTIL QA HAS BEEN COMPLETED.	7/28/03
LCE-APP-10-050		50. MADE C36 A NO POP	8/15/03
	F	RELEASE FOR PRODUCTION	8/15/03
LCE-APP-10-051		51. ADDED BOX AROUND THE NO POP RESISTOR ON ENET CONNECTOR	4/16/04
LCE-APP-10-052		52. REMOVED A0 FROM CF CONNECTOR FOR COMPATABILITY WITH A400 BSC IN A 16BIT AREA	4/16/04
LCE-APP-10-053		53. UPDATED JUMPER TABLE FOR NORMAL OPERATION TO INDICATE THAT THE JUMPERS SHOULD BE NOT POPULATED	4/16/04
LCE-APP-10-054		54. REMOVED NOTE REGARDING 75401, RTCK AND WIGGLER EMULATOR	4/16/04
READY FOR RELEASE			

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