01 - TITLE PAGE

Project:	EPS
Part Number:	80000258
Assembly Name:	LH7A404-11
Schematics	ECR

TABLE OF CONTENTS

PAGE	DESCRIPTION
1	TITLE PAGE AND BLOCK DIAGRAM
2	CONNECTORS
3	BUFFERS
4	SDRAM
5	FLASH
6	WIRED LAN
7	CPLD
8	PERIPHERAL CIRCUITS
9	CODEC
10	PROCESSOR
11	TEST POINTS

COLOR LEGEND

NOTE:
NOTES IN GREEN TEXT ARE GENERAL DESIGN OR SCHEMATIC NOTES

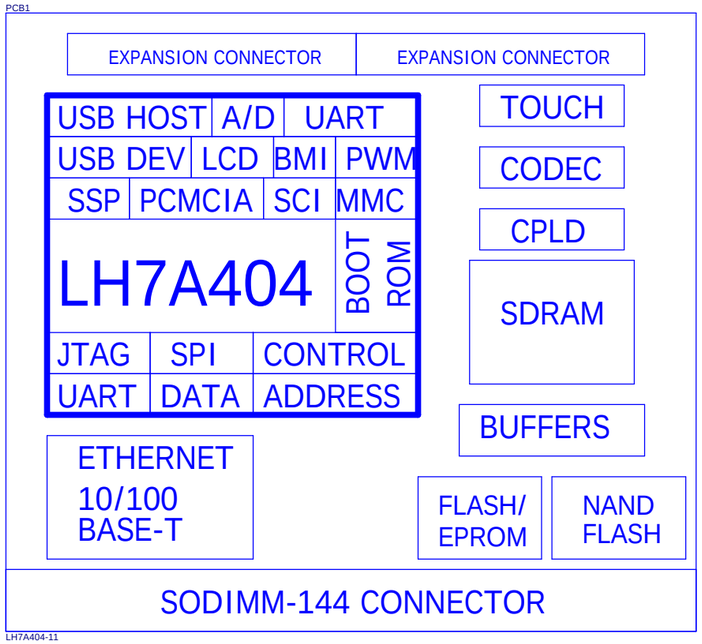
LAYOUT NOTE:
NOTES IN RED TEXT ARE PCB LAYOUT RECOMMENDATIONS OR GUIDLINES

NET NAMES

NET NAMES IN GREEN TEXT ARE NETS THAT ARE NOT DIRECTLY CONNECTED WITH A VISIBLE WIRE ON SINGLE SCHEMATIC PAGE, BUT USE THIS CONVENTION TO MAKE THE SCHEMATIC EASIER TO READ

NET NOTE

NET NOTES IN BLACK TEXT INDICATE A PARTICULAR FUNCTIONALITY OF A SPECIFIC NET, IT IS NOT A NET NAME MERELY TEXT AND HAS NO AFFECT ON THE DRC.

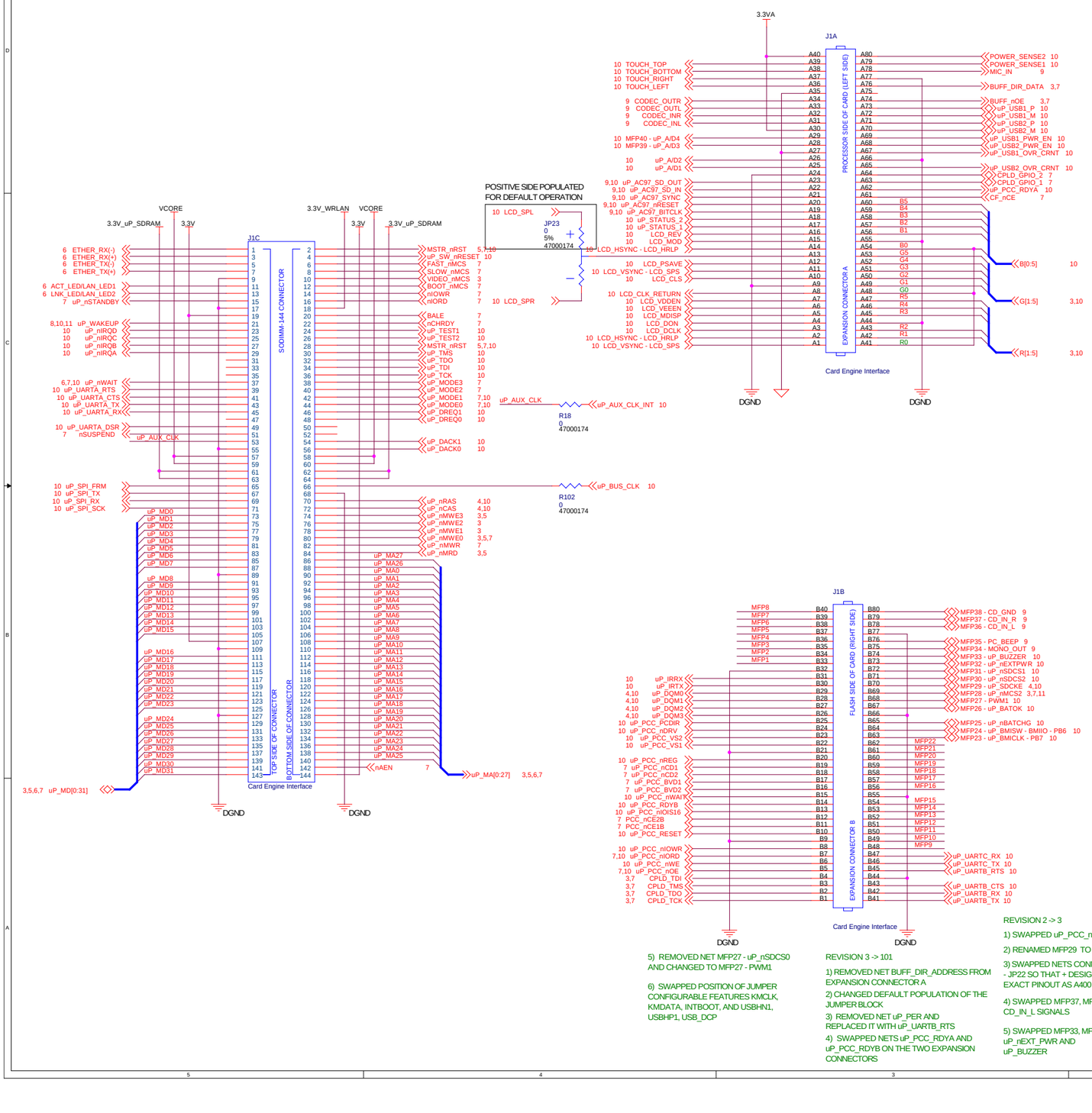


Schematic Modify Date = Monday, June 28, 2004

LOGIC
PRODUCT DEVELOPMENT
411 WASHINGTON AVE. N
MINNEAPOLIS, MN 55401
PHONE: (612) 672-9495
FAX: (612) 672-9489

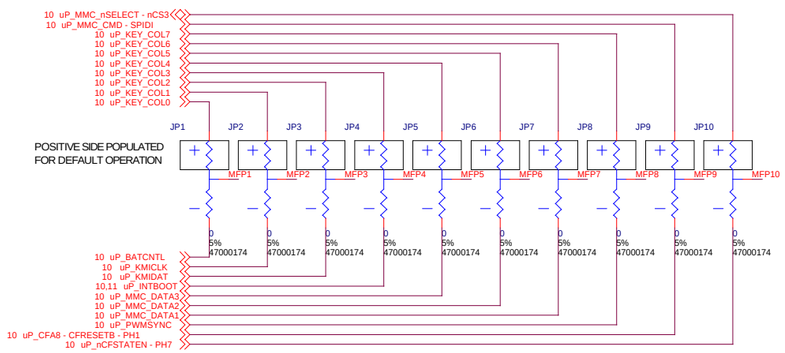
Title LH7A404-11 Card Engine		
Size C	Number 80000258	Rev 201
Design Create Date = Friday, October 18, 2002	Project LH7A404-11	Sheet 1 Of 12

02 - EXPANSION BUS



RGB TO LCD DATA LINE

BLUE5	LCD_D14
BLUE4	LCD_D13
BLUE3	LCD_D12
BLUE2	LCD_D11
BLUE1	LCD_D10
BLUE0	LCD_D15
GREEN5	LCD_D9
GREEN4	LCD_D8
GREEN3	LCD_D7
GREEN2	LCD_D6
GREEN1	LCD_D5
GREEN0	LCD_D15
RED5	LCD_D4
RED4	LCD_D3
RED3	LCD_D2
RED2	LCD_D1
RED1	LCD_D0
RED0	LCD_D15



REVISION 2 -> 3

1) SWAPPED uP_PCC_nCE1/2A AND uP_PCC_nCE1/2B

2) RENAMED MFP29 TO MFP29 - uP_SDCKE

3) SWAPPED NETS CONNECTED TO EACH END OF JP11 - JP22 SO THAT + DESIGNATIONS WILL PROVIDE FOR EXACT PINOUT AS A400 CARD ENGINE

4) SWAPPED MFP37, MFP36 – CD_IN_R and CD_IN_L SIGNALS

5) SWAPPED MFP33, MFP32 – uP_nEXT_PWR AND uP_BUZZER

REVISION 3 -> 101

1) REMOVED NET BUFF_DIR_ADDRESS FROM EXPANSION CONNECTOR A

2) CHANGED DEFAULT POPULATION OF THE JUMPER BLOCK

3) REMOVED NET uP_PER AND REPLACED IT WITH uP_UARTB_RTS

4) SWAPPED NETS uP_PCC_RDYA AND uP_PCC_RDYB ON THE TWO EXPANSION CONNECTORS

5) REMOVED NET MFP27 - uP_nSDCS0 AND CHANGED TO MFP27 - PWM1

6) SWAPPED POSITION OF JUMPER CONFIGURABLE FEATURES KMCLK, KMDATA, INTBOOT, AND USBHN1, USBHP1, USB_DCP

REVISION 1 -> 2

1) CHANGED uP_IRQE TO uP_WAKEUP ON J1C

2) SWAPPED LCD_REV AND LCD_PSAVE SIGNALS

3) RENAMED TOUCH NETS

4) RENAMED uP_USB_DN, uP_USB_DP TO uP_USB_HN1, uP_USB_HP1 TO COINCIDE WITH USB ARCHITECTURE CHANGE FOR SDK BOARD

5) CHANGED uP_PCC_nCE2 TO uP_PCC_nCE2A, uP_PCC_nCE1 TO uP_PCC_nCE1A

6) REMOVED PWM SIGNALS AND REPLACED THEM WITH uP_PCC_nCE1B AND uP_PCC_nCE2B FOR DUAL PC CARD SUPPORT

7) MOVED uP_PWMSYNC, uP_INTBOOT TO MFPs

8) REMOVED C37, C79

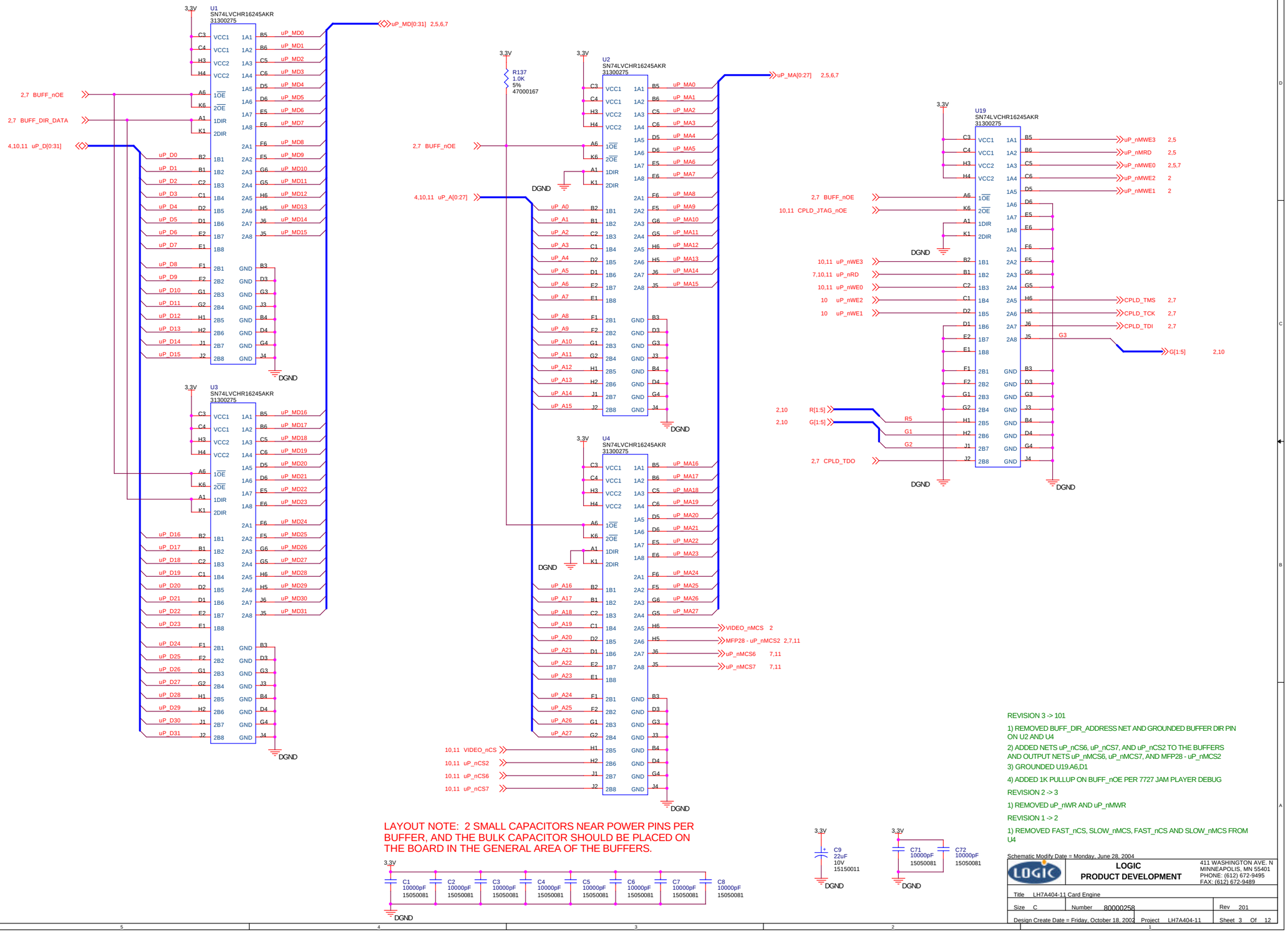
Schematic Modify Date = Monday, June 28, 2004

LOGIC PRODUCT DEVELOPMENT

411 WASHINGTON AVE. N
MINNEAPOLIS, MN 55401
PHONE: (612) 672-9495
FAX: (612) 672-9489

Title	LH7A404-11 Card Engine		
Size	Custom	Number 80000258	Rev 201
Design Create Date = Friday, October 18, 2002	Project LH7A404-11		Sheet 2 Of 12

03 - BUFFERS



REVISION 3 -> 101

1) REMOVED BUFF_DIR_ADDRESS NET AND GROUNDED BUFFER DIR PIN ON U2 AND U4

2) ADDED NETS uP_nCS6, uP_nCS7, AND uP_nCS2 TO THE BUFFERS AND OUTPUT NETS uP_nMCS6, uP_nMCS7, AND MFP28 - uP_nMCS2

3) GROUNDED U19.A6,D1

4) ADDED 1K PULLUP ON BUFF_nOE PER 7727 JAM PLAYER DEBUG

REVISION 2 -> 3

1) REMOVED uP_nWR AND uP_nMWR

REVISION 1 -> 2

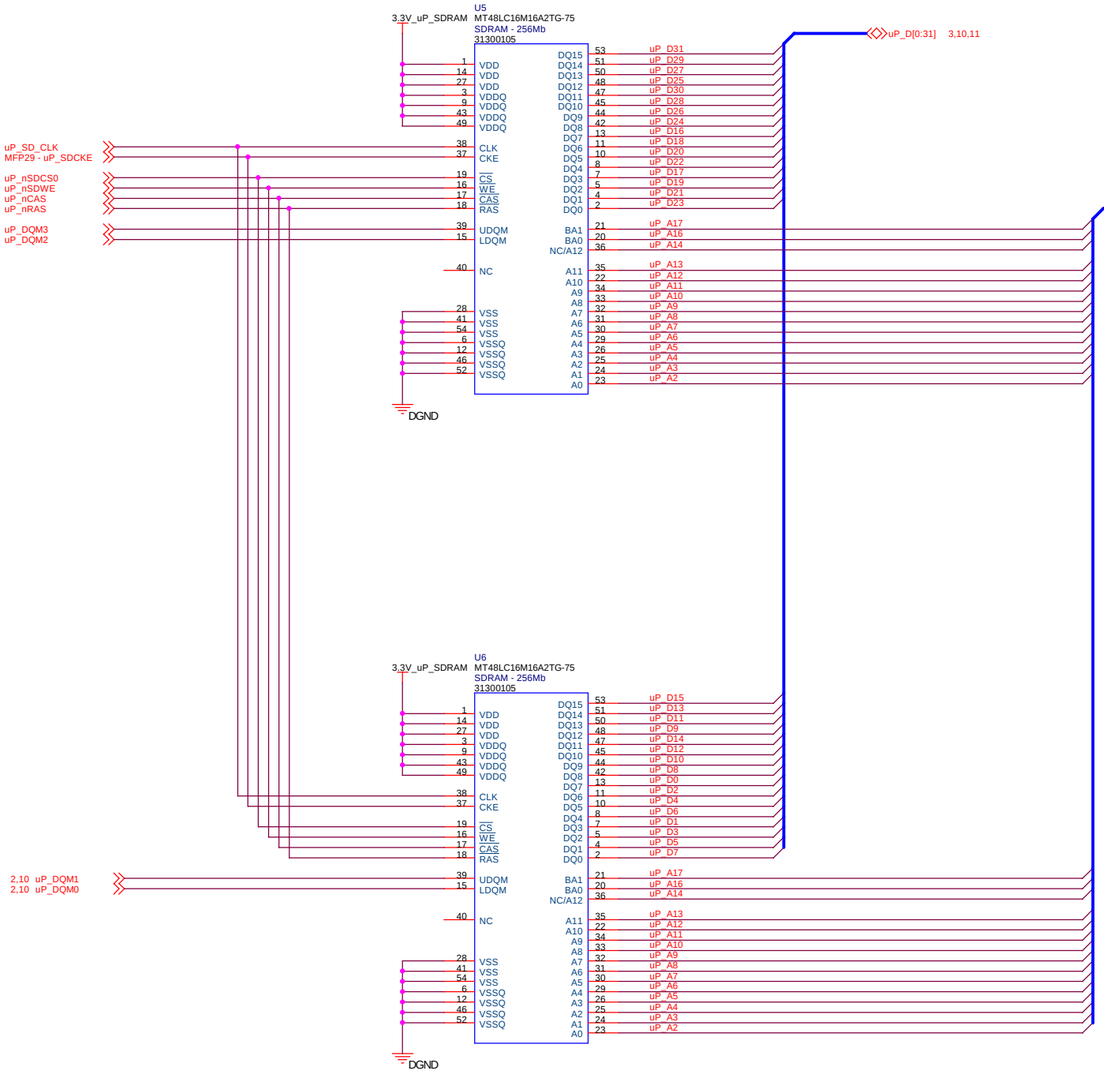
1) REMOVED FAST_nCS, SLOW_nMCS, FAST_nCS AND SLOW_nMCS FROM U4

Schematic Modify Date = Monday, June 28, 2004

LOGIC
PRODUCT DEVELOPMENT
411 WASHINGTON AVE. N
MINNEAPOLIS, MN 55401
PHONE: (612) 672-9495
FAX: (612) 672-9489

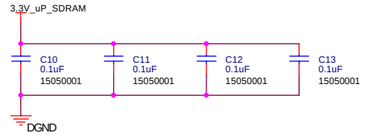
Title	LH7A404-11 Card Engine		
Size C	Number 80000258		Rev 201
Design Create Date = Friday, October 18, 2002	Project LH7A404-11		Sheet 3 Of 12

04 - SDRAM



ENGINE DENSITY	CONFIG	PART #
16 MByte		MT48LC4M16A2TG-75
32 MByte		MT48LC8M16A2TG-75
64 MByte	STANDARD	MT48LC16M16A2TG-75

LAYOUT NOTE: TWO .1uF DECOUPLING CAPS PER CHIP, TWO BULK CAPS TO BE PLACE IN THE GENERAL AREA OF THE SDRAM ON PCB.



REVISION 3 -> 101

1) CHANGED STANDARD SDRAM POPULATION TO 64MB

REVISION 2 -> 3

1) RENAMED uP_SDCKE TO MFP29 - uP_SDCKE

Schematic Modify Date = Monday, June 28, 2004

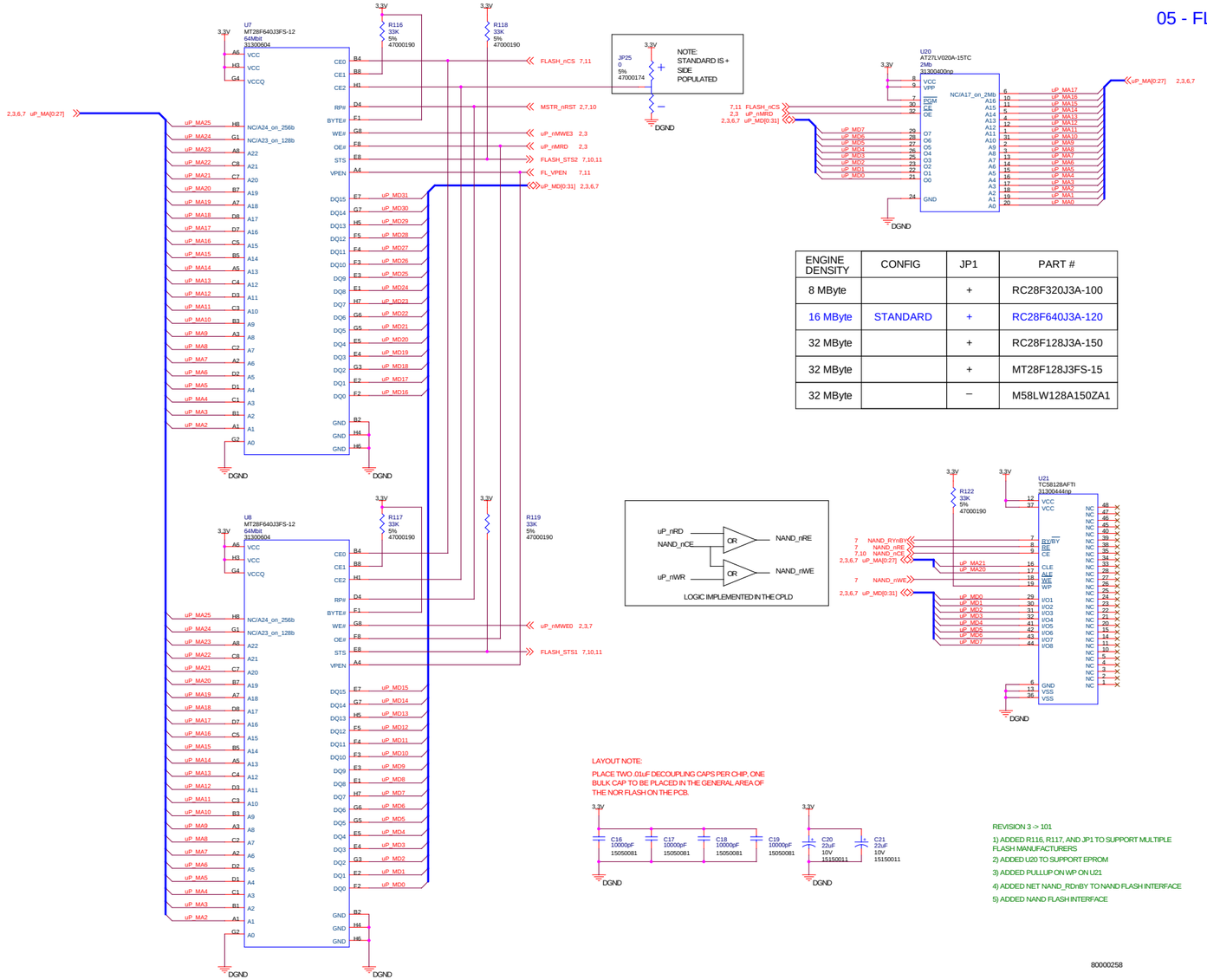
LOGIC
PRODUCT DEVELOPMENT
411 WASHINGTON AVE. N
MINNEAPOLIS, MN 55401
PHONE: (612) 672-9495
FAX: (612) 672-9489

Title LH7A404-11 Card Engine

Size C | Number 80000258 | Rev 201

Design Create Date = Friday, October 18, 2002 | Project LH7A404-11 | Sheet 4 Of 12

05 - FLASH



ENGINE DENSITY	CONFIG	JP1	PART #
8 MByte		+	RC28F320J3A-100
16 MByte	STANDARD	+	RC28F640J3A-120
32 MByte		+	RC28F128J3A-150
32 MByte		+	MT28F128J3FS-15
32 MByte		–	M58LW128A150ZA1

LAYOUT NOTE:

PLACE TWO .01uF DECOUPLING CAPS PER CHIP, ONE BULK CAP TO BE PLACED IN THE GENERAL AREA OF THE NOR FLASH ON THE PCB.

REVISION 3 -> 101

1) ADDED R116, R117, AND JP1 TO SUPPORT MULTIPLE FLASH MANUFACTURERS

2) ADDED U20 TO SUPPORT EPROM

3) ADDED PULLUP ON WP ON U21

4) ADDED NET NAND_RDnBY TO NAND FLASH INTERFACE

5) ADDED NAND FLASH INTERFACE

80000258

Schematic Modify Date = Monday, June 28, 2004

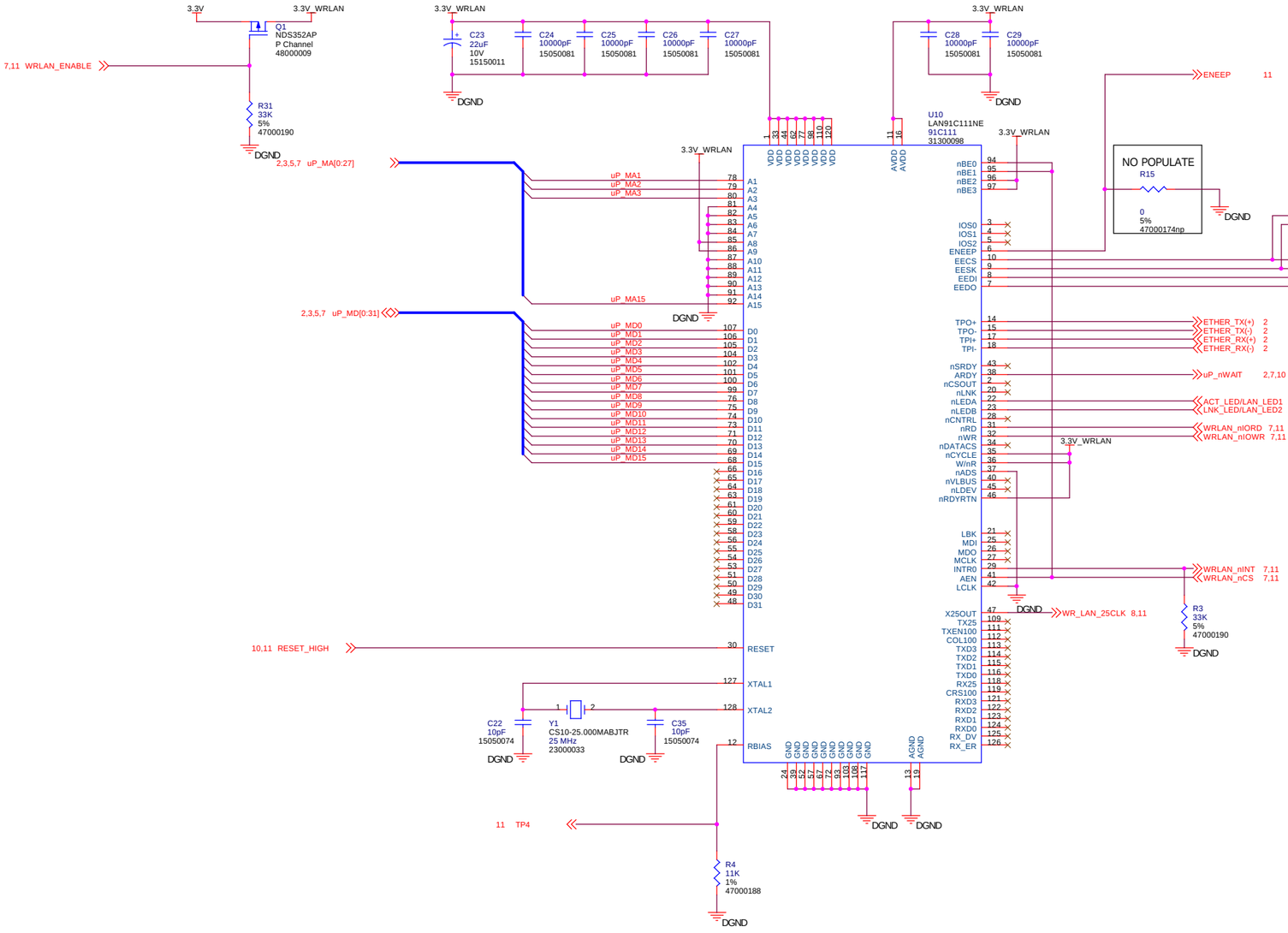
LOGIC
PRODUCT DEVELOPMENT
411 WASHINGTON AVE. N
MINNEAPOLIS, MN 55401
PHONE: (612) 672-9495
FAX: (612) 672-9489

Title LH7A404-11 Card Engine

Size D | Number | Rev 201

Design Create Date = Friday, October 18, 2002 | Project LH7A404-11 | Sheet 5 Of 12

06 - WIRED LAN



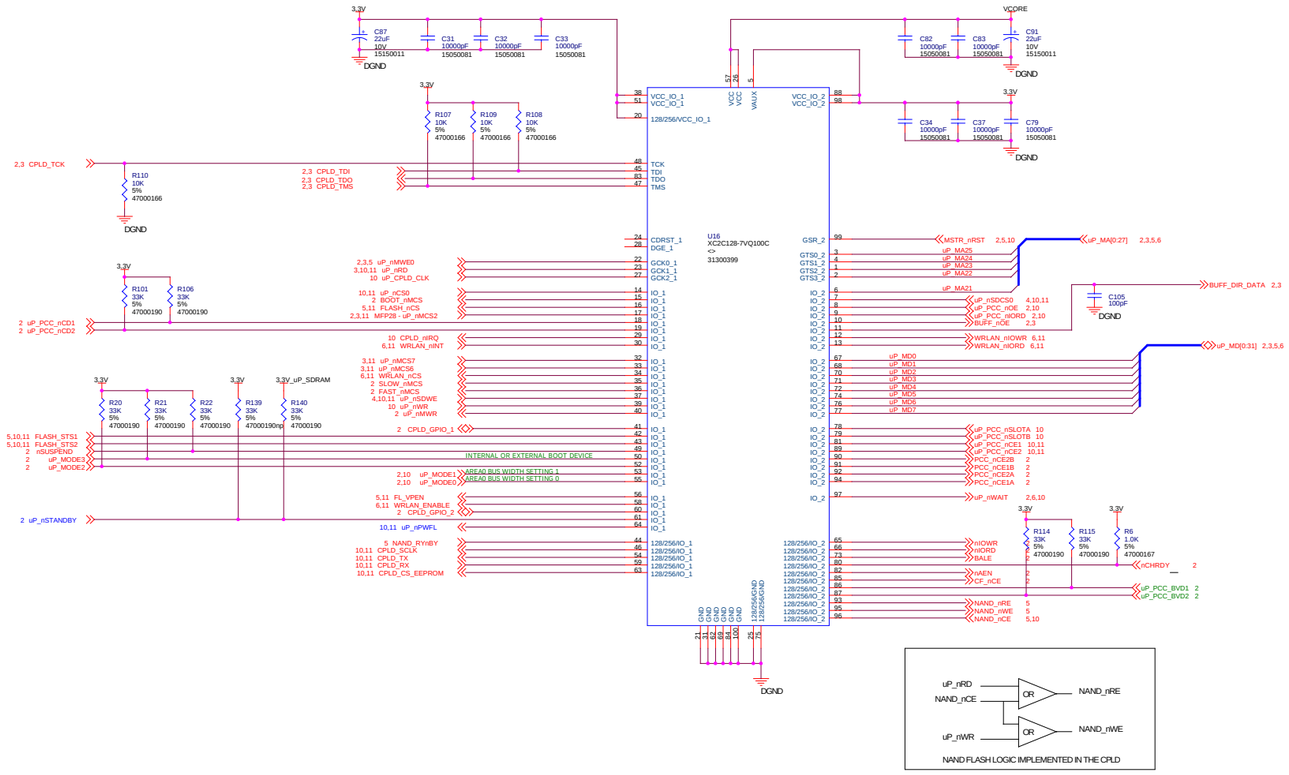
REVISION 1 -> 2

1) CHANGED WR_nWAIT TO uP_nWAIT

Schematic Modify Date = Monday, June 28, 2004

LOGIC PRODUCT DEVELOPMENT		411 WASHINGTON AVE. N MINNEAPOLIS, MN 55401 PHONE: (612) 672-9495 FAX: (612) 672-9489
Title LH7A404-11 Card Engine		
Size C	Number 80000258	Rev 201
Design Create Date = Friday, October 18, 2002 Project LH7A404-11		Sheet 6 Of 12

07 - CPLD



REVISION 101 -> 201

1) CHANGED NET NAME OF CPLD_nCS_EEPROM TO CPLD_CS_EEPROM BECAUSE IT IS ACTIVE HIGH

2) ADDED PULLUP TO NET uP_nSTANDBY, THAT IS SELECTABLE BTWN 3.3V AND 3.3V_uP_SDRAM

3) FIXED CPLD JTAG LINES

4) ADDED CAP TO FILTER OUT POSSIBLE GLITCH ON BUFF DIR DATA NET

REVISION 3 -> 101

1) MOVED FROM ALTERA TO XILINX CPLD

2) REMOVED uP_nWE3, BUFF_DIR_ADDRESS, uP_AUX_CLK_INT, MFP30 - uP_nSDCS2, MFP31 - uP_nSDCS1 SIGNALS

3) REMOVED PULLUP ON BUFF_nOE PIN

4) MOVED NETS UP_PCC_BVD1 AND UP_PCC_BVD2 TO THE FPGA AND R114 AND R115

5) ADDED NETS NAND_nRE, NAND_nWE, AND NAND_nCE TO THE FPGA

6) CHANGED NETS uP_nCS6, uP_nCS7, AND uP_nCS2 TO BE BUFFERED INPUTS TO THE CPLD NAMED uP_nMCS6, uP_nMCS7, AND MFP28 - uP_nMCS2

7) ADDED NET NAND_RDnBY FOR NAND FLASH INTERFACE

8) ADDED PULLDOWN TO USB OVERCURRENT SIGNAL

9) REMOVED NETS WRLAN_25, AND uP_WAKEUP, AND ADDED uP_STANDBY AND NEW NET uP_nPWFL

REVISION 2 -> 3

1) MOVED uP_PCC_nCD1 AND uP_PCC_nCD2 FROM PROCESSOR TO CPLD

2) MOVED CPLD_nCS_EEPROM TO NEW PIN ON CPLD

3) REMOVED uP_nIRQE, RENAMED uP_nIRQD TO CPLD_nIRQ

4) ADDED INPUT uP_nWR AND uP_nSDWE TO CREATE uP_nMWR

5) CHANGED uP_nMWR TO AN OUTPUT

6) REMOVED RSVD_1, MFP29 - CPLD_GPIO_3

7) REMOVED R9

8) ADDED R107, R108, R109, R110

REVISION 1 -> 2

1) ADDED R105 PULLUP TO uP_WAKEUP

2) RENAMED CHIP SELECTS AND MADE uP_nCS6 AND uP_nCS7 AS INPUT TO CPLD AND CPLD NOW CREATES FAST_nMCS AND SLOW_nMCS

3) REMOVED uP_PCC_nCE1, uP_PCC_nCE2 FROM THE CPLD, WR_nWAIT, AND EXTRA uP_nRD SIGNAL

4) ADDED uP_nMWR, uP_PCC_nIORD, AND uP_PCC_nOE TO CPLD

5) CHANGED PULL UP R6 TO 1K OHM

6) ADDED PC CARD CE1, CE2, SLOT1, AND SLOT2 SIGNALS TO CREATE SEPERATE CE SIGNALS FOR DUAL PC CARDS A AND B

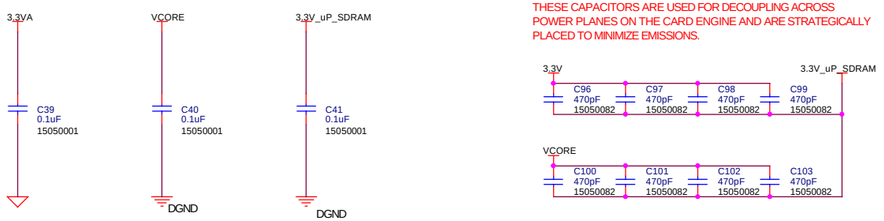
Schematic Modify Date = Monday, June 28, 2004

LOGIC
PRODUCT DEVELOPMENT
411 WASHINGTON AVE. N
MINNEAPOLIS, MN 55401
PHONE: (612) 672-9495
FAX: (612) 672-9469

Title LH7A404-11 Card Engine			
Size D	Number 80000259		Rev 201
Design Create Date = Friday, October 18, 2002	Project LH7A404-11		Sheet 7 Of 12

08 - PERIPHERAL CIRCUITS

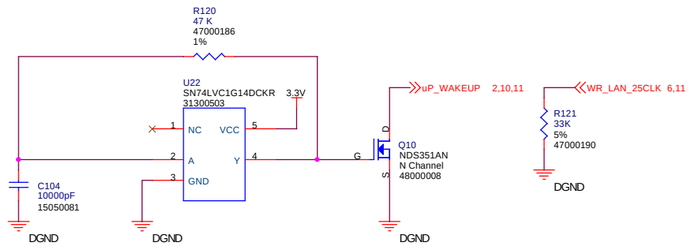
POWER



LAYOUT NOTE:

THESE CAPACITORS ARE USED FOR DECOUPLING ACROSS POWER PLANES ON THE CARD ENGINE AND ARE STRATEGICALLY PLACED TO MINIMIZE EMISSIONS.

AUTOWAKEUP



REVISION 3 -> 101

1) ADDED EMI REDUCING CAPACITORS:C96 - C106

2) ADDED AUTO WAKEUP CIRCUITRY IF U10 NOT POPULATED

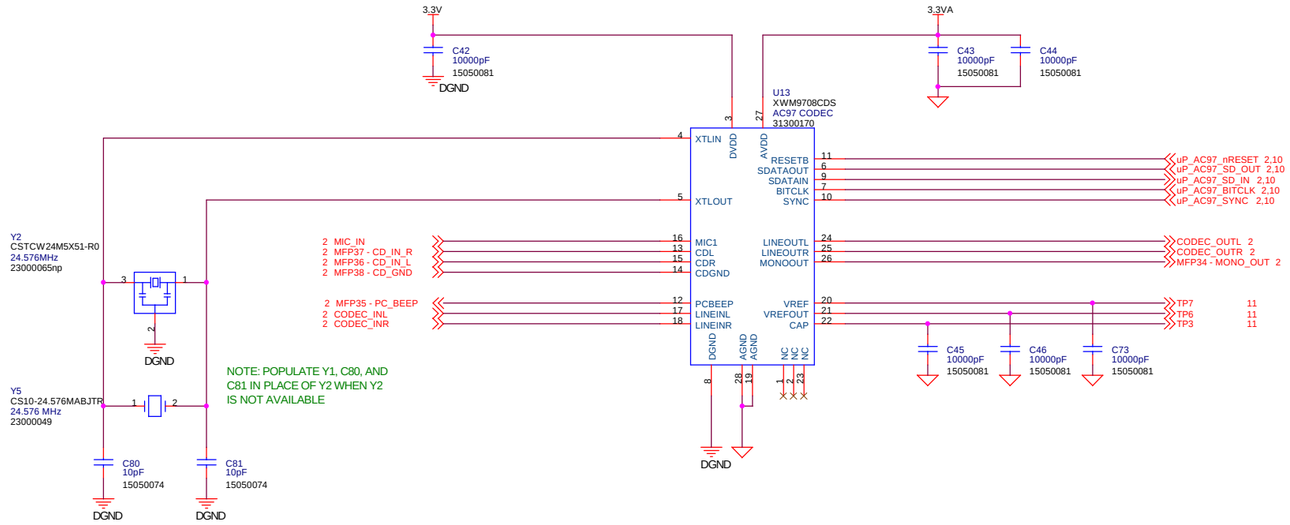
3) MADE AUTO WAKEUP CIRCUITRY TO BE ALWAYS POPULATED

Schematic Modify Date = Monday, June 28, 2004

LOGIC
PRODUCT DEVELOPMENT
411 WASHINGTON AVE. N
MINNEAPOLIS, MN 55401
PHONE: (612) 672-9495
FAX: (612) 672-9489

Title LH7A404-11 Card Engine		
Size C	Number 80000258	Rev 201
Design Create Date = Friday, October 18, 2002	Project LH7A404-11	Sheet 8 Of 12

09 - CODEC



REVISION 1 -> 2

1) ADDED Y5, C80, C81 FOR AN ALTERNATE TO RESONATOR

2) SWAPPED uP_AC97_SD_OUT AND uP_AC97_SD_IN
SIGNALS ON WOLFSON CODEC

Schematic Modify Date = Monday, June 28, 2004

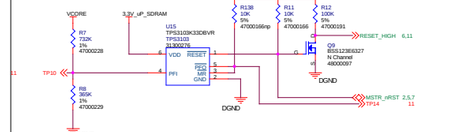
LOGIC
PRODUCT DEVELOPMENT
411 WASHINGTON AVE. N
MINNEAPOLIS, MN 55401
PHONE: (612) 672-9495
FAX: (612) 672-9489

Title LH7A404-11 Card Engine		
Size C	Number 80000258	Rev 201
Design Create Date = Friday, October 18, 2002	Project LH7A404-11	Sheet 9 Of 12

10 - PROCESSOR

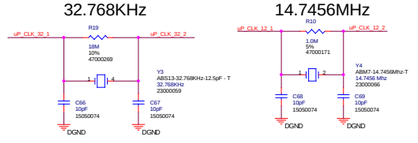
RESET CIRCUIT

NOTE:
SET TO RESET AT 1.63/1-1.67/V



CLOCKS

NOTE: PLACE THE CRYSTAL AND RESONATOR NEXT TO THE PROCESSOR.



POWER SENSE

NOTE: PLACE NEAR PINS 79 AND 80 OF EXPANSION CONNECTOR
A

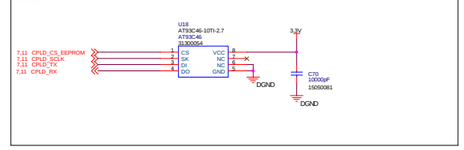
POPULATE ONLY FOR
LOGIC PRODUCT
DEVELOPMENT
INTERFACE BOARDS

R54
2.37K
1%
47002212

VCORE = 1.8V

POWER_SENSE1 2
POWER_SENSE2 2

EEPROM



REVISION 3 -> 101

1) MOVED FROM PBGA TO CABGA PACKAGE

2) REMOVED DOUBLE PULLUP ON MSTR_nRST (R37)

3) ADDED FILTER CAPS TO TOUCH LINES AS NO-POPS

4) REMOVED MOVED NETS UP_PCC_BVD1 AND UP_PCC_BVD2 TO THE FPGA AND R114 AND R115

5) RENAMED NET uP_SCI_MEDCHG TO uP_MEDCHG

6) MOVED NET FLASH_STS1 FROM PC6 TO PA6 TO ENABLE NAND FLASH INTERFACE, ADDED SIGNAL NAND_NOE TO PC6

7) REMOVED NET uP_PER AND REPLACED IT WITH uP_UARTB_RTS

8) ADDED 22 OHM SERIES RESISTORS ON THE SDRAM CONTROL SIGNALS, uP_nSDCD, uP_nRAS, uP_nCAS, uP_nSDWE

9) REMOVED PULLUPS/PULLDOWNS ON uP_SPI_FRM AND uP_SPI_TX, TO MATCH A400, ADDED PULLDOWNS ON uP_UARTA_CTS, AND uP_UARTB_CTS

10) ADDED PULLUP ON RESET CKT ON PFOMR BECAUSE PFO IS AN OPEN DRAIN OUTPUT AND IS CONNECTED TO MR. IS NO POP FOR NOW BECAUSE IT IS CURRENTLY WORKING

11) ADDED NEW NET FROM CPLD: uP_nPWRL

REVISION 2 -> 3

1) MOVED uP_PCC_IOIS16 TO PA2

2) TIED WAIT1 AND WAT2 SIGNALS TOGETHER THROUGH R71

3) TIED VDDA3 TO 3.3V FOR TOUCH CIRCUITRY

4) REMOVED DUPLICATE MSTR_nRST PULLUP R38

5) ADDED R38 TO uP_PCC_RDY2

6) RENAMED uP_nIRQD TO CPLD_nIRQ, RENAMED uP_nIRQE TO uP_nIRQD

7) REPLACED R56 WITH JP24

8) CHANGED R57-R62 FROM 12 OHMS TO 0 OHMS – SDK/DK BASEBOARDS HAVE REQUIRED IMPEDENCE MATCHING CIRCUITRY

9) SWAPPED MFP33, MFP32 – uP_nEXT_PWR AND uP_BUZZER

REVISION 101 -> 201

1) ADDED 33K PULLUP TO NET uP_nSW_RESET

2) CHANGED NET NAME OF CPLD_nCS_EEPROM TO CPLD_CS_EEPROM BECAUSE IT IS ACTIVE HIGH

REVISION 1 -> 2

1) ADDED R105 PULLUP TO uP_WAKEUP

2) ADDED R16, R70, R72 SERIES RESISTORS FOR EMI REDUCTION

3) REMOVED TP11 AND TP12

4) RENAMED TOUCH NETS

5) RENAMED CHIP SELECTS CS6 AND CS7

6) CHANGED PULL UP R48 TO 1K OHM

7) SWAPPED USB1, USB2, AND USB DEVICE DATA AND CONTROL SIGNALS AROUND TO SUPPORT DEVICE AND HOST FUNCTION ON SDK APPLICATION BOARD

8) CHANGED uP_nDRV, uP_PA3, uP_CFA9 - CFA25 - nCFENB - PH3 TO uP_SLOT1, uP_nDRV, uP_SLOT2

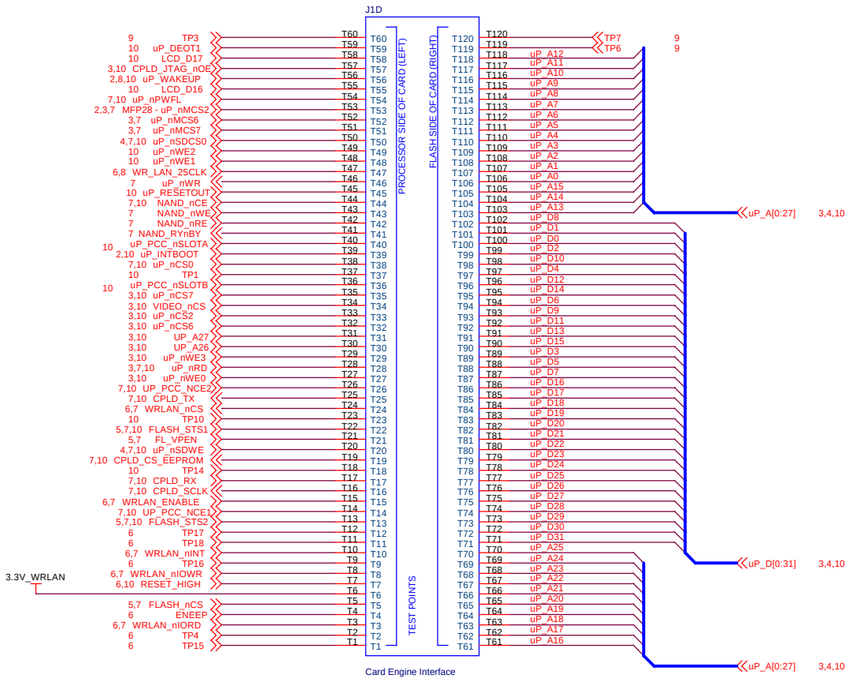
9) REMOVED uP_PWMEN1, uP_PWM1, uP_PWM2, uP_PWM3, uP_SCKE0, uP_SCKE1, uP_SCKE2, uP_nSDCS3

Schematic Modify Date = Monday, June 28, 2004

LOGIC
PRODUCT DEVELOPMENT
411 WASHINGTON AVE. N
MINNEAPOLIS, MN 55401
PHONE: (612) 672-9495
FAX: (612) 672-9469

Title	LH7A404-11 Card Engine		
Size	Custom	Number	800002458
Rev	201		
Design Create Date = Friday, October 18, 2002	Project	LH7A404-11	Sheet 10 Of 12

11 - TEST POINTS



REVISION 101-> 201

1) CHANGED NET NAME OF CPLD_nCS_EEPROM TO CPLD_CS_EEPROM BECAUSE IT IS ACTIVE HIGH

REVISION 3 -> 101

1) ADDED uP_MCS6, uP_MCS7, MFP28 - uP_nMCS2 TO TESTPOINTS

REVISION 2 -> 3

1) REMOVED uP_SDCKE

REVISION 1 -> 2

1) REMOVED TP11 AND TP12

Schematic Modify Date = Monday, June 28, 2004

LOGIC
PRODUCT DEVELOPMENT
411 WASHINGTON AVE. N
MINNEAPOLIS, MN 55401
PHONE: (612) 672-9495
FAX: (612) 672-9489

Title LH7A404-11 Card Engine			
Size C	Number 80000258		Rev 201
Design Create Date = Friday, October 18, 2002	Project LH7A404-11		Sheet 11 Of 12

12 - ECO LIST

Revision Control			
ECO Number	Rev	Description of Change	Date
	3	Release For Production	2/23/04
LH7A404-10-001		ADDED U20 TO SUPPORT EPROM	2/27/04
		REMOVED DOUBLE PULLUP ON MSTR_nRST (R37)	2/27/04
		ADDED FILTER CAPS TO TOUCH LINES AS NO-POPS	2/27/04
		ADDED R116, R117, AND JP1 TO SUPPORT MULTIPLE FLASH MANUFACTURERS	2/27/04
		ADDED EMI REDUCING CAPACITORS:C96 - C106	3/9/04
		ADDED NETS NAND_nRE, NAND_nWE, AND NAND_nCE TO THE FPGA	3/9/04
		CHANGED NETS uP_nCS6, uP_nCS7, AND uP_nCS2 TO BE BUFFERED INPUTS TO THE CPLD NAMED uP_nMCS6, uP_nMCS7, AND MFP28 - uP_nMCS2	3/11/04
		ADDED AUTO WAKEUP CIRCUITRY IF U10 NOT POPULATED	3/11/04
		CHANGED MODEL NUMBER TO -11 DESIGN-WIDE	4/06/04
		CHANGED DEFAULT POPULATION OF THE JUMPER BLOCK	4/16/04
		ADDED uP_MCS6, uP_MCS7, MFP28 - uP_nMCS2 TO TESTPOINTS	4/16/04
		CHANGED STANDARD SDRAM POPULATION TO 64MB	4/16/04
		ADDED PULLUP ON WP ON U21	4/16/04
		REMOVED NETS uP_PCC_CE1A, uP_PCC_CE2A FROM CPLD	4/16/04
		ADDED PULLDOWN TO USB OVERCURRENT SIGNAL	4/16/04
		REMOVED NET uP_PER AND REPLACED IT WITH uP_UARTB_RTS	4/16/04
		SWAPPED NETS uP_PCC_RDYA AND uP_PCC_RDYB ON THE TWO EXPANSION CONNECTORS	4/16/04
		ADDED 22 OHM SERIES RESISTORS ON THE SDRAM CONTROL SIGNALS, uP_nSDC0, uP_nRAS, uP_nCAS, uP_nSDWE	4/16/04
		ADDED 1K PULLUP ON BUFF_nOE PER 7727 JAM PLAYER DEBUG	4/16/04
		GLOBALLY CHANGED MOST PULLUPS/PULLDOWNS TO 33K	4/16/04
		ADDED NAND FLASH INTERFACE	4/16/04
		MADE AUTO WAKEUP CIRCUITRY TO BE ALWAYS POPULATED	4/22/04
		REMOVED NETS WRLAN_25, AND uP_WAKEUP, AND ADDED uP_STANDBY AND NEW NET uP_nPWFL	4/22/04
		ADDED NEW NET FROM CPLD: uP_nPWFL	4/22/04
	101	READY FOR RELEASE	
		PROCESSOR - ADDED 33K PULLUP TO NET uP_nSW_RESET	6/11/04
		PROCESSOR, CPLD, TESTPOINTS - CHANGED NET NAME OF CPLD_nCS_EEPROM TO CPLD_CS_EEPROM BECAUSE IT IS ACTIVE HIGH	6/11/04
		CPLD - ADDED PULLUP TO NET uP_nSTANDBY, THAT IS SELECTABLE BTWN 3.3V AND 3.3V_uP_SDRAM	6/11/04
		CPLD - FIXED CPLD JTAG LINES	6/11/04
		CPLD - ADDED CAP TO FILTER OUT POSSIBLE GLITCH ON BUFF DIR DATA NET	6/28/04

Schematic Modify Date = Monday, June 28, 2004

LOGIC
PRODUCT DEVELOPMENT
411 WASHINGTON AVE. N
MINNEAPOLIS, MN 55401
PHONE: (612) 672-9495
FAX: (612) 672-9489

Title LH7A404-11 Card Engine

Size C | Number 80000258 | Rev 201

Design Create Date = Friday, October 18, 2002 | Project LH7A404-11 | Sheet 12 Of 12