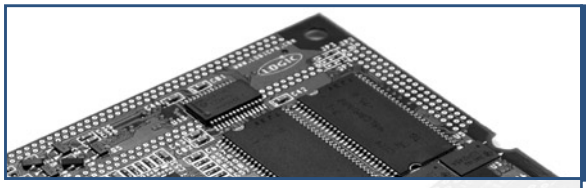
LOGIC PRODUCT DEVELOPMENT WWW.LOGICPD.COM



Zoom™

Card Engine

LH7A404-11 Card Engine Hardware Specification

REVISION HISTORY

REV	EDITOR	REVISION DESCRIPTION	CARD ENGINE REV	APPROVAL	DATE
1	Erik Reynolds	Beta	-	ER	5/28/2004
A	James Wicks	Removed Preliminary References	A	ER	8/19/2004
B	James Wicks	Updated Pin Descriptions	201	ER	1/13/2005

Please check www.logicpd.com for the latest revision of this manual, errata's, and additional application notes.

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LH7A404 CARD ENGINE

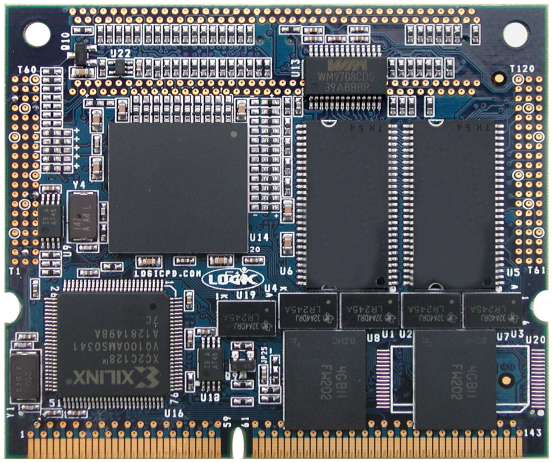
Developing products is as simple as

A B C

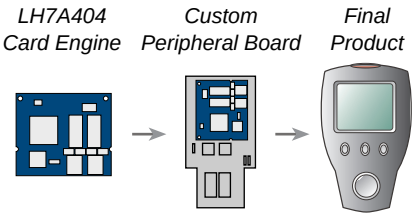
- A Application Development Kits
- B Board Support Packages
- C Card Engines

The LH7A404 Card Engine is a compact, product-ready hardware and software solution for developing embedded products with **less time, less cost, less risk ... more innovation.**

The LH7A404 Card Engine is a complete embedded computing module offering essential features for handheld and embedded networking applications in the industrial, consumer and medical markets. The use of custom peripheral boards makes the Card Engine the ideal foundation for OEMs developing handheld and compact products. The Card Engine provides a common reference pin-out on its expansion connectors, which enables customers to easily scale to next generation micro controller Card Engines when new functionality or performance is required.



Actual Size (2.37" x 2.67")



SOFTWARE HIGHLIGHTS

- Ready to run Windows™ CE or Linux BSPs
- Bootloader/Monitor
- Board Support Packages
- Custom Linux or Windows™ CE device driver development

CUSTOMER SUPPORT

Logic provides technical support for Card Engines. Various support packages are available; contact us for more information.

- **Processor** Sharp LH7A404 32 bit ARM922TDMI RISC microprocessor
  - Running up to 200 MHz (0 to 70 Degrees C) with 100 MHz bus speed
  - Running up to 166 MHZ (-40 to 85 Degrees C) with 83 MHz bus speed
- **SDRAM Memory** 32, 64, or 128 MBytes on board
- **Flash Memory** Up to 32 MBytes on board
- **Display** Programmable color LCD controller
  - Built in driver supports up to 1024 x 768 x 16 bit color
  - Supports STN, Color STN, Dual STN, HR-TFT, AD-TFT, TFT
- **Touch Screen** Four or Five wire integrated touch interface
- **Network Support** 10/100 BASE-T Ethernet controller (application/debug)
  - SMSC LAN 91C111 (MAC & PHY)
- **Audio** Audio Codec AC97 (Wolfson WM9708)
- **Memory Card Expansion**
  - CompactFlash Type 1 card (memory storage only)
  - Dual PCMCIA interface
  - Smart Card Interface (ISO7816)
  - MMC/SD
- **USB** 2 X USB host and 1 device interface (USB 1.1)
- **Serial Ports** 3 X 16C550 like, standard UARTs
- **IrDA** SIR supports up to 115.2 Kbps
- **PS2** PS2 Keyboard & Mouse
- **GPIO** Programmable depending on peripheral requirements
- **SSP** Supports either Motorola SPI™, National Semiconductor MICROWIRE™, TI SSI
- **Software**
  - Windows™ CE and Linux BSPs available
  - LogicLoader™ (bootloader/monitor)
- **Mechanical**
  - Compact Size: 2.37" (60.2 mm) long x 2.67" (67.8 mm) wide x 0.17" (4.4 mm) high
  - 144 pin SODIMM Connector for connection to custom peripheral board
  - Two high density 80-pin expansion connectors for peripheral access
- **Application Development Kits**
  - Zoom™ Starter Development Kit
  - Zoom™ Integrated Development Kit (Avail. Soon)

SHARP

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DN: 1000571 Rev A

1.2 Acronyms

ACI	Audio CODEC Interface
ADC	Analog to Digital Converter
AFE	Analog Front End Interface
AHB	Advanced Hardware Bus
BSP	Board Support Package
CPLD	Complex Programmable Logic Device
DAC	Digital to Analog Converter
DC	Direct Current
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
ENDEC	Encoder Decoder
ESD	Electro Static Dissipative
FET	Field Effect Transistor
FIQ	Fast Interrupt Request
FIFO	First In First Out
GPIO	General Purpose Input Output
HAL	Hardware Abstraction Layer
IC	Integrated Circuit
I²S	Inter-IC Sound
IDK	Integrated Development Kit
I/O	Input/Output
IRQ	Interrupt Request
LCD	Liquid Crystal Display
LOLO	LogicLoader™
MMC	Multi Media Card
NC	No Connect
PHY	Physical Layer
PLL	Phase Lock Loop
PMOS	P Metal Oxide Semiconductor
RTC	Real Time Clock
SDK	Starter Development Kit
SDRAM	Synchronous Dynamic Random Access Memory
SIR	Serial Infrared
SoC	System-on-Chip
SSP	Synchronous Serial Port
SPI	Standard Programming Interface
TSC	Touch Screen Controller
TTL	Transistor-Transistor Logic
UART	Universal Asynchronous Receive Transmit
UHCI	Universal Host Controller Interface
VIC	Vectored Interrupt Controller

1.3 Technical Specification

Please refer to the following component specifications and data sheets.

LH7A404-11 Card Engine IO Controller Interface Specification
LogicLoader™ User's Manual
LH7A404 Universal Microcontroller User's Guide
Altera MAX 7000A CPLD data sheet (EPM7128)
Altera Device Package Information data sheet
Altera Ordering Information
Wolfson WM9708 AC97 Audio CODEC data sheet

1.4 Card Engine Advantages

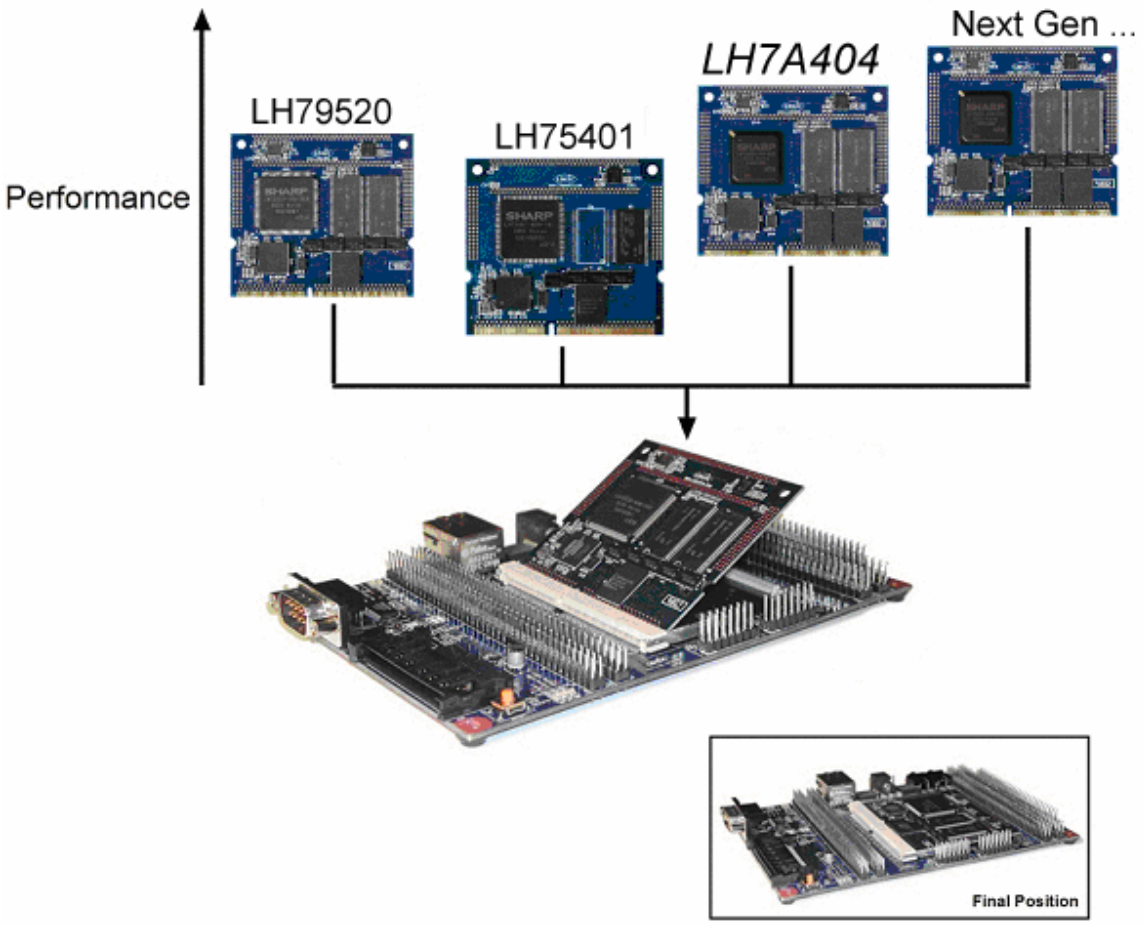
Logic's Card Engines accelerate your product's time-to-market, and provide the following advantages:

- Product Ready Hardware and Software solutions allow immediate application development that results in a shorter product development cycle with less time, less cost, less risk… more innovation.
  - Less time – time to market solution allows software application development to begin immediately
  - Less cost – significantly lowers development cost
  - Less risk – complex portion of design product ready
  - More innovation – Allows you to focus on other aspects of your design
- Common Card Engine Footprint (See Figure 1.1)
  - Easy migration path to new processors and technology
  - Provides a scaleable solution for your product family
  - Extends product life cycle – worry free component obsolescence
- Low Cost Hardware Solution – Custom configurations are available to meet your design requirements and price points.
- Complex portion of the design complete and ready to go.

1.5 Card Engine Interface

Logic's common Card Engine interface allows for easy migration to new processors and technology. Logic is constantly researching and developing new technologies to improve performance, lower cost, and increase feature capabilities. By using the common Card Engine footprint, it is possible to take advantage of Logic's work without having to re-spin the old design. Contact Logic sales for more information.

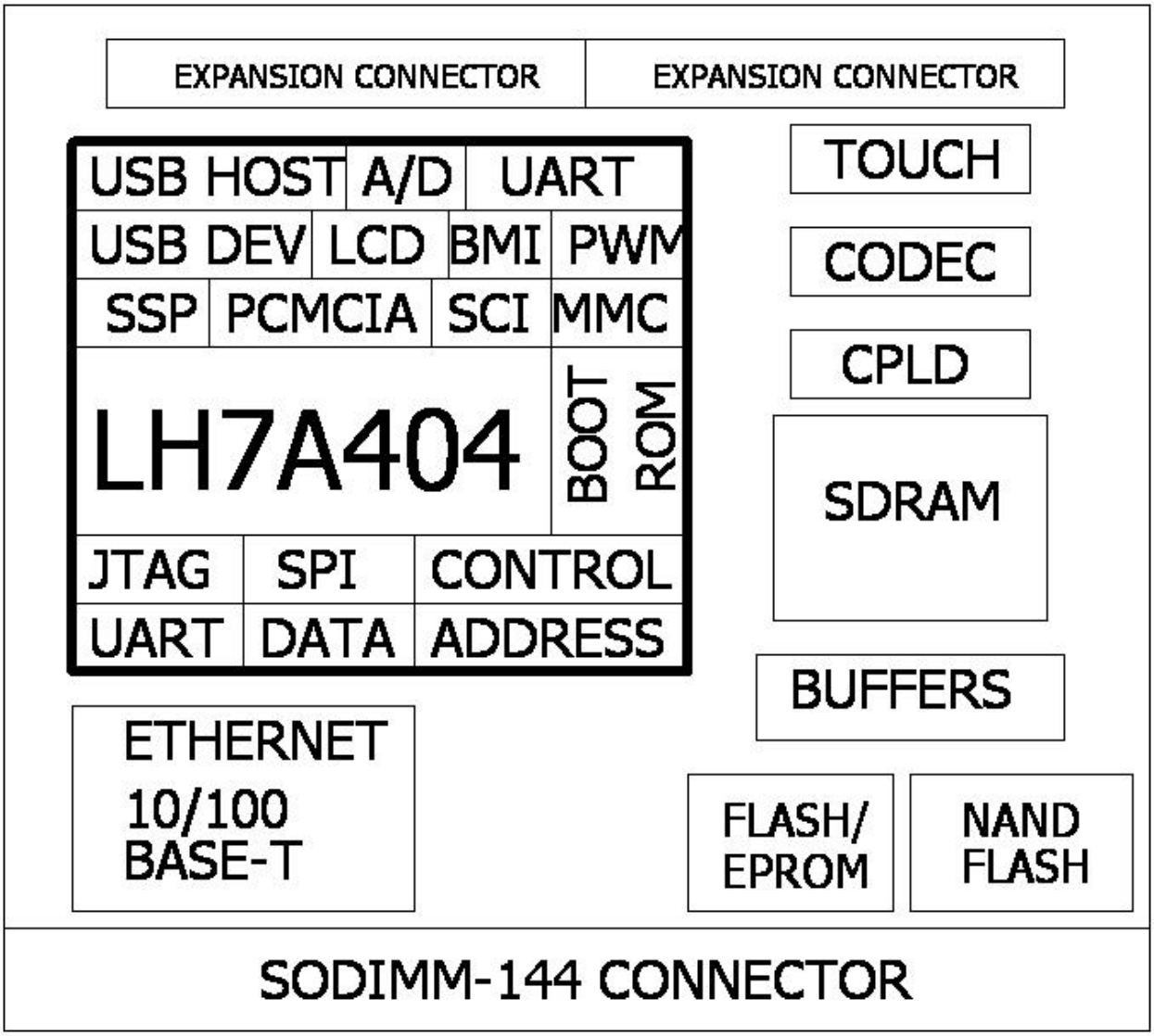
Figure 1.1: Card Engine Advantages



In fact, encapsulating a significant amount of your design onto the Card Engine reduces any long-term risk of obsolescence. If a component on the Card Engine design becomes obsolete, Logic will simply design for alternative part that is transparent to your product. Furthermore, Logic tests all Card Engines prior to delivery, decreasing time-to-market and ensuring a simpler and less costly manufacturing process.

1.6 LH7A404-11 Card Engine Block Diagram

Figure 1.2: LH7A404-11 Card Engine Block Diagram



1.7 Electrical, Mechanical, and Environmental Specifications

1.7.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	unit
DC IO and Peripheral Supply Voltage	3.3V	-0.3 to 4.6	V
DC Core Supply Voltage	VCORE	-0.3 to 2.4	V

NOTE: These stress ratings are only for transient conditions. Operation at or beyond absolute maximum rating conditions may affect reliability and cause permanent damage to the Card Engine and its components.

1.7.1.1 Recommended Operating Conditions

Parameter	Min	Typical	Max	Unit	Notes
DC IO and Peripheral Supply Voltage	3.0	3.3	3.6	V	1
DC IO Supply Active Current	TBD	TBD	TBD	mA	2
DC IO Supply Standby Current	TBD	TBD	TBD	mA	2
DC IO Supply Sleep Current	TBD	TBD	TBD	mA	2
DC Core Supply Voltage	1.62	1.8	1.98	V	1
DC Core Supply Active Current	TBD	TBD	TBD	mA	2
DC Core Supply Standby Current	TBD	TBD	TBD	mA	2
DC Core Supply Sleep Current	TBD	0	TBD	mA	2
Commercial Operating Temperature	0	25	70	°C	
Industrial Operating Temperature	-40	25	85	°C	3
Storage Temperature	-40	25	85	°C	
Dimensions		2.35 x 2.6		Inches	
Weight		17		Grams	4
Connector Insertion/removal		50		Cycles	
Input Signal High Voltage		2.0		V	
Input Signal Low Voltage		0.8		V	
Output Signal High Voltage	2.6		VIO	V	
Output Signal Low Voltage	GND		0.4	V	

1. Core voltage must never exceed IO and peripheral supply voltage.
2. This test was performed with the 91C111 chip power disabled.
3. Contact Logic for more information on an industrial temperature LH7A404-11 Card Engine
4. May vary depending on Card Engine configuration.

2 Electrical Specification

2.1 Microcontroller

2.1.1 LH7A404 Microcontroller

The LH7A404-11 Card Engine uses Sharp's highly integrated system on a chip LH7A404 microcontroller. This SoC possesses a 32-bit ARM922T RISC core and provides many integrated on-chip peripherals including:

Integrated ARM922T™ Core
- 32-bit ARM922T™ RISC Core
- 16kB Cache: 8kB Instruction Cache and 8kB Data Cache
- MMU
- 4 GB logical address space

80 KB on-chip SRAM
Integrated LCD Controller
- Up to 800 x 600 Resolution at 16-bit color
  - (1024 x 786 at 8 bits color)
- Supports STN, TFT, and HR-TFT
- Up to 65,536 Colors

Three UART's
Classic IrDA (up to 115.2 Kbps)
SSP interface
AC97 CODEC Interface
1 USB Client and 1 USB host Interface (USB 1.1)
MultiMediaCard/Secure Digital interface
Smart Card interface (ISO7816)
Smart Battery Monitor Interface
Up to 64 General Purpose I/O Signals
Two 16-bit Pulse Width Modulators
- **Ten fully independent DMA Channels**

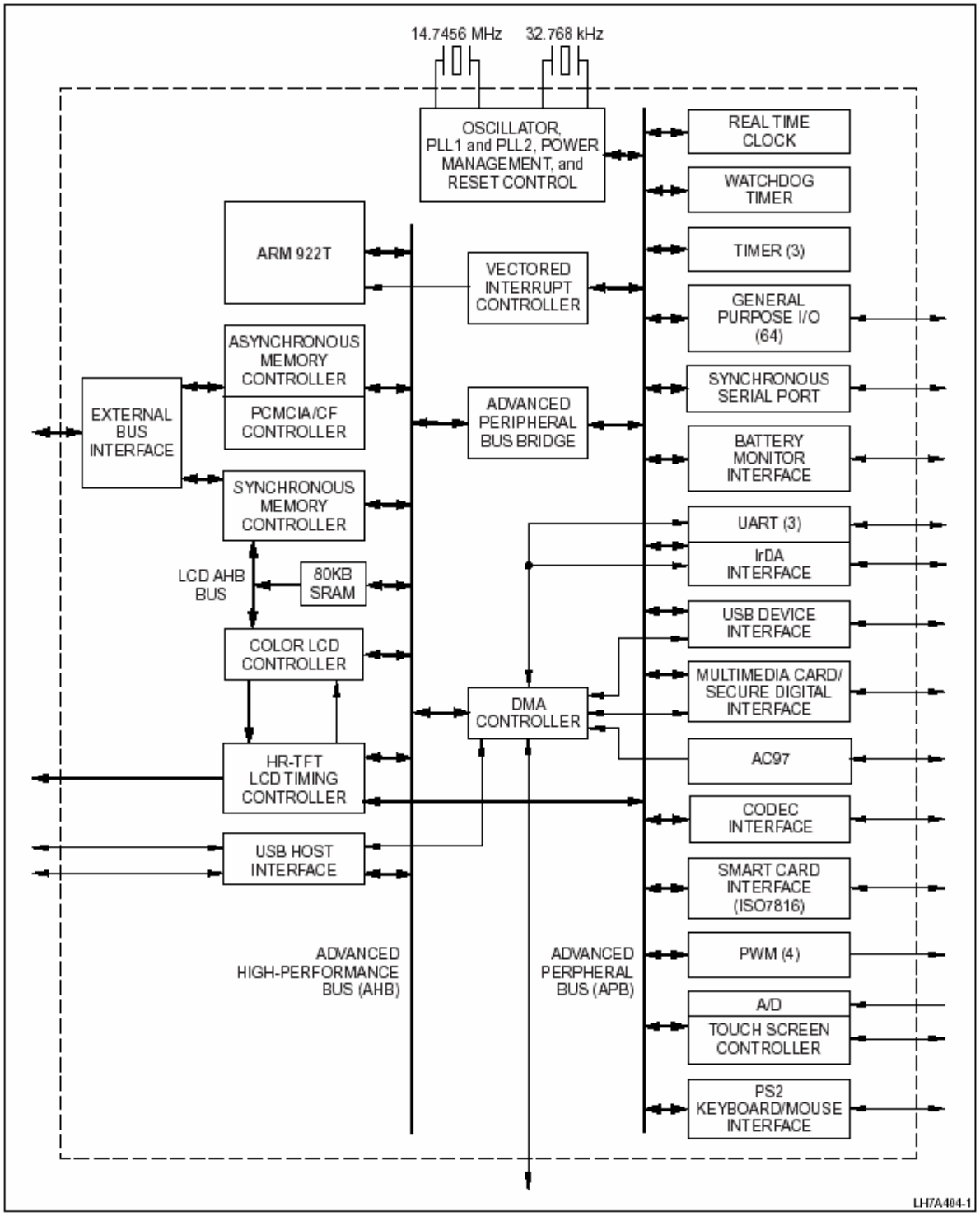
Three Programmable Timers
RTC
Boot ROM
Low Power Modes
5-Volt Tolerant Inputs

See Sharp's LH7A404 Universal Microcontroller User's Guide for additional information.
http://www.sharpsma.com/

IMPORTANT NOTE: Please see http://www.sharpsma.com/ for errata on the LH7A404.

2.1.2 LH7A404 Microcontroller Block Diagram

Figure 2.1: LH7A404 Microcontroller Block Diagram



2.2 Clocks

The LH7A404 requires 2 crystals in order to enable proper internal timing. The first, a 14.7456 MHz crystal, is used to generate many of the processor's internal clocks via a series of signal dividers. To generate the FCLK signal, for example, the 14.7456 MHz signal is run through a PLL in which the divisor is set in the Clock Set register. FCLK is then used internally as the Synchronous Bus Mode core clocking for the ARM922T core and cache. The 14.7456 MHz signal is also used to create the HCLK, HCLK_CPU, PCLK, and peripheral clock signals. One such peripheral clock is set up through a separate PLL to produce a 48.0 MHz clock for USB operations. An additional signal which stems from the crystal input is the uP_AUX_CLK signal; it is produced through a programmable divider on the card engine. The uP_AUX_CLK is provided on the 144-pin SO-DIMM expansion connector as the LH7A404 CLKOUT, and is set to a default of 14.7456MHz.

IMPORTANT NOTE: Please see Sharp's LH7A404 Universal Microcontroller User's Guide for additional information about the relationship between FCLK and HCLK.

The second required crystal runs at 32.768 kHz and is the only permanently running clock in the LH7A404. Because this clock runs regardless of the processor's state, a ripple divider is used in order to reduce power consumption during the halt and standby states. This divider produces the 1 Hz signal for the RTC interface as well as intermediate frequencies of 16kHz and 8kHz for the state controller and PLL interlocks.

The LH7A404 is able to operate in three different clocking modes: asynchronous, synchronous, or FastBus extension. Each of the three has certain advantages or disadvantages in system throughput and power consumption, depending on the whether the end application is CPU-, memory-, or peripheral-intensive. Refer to the LH7A400 Universal Microcontroller User's Guide for information on the specific advantages/disadvantages of each bus-clocking mode

The LH7A404's microcontroller core clock speed is initialized to 200 MHz on the Card Engine and the Bus speed is set at 100 MHz in the LogicLoader™. Other clock speeds can be supported and modified in software for specific user applications, such as a specific serial baud rate.

The LH7A404-11 Card Engine provides an external Bus clock, uP_BUS_CLK, on the 144-pin SO-DIMM connector. The uP_BUS_CLK, which is connected to the processor's SCLK, is set to a default of 100 MHz. SCLK also serves as the SDRAM and CPLD clock on the LH7A404-11 Card Engine.

LH7A404 Microcontroller Signal Name	LH7A404-11 Card Engine Net Name	Default Software Value in LogicLoader™
FCLK	N/A	200 MHz
HCLK	N/A	100 MHz
SCLK	uP_BUS_CLK	100 MHz
PGMCLK	uP_AUX_CLK	14.7456 MHz

2.3 Memory

2.3.1 Synchronous DRAM

The LH7A404-11 Card Engine uses a 32-bit memory bus to interface to SDRAM. The memory can be configured as 16, 32 or 64MBs in order to meet the user's memory requirements and cost constraints. Logic's default memory configuration on both the IDK and SDK boards is specified as 32 MB.

2.3.2 Direct Memory Access (DMA)

The Sharp LH7A404 microcontroller has an internal DMA controller that offers 10 fully independent channels. These channels can be used to interface streams from 20 internal peripherals to the system memory (including USB, SD/MMC, AAC, and all three UARTs). The DMA controller can also be used to interface streams from Memory to Memory or Memory to External Peripheral using 2 dedicated M2M channels. External handshake signals are available to support transfers to/from external peripherals. For more information on using the DMA refer to the LH7A404 Universal Microcontroller User's Guide.

2.3.3 NOR flash

The LH7A404-11 Card Engine uses a 32-bit memory bus (split into 2, 16-bit channels, one to each flash memory) to interface to Intel StrataFlash memory chips. The onboard Card Engine memory can be configured as 8, 16, or 32MBs to meet the user's flash requirements and cost constraints. Logic's default flash configuration is 16MB on the SDK and 32MB on the IDK. Because flash is one of the most expensive components on the LH7A404-11 Card Engine, it is important to contact Logic when determining the necessary flash size.

It is possible to expand the system's non-volatile storage capability by adding external flash IC's, CompactFlash, or NAND flash. See the LH7A404-11 Application Kit for reference designs or contact Logic for other possible peripheral designs.

2.3.4 NAND flash

The LH7A404-11 Card Engine can be configured to boot from and use NAND flash. This functionality is currently under development, please contact Logic for more information.

2.3.5 EPROM

The LH7A404-11 Card Engine can be configured to boot from on board EPROM. This functionality is currently under development, please contact Logic for more information.

2.3.6 CompactFlash (memory-mapped mode only)

The LH7A404-11 Card Engine supports a CompactFlash memory-mapped mode only slot that compliments the processor's standard dual PC card support. The LH7A404-11 Card Engine uses the CPLD to provide the necessary signals for a CompactFlash card interface in memory-mapped mode only. The Zoom™ Starter Kit reference design includes a CompactFlash connector for memory-mapped mode, but does not support hot-swappable capability. If hot-swappable capability is desired, it can be achieved by adding further hardware on the user's base-board. See the LH7A404-11 CPLD IO controller specification for further details on the use of CompactFlash.

IMPORTANT NOTE: The CPLD CompactFlash interface supports memory-mapped mode only. Use the LH7A404 processor's PC card slots for more PC card mode options.

2.4 Secure Digital (SD) and MultiMediaCard (MMC)

The LH7A404-11 Card Engine provides one SD/MMC adapter that can be used as an MMC card or SD card. This controller supports the full MMC/SD bus protocol identified in the MMC System Specification 2.11 and SD Memory Card Specification Version 1.0. The controller can also implement a SPI interface to either card. For more detailed operation and programming operations see the MultiMediaCard Association and SD Card System Specifications, available at www.mmca.org and www.sdcard.org, respectively.

2.5 PCMCIA/CompactFlash (external)

Both PCMCIA and CF devices are externally supported on the LH7A404 card engine. To handle these devices, the static memory controller has allocated two of the eight configurable memory banks for PCMCIA and CF interfaces. The Card Engine can directly support one PCMCIA/CompactFlash card and has the capability to interface to two cards with minimal external circuitry through the CPLD. Please refer to the IDK kit for an example implementation. In order to properly take advantage of these features software parameters need to be set; see Chapter 5: "Static Memory Controller" in the LH7A404 Universal Microcontroller User's Guide for more information.

2.6 10/100 Ethernet Controller

The LH7A404-11 Card Engine uses the SMSC 91C111 10/100 single chip Ethernet Controller to provide an easy-to-use networking interface. To facilitate use, six signals from the 91C111 are mapped to external connectors: transmit plus/minus, receive plus/minus, and two status LED's. The four analog PHY interface signals (transmit/receive) each require an external impedance matching circuit to operate properly. Logic provides an example circuit schematic in the LH7A404-11 Application Kit for reference.

IMPORTANT NOTE: The ENEEP signal on the SMSC 91C111 is connected to a zero ohm resistor that is not populated. This is because the ENEEP signal has a weak internal pull-up in the SMSC 91C111and if the signal is tied low it low will disable the serial EEPROM interface.

2.7 Audio CODEC

The LH7A404 processor has an internal AC97 controller that is compliant with the Audio CODEC '97 Component Specification, v2.2. This AC97 Controller implements a 5-pin serial interface to the AC97 Audio CODEC, in this case the Wolfson WM9708. From the Wolfson CODEC on the LH7A404-11 Card Engine there are 3 outputs, CODEC_OUTL, CODEC_OUTR, and MFP34 – MONO_OUT. All of these signals are available from the 80-pin expansion connectors.

IMPORTANT NOTE: See Intel's specifications for the AC97 standard available on the Internet at http://www.intel.com/ial/scalableplatforms/audio.

The Wolfson CODEC on the LH7A404 Card Engine performs full duplex 18-bit CODEC functions and supports variable sample rates from 8-48k samples/second. The Wolfson chip also has an onboard 24.576 MHz crystal which is used for the AC97 master clock frequency.

NOTE: The Sharp LH7A404 also offers an ACI interface for non-AC97 CODEC devices. This interface provides a digital 8-bit interface that is multiplexed with the signals from the AC97 controller. If you are looking for a different CODEC option, Logic has previously interfaced different high performance audio CODEC's into other Card Engines. Contact Logic for assistance in selecting an appropriate audio CODEC for your application.

2.8 Video Interface

Sharp's LH7A404 microcontroller has a built in LCD controller supporting STN, Color STN, HR-TFT, AD-TFT, TFT panels at up to 800 x 600 x 16-bit or 1024 x 768 x 8-bit color resolution. See the LH7A404 Universal Microcontroller User's Guide for further information on the integrated LCD controller. The signals from the LH7A404's LCD controller are organized by bit and color and can be interfaced through the J1A expansion connectors. Logic has written drivers for numerous panels of different types and sizes. Please contact Logic before selecting a panel for your application.

IMPORTANT NOTE: Using the internal graphics controller will affect processor performance. Selecting display resolutions and color bits per pixel will vary processor busload.

2.9 Serial Interface

The LH7A404-11 Card Engine comes with the following serial channels: UARTA, UARTB, UARTC, and SSP. If additional serial channels are required, please contact Logic for reference designs. UARTC supports both wired serial and infrared communications, supporting a digital encoded output and decoded input without analog processing. Please see the LH7A404 Universal Microcontroller User's Guide for further information regarding serial communications.

2.9.1 UARTA

UARTA has been configured to be the LH7A404-11 development kit's main serial port. It is an asynchronous 16C550-compatible UART. This UART provides a high-speed serial interface that uses FIFO and is capable of sending and receiving serial data simultaneously. The signals from the Card Engine are TTL level signals not RS232 level. The user must provide an external RS232 transceiver for RS232 applications. Logic has provided an example reference design with the SDK and IDK kits. When choosing an RS232 transceiver, the user should keep in mind cost, availability, ESD protection, and data rates.

UARTA's baud rate is set by default to 115.2K bits/sec, though it supports all common serial baud rates from 2.4kbps to 460.8kbps. UARTA is available off the J1C 144-pin SO-DIMM connector.

2.9.2 UARTB

Serial Port UARTB has dual functionality; its primary function is as an asynchronous 16C550 compatible UART. This UART is a high-speed serial interface that uses FIFO, and it is capable of sending and receiving serial data simultaneously. The signals from the Card Engine are TTL level signals, not RS232 level. The user is responsible for providing an external RS232 transceiver for RS232 applications. UARTB's baud rate can also be set to all common serial baud rates from 2.4kbps to 460.8kbps.

The UARTB pins are multiplexed with GPIO Ports B1-B5; when UARTB is not in use, the GPIO pins can be used instead. UARTB is available off the J1B 80-pin expansion connector.

2.9.3 UARTC

Like UARTA and UARTB, UARTC supports serial communications. Unlike the previous UART's, however, UARTC also supports the infrared communication protocol. When functioning as a serial port, UARTC will perform many of the characteristics as discussed above, only UARTC does not have any status signals. If status signals are desired, it is necessary to map these control signals to GPIO ports.

In order to define UARTC's functionality, a programmable register is available to specify infrared or serial operation. Once one communication is chosen, the pins for the other connection are ignored, and vice-versa. The pins used for UARTC's functions are uP_IRTX and uP_IRRX (infrared) and uP_UARTC_RX and uP_UARTC_TX (serial), available off the J1B 80-pin expansion connector. Because there are two sets of transmission signals, UARTC's serial transmit and receive pins are multiplexed with GPIO Ports B0 and C0, becoming available GPIO pins when Infrared communications are not being used (the two sets of signals would otherwise be redundant). Refer to Sharp's LH7A404 Universal Microcontroller User's Guide for more information on using infrared communications.

2.9.4 SSP/SPI

The SSP interface on the LH7A404 Card Engine supports three data frame formats:

- Texas Instruments' SSI

- Motorola SPI
- National Semiconductor Microwire

Logic has chosen to implement Motorola's SPI interface as the default setting. If another interface is desired, programming the Control Register 0's 2-bit Frame Format field allows the default settings to be adjusted. The SPI format is used to interface between the parallel data inside the SoC and synchronous serial communications on slave peripheral devices. The SPI interface is master-only, with programmable clock rate and pre-scale options that are used to generate the appropriate bit-rate and Serial Clock output. The Data Size Specification is also configurable, and as such the SPI port can receive or transport anywhere from 4 to 16 bits. The SPI signals are available off the 144-pin SO-DIMM connector. Please see the LH7A404 Universal Microcontroller User's Guide for further information.

2.10 Keyboard and Mouse Interface (KMI)

The LH7A404 KMI implements a standard IBM PS2 or AT-compatible keyboard and mouse interface and complies with the AMBA specification rev 2.0. Communications with the KMI can be initiated through polling or interrupts. Furthermore, the interface offers a programmable clock divider, odd-bit parity generation/checking, and open drain outputs. Refer to Sharp's LH7A404 Universal Microcontroller User's Guide for more information about using a keyboard or mouse with the LH7A404-11 Card Engine.

2.11 USB Interface

The LH7A404 card engine is configured with both USB Host and Device functionality. The USB device interface is compliant to the USB 1.1 specification and both the OpenHCI and Intel UHCI specifications. This USB client supports full-speed (12M bits/sec) operation and both suspend and resume signaling. The USB device interface on the LH7A404 is able to transmit, receive data, or control information over the bus, and is available for external use off the J1A 80-pin connector.

The USB Host interface is compatible with both the USB 1.1 and OpenHCI 1.0 specifications. This controller also supports both low speed and high-speed USB devices and features a root hub with two downstream ports. The four signal USB connector signals are available off the J1A 80-pin connector while the host interface control functions are available can be accessed through jumper signals (see section 5.4 J1B Jumper Table) off the J1B 80-pin connector. For more information on using both the USB device and host interfaces, please see the LH7A404 Universal Microcontroller User's Guide for more information on using both the USB device and host interfaces.

IMPORTANT NOTE: In order for USB to be correctly implemented on the LH7A404 card engine, additional impedance matching circuitry is required on the USBP and USBM signals before they can be used. USB 1.1 requirements specify that the impedance on each driver must be between 28Ω and 44Ω. For reference, see the impedance matching circuit on the Logic SDK or IDK board.

2.12 ADC/Touch Interface

The LH7A404-11 Card Engine offers a 10-bit analog-to-digital converter (ADC). This ADC also can be used to implement a touch screen controller (TSC), supporting standard 4-wire resistive touch panels. This TSC supports up to 8-wire touch screens – if more than 4-wire operation is desired, please see the application note 'Using the SHARP ADC with Resistive Touch Screens', available at http://www.sharpsma.com/. The other six A/D signals are available externally off the J1A and J1B 80-pin connectors. Please see the LH7A404 Universal Microcontroller User's Guide for more information.

2.13 General Purpose I/O

Logic designed the LH7A404-11 Card Engine to be flexible and provided multiple options for analog and digital GPIO. There are numerous digital GPIO pins on the Card Engine that interface to the LH7A404, and the Altera CPLD. Some of these GPIO pins are interrupt capable while other signals are input or output only -- see the Pin Descriptions section of this data sheet for more information on these options. If certain peripherals are not desired, such as the LCD Controller, Chip Selects, IRQs, UARTS, AC97, PCMCIA and CompactFlash, Smart Card Interface, or BMI interface, then multiple GPIO pins become available. Please see the table in section 5.5 Multiplexed Signal Trade-Offs for a list of the available GPIO trade-offs.

2.14 CPLD

Please see the LH7A404-11 Card Engine IO Controller Specification for CPLD information.

2.15 Serial EEPROM Interface

Logic designed the LH7A404-11 Card Engine to have a low-cost 1 kbit serial EEPROM for non-volatile data storage. The serial EEPROM is connected to the LH7A404 microcontroller via the CPLD through an SPI interface – discussed in the touch screen controller section above. See figure 2.4 below. For more information please view the LH7A404-11 Card Engine CPLD Interface Specification.

Figure 2.2: Serial EEPROM Block Diagram

2.16 Expansion/Feature Options

The LH7A404-11 Card Engine was designed for expansion and a variable feature set, providing all the necessary control signals and bus signals to expand the user's design. Some of these signals are buffered and brought out to the 144-pin SO-DIMM connector and two 80-pin expansion connectors. It is possible for a user to expand the Card Engine's functionality even further by adding PCI or ISA devices. Some features that are implemented on the LH7A404, but are not discussed herein, include: PWM, DC-DC, BMI, and ACI setup. See the LH7A404 Universal Microcontroller User's Guide and the LH7A404-11 Card Engine schematics for more detail. Logic has experience implementing additional options, including other audio codecs, Ethernet IC's, co-processors, and components on the Card Engine boards. Please contact Logic for potential reference designs before selecting your peripherals.

3 System Integration

3.1 Configuration

The LH7A404-11 Card Engine was designed to meet multiple applications for specific users and budget requirements. As a result, this Card Engine supports a variety of embedded operating systems and comes with the following hardware configurations:

- Flexible memory footprint: 16, 32, or 64MBs SDRAM
- Flexible flash footprint: 8, 16, or 32MBs StrataFlash
- Optional SMSC 91C111 10/100 Ethernet Controller
- Optional Wolfson WM9708 Audio CODEC

Please contact Logic for additional hardware configurations to meet your application needs.

3.2 Resets

3.2.1 Master Reset (Hard Reset)

All hardware peripherals should connect their hardware-reset pin to the MSTR_nRST signal on the SODIMM connector. Internally all card engine peripheral hardware reset pins are connected to either the MSTR_nRST net or to the RESET_HIGH net as shown in the figure below. The MSTR_nRST signal is an open-drain output, enabling the user to assert the MSTR_nRST signal externally. Logic suggests that custom designs implemented with the LH7A404-11 Card Engine use the MSTR_nRST signal as the “pin hole” reset used in commercial embedded systems.

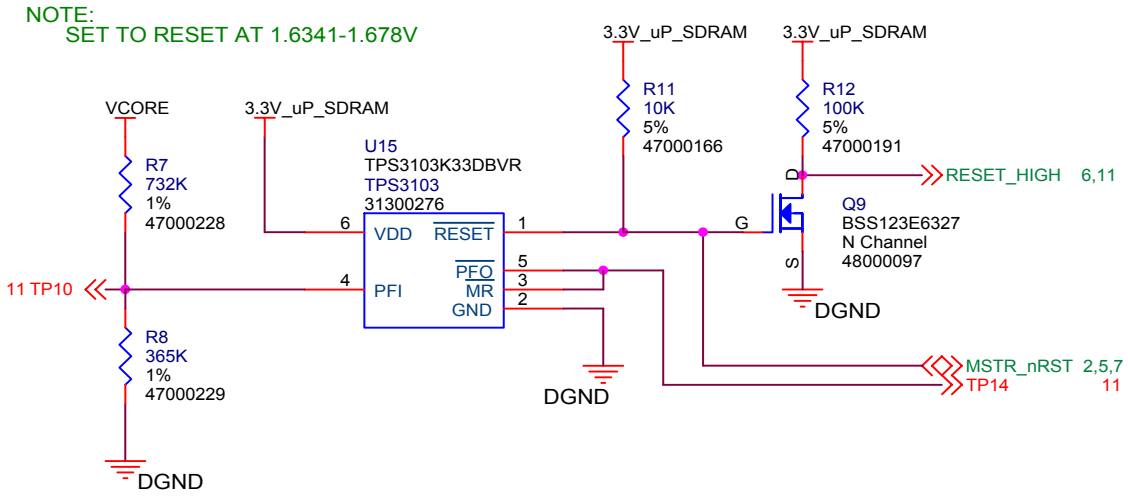


Figure 3.1: Reset Circuit

If the output of the reset chip, MSTR_nRST, is asserted (active low), the user can expect to lose information stored in SDRAM. The data loss occurs because the external signals uP_BUS_CLK and uP_AUX_CLK are interrupted during the assertion of the MSTR_nRST signal. The RESET_HIGH signal, on the other hand, is the active high output of the reset circuit and is not provided as part of the card engine connector interface.

IMPORTANT NOTE: Any custom reset circuit design should guard the assertion of the reset lines during a low power state so as to prevent power-up in a low or bad power condition (which will cause data corruption and possible temporary system lockup). See the section entitled “Power Management” for further details.

There following three conditions will cause a system-wide reset: power-on, a low pulse on the MSTR_nRST signal, and the power fail comparator input (PFI pin) falling below the internal comparator threshold.

Power On:
At power on, the MSTR_nRST signal is asserted low when the supply voltage (VDD) of the reset chip is between 0.4V and 2.941V. Once the 3.3V_uP_SDRAM supply surpasses 2.941V the reset chip will trigger a rising edge of MSTR_nRST after a 65-195ms delay (130ms typical).

Low Pulse on MSTR_nRST Signal:
A low pulse on the MSTR_nRST signal of the reset chip, asserted by an external source (for example, the reset button on the custom design application) will bring MSTR_nRST low until the assertion source is de-asserted. There is no delay beyond the de-assertion of the external MSTR_nRST signal source, so the custom design must ensure that the assertion time is sufficient for all related peripherals.

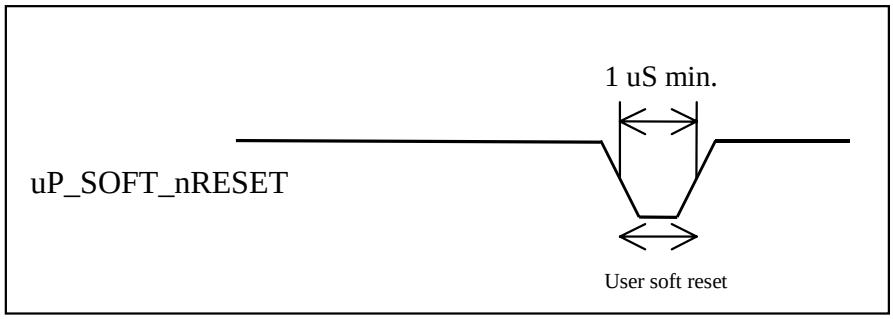
Logic suggests that any external assertion source that triggers the MSTR_nRST signal, analog, or digital de-bouncing be used to generate a clean one shot reset signal.

Power Fail:
If the power fail comparator input pin (PFI pin) falls below the internal comparator threshold of 0.551V, it will create a low pulse on the MR input pin of the reset chip. The low assertion of the MR pin will assert the MSTR_nRST signal and will hold it low after the MR pin is de-asserted (PFI is above the comparator level and power is restored) for 65 to 195 ms (130 ms typical). Please see the TI TPS3103 data sheet at http://www.ti.com for additional details on reset timing and thresholds.

3.2.2 Soft Reset

Logic has created a soft reset signal, SW_nRESET, designated as a reset for the LH7A404's internal registers without affecting the peripherals on the rest of the board or the data stored in SDRAM. The data is saved because the SDRAM controller automatically places the SDRAM in self-refresh before the uP_SD_CLK clock is disabled. As in the Standby state described in section 3.5.4.2, the 32.768 kHz clock continues running, allowing the system to properly wake up. The SW_nRESET signal is an input to the LH7A404 processor's user reset input pin.

Figure 3.2: Soft Reset



See Sharp's LH7A404 Universal Microcontroller User's Guide for additional information on register conditions after a soft (manual) reset.

3.3 Interrupts

The LH7A404 incorporates two Vectored Interrupt Controllers (VIC1 and VIC2): the advantage being that a vectored interrupt has improved latency as it provides direct information where service routines are located, eliminating the need for levels of software arbitration. Through these

two interrupt controllers the LH7A404 can prioritize and process up to 64 interrupts (40 internal). Table 3.3 shows list of the interrupt hierarchy, ordered by priority. All VIC1 interrupts have a higher priority than any VIC2 interrupts. In both VIC's FIQ interrupts have the highest priority, followed by interrupt vector 0 through interrupt vector 15; non-vectored IRQ interrupts have the lowest priority. Refer to Sharp's LH7A404 Universal Microcontroller User's Guide for further information on using IRQ and FIQ interrupts.

VIC	INTERRUPT TYPE
VIC1	FIQ Interrupt(s)
VIC1	Vectored Interrupts 0-15 (in that order)
VIC1	Non-vectored Interrupts
VIC2	FIQ Interrupt(s)
VIC2	Vectored Interrupts 0-15 (in that order)
VIC2	Non-vectored Interrupts

Figure 3.3: Interrupt Priorities (high to low)

NOTE: The CPLD interrupts the processor via the uP_nIRQE signal. This signal is a FIQ interrupt (PF4) in VIC2.

3.4 JTAG Debugger Interface

The JTAG connection on the LH7A404 allows recovery of corrupted flash memory and real time applications debug. When choosing a debugger board, remember that many different third-party JTAG debuggers are available for Sharp ARM microcontrollers. The following signals make up the JTAG interface to the LH7A404: uP_TDI, uP_TMS, uP_TCK, and uP_TDO. These signals should interface directly to a 20-pin 0.1" through-hole connector as demonstrated in the Sharp LH7A404 Universal Microcontroller User's Guide, or as shown on reference schematics.

IMPORTANT NOTE: When laying the 20-pin connector out, realize it may not be numbered as a standard 20-pin 0.1" IDC through-hole connector. See LH7A404-11 Card Engine Application Kit reference design for further details. Different IC manufacturers define the 20-pin IDC connector pin-out differently.

IMPORTANT NOTE ON USING JTAG: The Sharp LH7A404 processor requires a rising edge on the processor wake-up signal to bring the processor from Cold Boot state to Run state. Therefore, in order to use JTAG operation on the LH7A404-11 Card Engine, one must consult their JTAG manufacturer to find when the JTAG device requires the processor to be in the Run state. If the JTAG device issues a reset to the processor, then the wake-up signal must transition from low to high to return to the Run state before the JTAG debugger may connect. The JTAG device may be able to connect to the processor while it is in Standby state, but will not be able to do anything that requires processor functioning until woken.

3.5 Power Management

3.5.1 System Power Supplies

In order to ensure a flexible design, the LH7A404-11 Card Engine was designed to have the following five power areas, 3.3V_uP_SDRAM, 3.3V, 3.3VA, 3.3V_WRLAN, and VCORE. All power areas are inputs to the card engine with the exception of 3.3V_WRLAN, which is an output from the card engine.

3.5.1.1 3.3V_uP_SDRAM

The 3.3V_uP_SDRAM input pins are connected to a 3.3V power supply with an optional backup battery. If the design is required to maintain SDRAM contents in a critical power situation (low battery, loss of power), the 3.3V_uP_SDRAM supply should be maintained above the minimum level at all costs (see Electrical Specifications section). Logic suggests using Standby mode to prepare the system for a critical power condition. In this way, the SDRAM is placed into self-refresh and processor is placed into the Standby state. Please note the description of Standby mode in this section below.

3.5.1.2 3.3V

The power nets connected to the 3.3V power plane handle the majority of the peripheral supply pins (digital) on the LH7A404-11 Card Engine. This supply must stay within the acceptable levels specified in the Electrical Specification section of this manual, unless experiencing power down or critical power conditions.

Under critical power conditions, Logic suggests notifying the system through the assertion of a Standby sequence first, and then powering this supply off.

3.5.1.3 3.3VA

The power nets connected to the 3.3VA power plane handles all peripheral supply pins (analog), but not the LH7A404 processor on the LH7A404-11 Card Engine. The 3.3VA supply must stay within the acceptable levels specified in the Electrical Specification section of this manual, unless powering down the board or under critical power conditions.
Under critical power conditions, Logic suggests first notifying the system through the assertion of a Standby sequence and then powering this supply off.

3.5.1.4 3.3V_WRLAN

This “power” supply net is an output from the card engine and is controlled through a registered bit in the on-board CPLD. For more details on this specific control bit, see the LH7A404 Card Engine IO Controller Interface Specification manual. Logic’s software BSP asserts this signal in order to properly manage power in the LAN91C111 Ethernet chip. This management does not, however, put the part in a low enough power state for many applications.

The custom application board should use the 3.3V_WRLAN output pin to supply the Ethernet impedance matching resistors with power. These resistors should not be connected to 3.3V directly or the entire Ethernet controller circuit on the card engine will try to power itself through the impedance matching resistors. Please see Logic’s schematics for the SDK or IDK reference designs for details.

IMPORTANT NOTE: The purpose of the 3.3V_WRLAN power plane on the card engine is to power the 91C111 chip separately and allow for a complete, but independent, shut down. Furthermore, the 3.3V_WRLAN output from the card engine is required to completely isolate the LAN circuit so that it is not back powered through the impedance matching resistors.

3.5.1.5 VCORE

The analog power pins on the LH7A404 are connected to the VCORE voltage with low-pass filtering. The VCORE input pins are connected to a 1.8V power supply with an optional backup battery. If the design is required to maintain SDRAM contents in a critical power situation (low battery, loss of power), the VCORE supply should be maintained above the minimum level at all costs (see Electrical Specifications section). Logic suggests using Standby mode to prepare the system for a critical power condition. In this way, the SDRAM is placed into self-refresh and the processor is placed into the Standby state. Please see the description of Standby mode later in this section.

3.5.2 System Power Management

Good power management design is important in any system development and embedded system design is no exception. In embedded system design, power management is typically one of the most complicated areas due to the dramatic effect it has on the product cost, performance, usability, and overall customer satisfaction. Many factors affect a power-efficient hardware design: power supply selection (efficiency), clocking design, IC and component selection, etc. The LH7A404-11 Card Engine was designed to keep these aspects in mind and provide maximum flexibility in software and system integration.

On the LH7A404 there are many different software configurations that drastically effect power consumption: microcontroller core clock frequency, microcontroller bus clock frequency, microcontroller peripheral clocks, microcontroller bus modes (asynchronous, synchronous, FastBus), microcontroller power management states (run, halt, standby), peripheral power states and modes, product user scenarios, interrupt handling, and display settings (resolution, backlight, refresh, bits per pixel, etc). These settings are typically initialized in the startup software routines and may be later modified in the operating system and application software. Information for these items can be found in the appropriate documents such as the LogicLoader™ User's Manual or appropriate BSP manual.

IMPORTANT NOTE: Most of the LH7A404-11 Card Engine hardware architecture was designed for low power battery operated applications. The Altera CPLD, on the LH7A404-11 Card Engine design, was chosen to optimize cost over power savings. If power-optimization is the primary goal of the design; please contact Logic for other design configurations in this area.

3.5.3 Peripherals

Most peripherals provide software programmable power states. Sometimes, however, these programmable power states may not be the best solution. The SMSC 91C111 controller, for example, has software programmable power states which may not be sufficient for some applications. In order to solve this problem, Logic has provided hardware to cut power to the 91C111 chip. Please see the appropriate data sheets and the LH7A404-11 Card Engine IO Controller Interface Specification for more information.

The LH7A404-11 Card Engine was designed to have the following five power areas, 3.3V_uP_SDRAM, 3.3V, 3.3V_WRLAN, 3.3VA, and VCORE for a flexible hardware design. See Figure 3.3 below.

Logic Net Name	Required Input VDC	Notes
3.3V_uP_SDRAM	3.3VDC	Connects to the Processor's 3.3-volt pins and the SDRAM. This net can be used for battery powered or bridge battery applications that require the processor and the SDRAM to refresh.
3.3V	3.3VDC	Connects to the digital peripherals on the Card Engine.
3.3VA	3.3VDC	Connects to the Audio Codec on the Card Engine to provide a clean analog plane. The user may choose not to provide a clean analog plane depending on their performance requirements.
VCORE	1.8V	Connects to the processor core voltage. See information on each specific processor for the VCORE voltage. Many processors require different VCORE voltages for different operating frequencies, temperatures, etc.
3.3V_WRLAN	3.3V (This Pin is an output, see section 3.5.1.4)	Provides power to the SMSC 91C111 processor from the 3.3V area. The power to the 3.3V_WRLAN area is controlled by the signal WRLAN_ENABLE from the CPLD. See the IO Controller Specification for controlling this signal.

IMPORTANT NOTE: Because the power management on the SMSC 91C111 is not suitable for many applications, the PMOS FET was added to control power input into the wired LAN.

Figure 3.4: Power Plane Diagram

3.5.4 Microcontroller

The LH7A404 processor power management's scheme was designed to be easy to use. There are three power management states provided in the LH7A404 microcontroller: RUN, STANDBY, and HALT. Please see below for descriptions from all three states and the LH7A404 Universal Microcontroller User's Guide for more details

3.5.4.1 Run Mode

Run is the LH7A404-11 Card Engine's normal operating stat in which both oscillator inputs and all clocks are hardware enabled. The LH7A404 can enter Run mode from either the Standby or Halt states. From the Standby state, Run can be accessed on three conditions: a rising-edge on the wakeup pin (the uP_WAKEUP signal), an exit from the Clock Set register (after a the clock divisor has been adjusted and the new clock output has stabilized), or the falling-edge of an interrupt (interrupts are active low). A Halt to Run transition occurs on the falling-edge of an interrupt (interrupts are active low), Power Fail, or on a user reset (see Soft Reset above).

IMPORTANT NOTE: Two seconds after a power on reset, a rising edge transition on the uP_WAKEUP signal is required to transition from Standby to Run mode. The uP_WAKEUP signal is pulled to 3.3V_uP_SDRAM on the Card Engine so a pushbutton tied to ground implementation can easily be used to provide the required low to high transition on the uP_WAKEUP signal. The SDK and IDK kits have example circuitry for the required uP_WAKEUP signal transition.

3.5.4.2 Standby Mode

Standby is the LH7A404 Card Engine's hardware power down mode, allowing for minimal power consumption. In this mode, only the 32.768 kHz clock input is enabled and the Real Time Clock and state controller are the only active functional blocks. Before all the clocks are turned off, however, the SDRAM is put into self-refresh mode, and maintains the contents of memory while in the low power state. Standby mode can only be entered after a system power-on or on a progression from the Run state. A Run to Standby transition occurs on a Power Fail, User Reset (Soft Reset), Write Clock Set (new clock divisors specified), or read of the STBY register.

3.5.4.3 Halt Mode

The Halt state is designed to reduce power consumption while the LH7A404 is waiting for an event such as a keyboard input. In this mode, although the processor clock is halted, the 14.7456 MHz oscillator input is enabled, thereby allowing software to specify the other active and inactive clocks. In this way, it is possible to maintain the LCD image yet reduce system-wide power usage at the same time. The only way to transition to the Halt state is on a read from the HALT register while in the Run state.

IMPORTANT NOTE: Although Halt consumes less power than Run mode, it consumes more power than the Standby Mode. Thus, on a power failure, the LH7A404 system will actually leave the Halt state and transition to the Standby state (the same thing occurs on an SW_nRESET.

3.6 ESD Considerations

The LH7A404-11 Card Engine was designed to interface to a customer's peripheral board. The Card Engine was designed to be low cost and adaptable to many different applications. The LH7A404-11 Card Engine does not provide any on-board ESD protection circuitry – this must be provided by the product it is used in. Logic has extensive experience in designing products with ESD requirements. Please contact Logic if you need any assistance in ESD design considerations.

4 Memory & I/O Mapping

4.1 SDRAM Memory Map

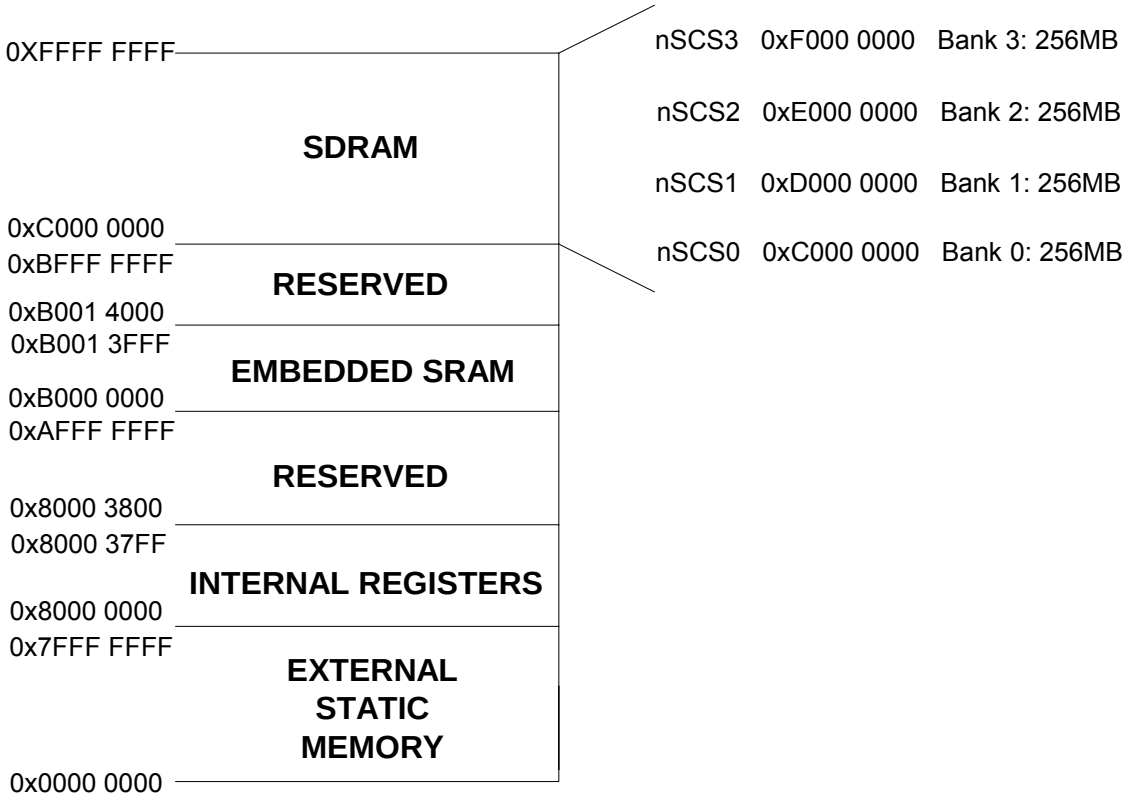


Figure 4.1: LH7A404 SDRAM Memory Map

4.2 External Static Memory Map

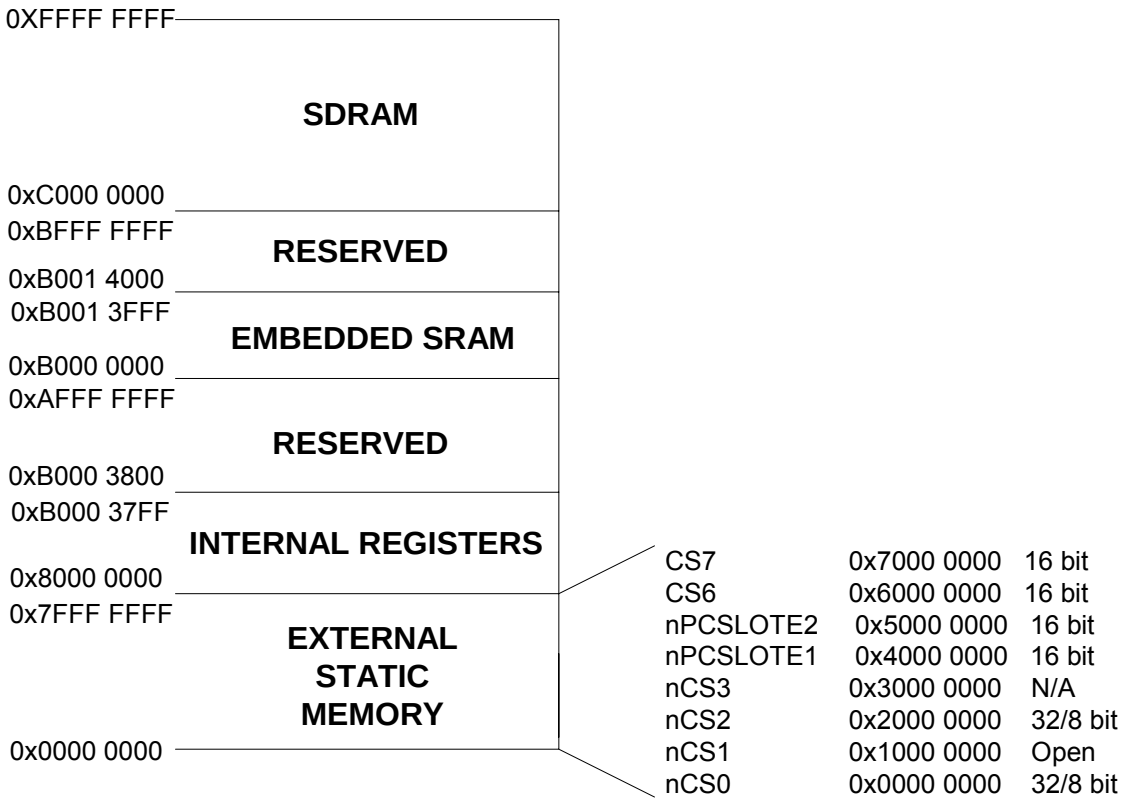


Figure 4.2: LH7A404 Static Memory Map

NOTE: The bit numbers refer to the bank width at reset. Banks 0 and 2 (nCS0 and nCS2) are 32-bits wide if flash is used as the boot device and 8-bits wide if an EEPROM is used as the boot device.

4.2.1 Card Engine Static Memory Map Description

The table below indicates what each bank of external static memory is being used for on the card engine.

Chip Select	Bank	Start Address	Memory Description
CS7	7	0x7000 0000	IO Controller Peripherals (Fast[1])
CS6	6	0x6000 0000	IO Controller Peripherals (Slow[1])
nPCSLOTE2	5	0x5000 0000	Used for PC Card Interface
nPCSLOTE1	4	0x4000 0000	Used for PC Card Interface
nCS3	3	0x3000 0000	Open[2]
nCS2	2	0x2000 0000	Boot Device (Flash or Off-Board)
nCS1	1	0x1000 0000	Video
nCS0	0	0x0000 0000	Boot Device (Flash or Off-Board)

Notes:
1. CPLD peripherals are components that get a decoded chip select from the CPLD. (i.e. CPLD memory mapped registers, onboard SMSC 91C111 Ethernet controller, etc... Please see the LH7A404-11 IO Controller Specification document for details.) These peripherals are separated into two different chip select banks, due to the difference in timing: slow and fast.
2. Chip Select 3 is multiplexed with the MultiMediaCard select signal.

4.2.2 Chip Select 6 (CS6) – CPLD Peripherals (slow timing)

The table below indicates how the CPLD decodes chip select 6. For more detailed information see the LH7A404-11 IO Controller Specification.

Chip Select	Memory Description	Address Range	Size
CS6	Reserved	0x6000 0000 – 0x601F FFFF	2MB
CS6	CF Chip Select	0x6020 0000 – 0x603F FFFF	2MB
CS6	ISA-like Bus Chip Select	0x6040 0000 – 0x605F FFFF	2MB
CS6	Reserved - On-Board Expansion	0x6060 0000 – 0x61FF FFFF	2MB (x13)
CS6	Reserved - Off-Board Expansion	0x6200 0000 – 0x62FF FFFF	1MB (x16)
CS6	Open - Available for User	0x6300 0000 – 0x63FF FFFF	1MB (x16)

4.2.3 Chip Select 5 (CS7) – CPLD Peripherals (fast timing)

The table below indicates how the CPLD decodes chip select 7. For more detailed information see the LH7A404-11 IO Controller Specification.

Address Range	Memory Block Description	Size
0x7000 0000 – 0x701F FFFF	Wired LAN Chip Select	2MB
0x7020 0000 – 0x703F FFFF	Card Engine Control Reg	2MB
0x7040 0000 – 0x705F FFFF	Reserved	2MB
0x7060 0000 – 0x707F FFFF	Reserved	2MB
0x7080 0000 – 0x709F FFFF	Reserved	2MB
0x70A0 0000 – 0x70BF FFFF	EEPROM SPI Reg	2MB
0x70C0 0000 – 0x70DF FFFF	Interrupt/Mask Reg	2MB
0x70E0 0000 – 0x70FF FFFF	Mode Reg	2MB
0x7100 0000 – 0x711F FFFF	FLASH Reg	2MB
0x7120 0000 – 0x713F FFFF	Power Management Reg	2MB
0x7140 0000 – 0x715F FFFF	IO Controller Code Revision Reg	2MB
0x7160 0000 – 0x717F FFFF	Extended GPIO Reg	2MB
0x7180 0000 – 0x719F FFFF	GPIO Data Reg	2MB
0x71A0 0000 – 0x71BF FFFF	GPIO Direction Reg	2MB
0x71C0 0000 – 0x71FF FFFF	Reserved - On-Board Expansion	2MB (X2)
0x7200 0000 – 0x72FF FFFF	Reserved - Off-Board Expansion	1MB (X16)
0x7300 0000 – 0x73FF FFFF	Open – Available for User	1MB (X16)

5 Pin Descriptions & Functions

IMPORTANT NOTE: The following pin descriptions and states are described after the initialization of the LogicLoader™ (bootloader). Many of the signals defined in the tables below can be configured as input or outputs – all GPIOs on the LH7A404 can be configured as either inputs or outputs – or active low/high, and have different functions. It is critical to review all signals in the final design (both electrical and software) to verify the necessary configuration (external pull ups/pull downs).

In addition, keep in mind that the following mode line numbers on the card engine do not necessarily line up with the mode line numbers on the processor.

5.1 J1C Connector SO-DIMM 144-Pin Descriptions

Pin #	Signal Name	I/O	Description
1	ETHER_RX(-)	I	This input pair receives 10/100 MB/s Manchester encoded data from the 10/100 BASE-T receive lines. Route as differential pair with ETHER_RX(+).
2	MSTR_nRST	I	Active Low. Driven low during power on in order to initiate a hard reset, erasing the contents of external memory. Refer to the reset description found in section 3.2.1 for more information on how this signal is driven. Every peripheral on the card engine with a reset line is reset with the assertion of this signal. Refer to LH7A404 processor datasheet for register states during or after power on reset. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor.
3	ETHER_RX(+)	I	This input pair receives 10/100 MB/s Manchester encoded data from the 10/100 BASE-T receive lines. Route as differential pair with ETHER_RX(-).
4	uP_SW_nRESET	I	Active Low. This signal initiates a soft reset (manual reset) – external memory contents are retained during reset. This pin is connected to the CPLD, please see LH7A404-11 Card Engine CPLD Interface Specification for detailed information on the use of the CPLD based reset. The SW_nRESET must be implemented in software in order to function properly. This signal is pulled up to 3.3V_uP_SDRAM through a 33K resistor.
5	ETHER_TX(-)	O	This output pair drives 10/100 Mb/s Manchester-encoded data to the 10/100 BASE-T transmit lines. Route as differential pair with ETHER_TX(+).
6	FAST_nMCS	O	Active Low. Buffered Chip select for area 7 of LH7A404-11 memory -- the "fast" peripheral chip select area. This signal is an output from the CPLD. Therefore, when the processor asserts the CS and does not decode an address that relates to the CPLD registers, it asserts FAST_nMCS.
7	ETHER_TX(+)	O	This output pair drives 10/100 Mb/s Manchester-encoded data to the 10/100 BASE-T transmit lines. Route as differential pair with ETHER_TX(-).
8	SLOW_nMCS	O	Active Low. Buffered chip select for area 6 of LH7A404-11 memory -- the “slow” peripheral chip select area. See memory map for details. This signal is an output from the CPLD. Therefore, when the processor asserts the CS and does not decode an address that relates to the CPLD registers, it asserts SLOW_nMCS.
9	DGND	I	Digital Ground (0V)
10	VIDEO_nMCS	O	Active Low. Buffered chip select for area 1 of LH7A404-11 memory. This is the "video" chip select area. This chip select is also capable of controlling additional external

			SDRAM. This is set to a 32-bit wide area and can be changed based on the user's needs. See memory map for details. This signal can not be used to select external SDRAM -- this processor has separate synchronous and asynchronous chip selects.
11	ACT_LED/LAN_LED1	O	Active Low open drain output. 24mA sink. This output indicates transmission or reception of frames or detection of a collision. This signal may be connected directly to an external LED.
12	BOOT_nMCS	O	Active Low. This signal is the buffered chip select for boot ROM in area 0 when uP_MODE3 is low. When uP_MODE3 is high, this signal is the buffered chip select for a specific memory mapped address in the slow chip select area of LH7A404-11 memory (8/16/32-bit wide area 2). See memory map for details.
13	LNK_LED/LAN_LED2	O	Active Low open drain output. 24mA sink. This output indicates valid link pulses. May be connected directly to an external LED.
14	nIOWR	O	Active Low. The ISA bus master or DMA controller drives the signal to communicate the presence of valid write data on the data bus. A peripheral may use this signal to latch the data in. See the LH7A404-11 CPLD Interface Specification for further details.
15	uP_nSTANDBY	I	Active Low. CPU power mode signal. A low nSTANDBY signal will cause the Card Engine to enter standby mode (hardware power down), where the contents of the SDRAM are placed in self-refresh and will be maintained. From standby, run is entered in response to a rising edge on wakeup, after an exit from CLKSET, or in response to an interrupt or fast interrupt falling edge (IRQ/FIQ – assuming interrupts are enabled). Software must be implemented in order for this signal to operate properly. This signal is pulled up to 3.3V_uP_SDRAM through a 33K resistor.
16	nIORD	O	Active Low. This signal is driven by the ISA bus master or DMA controller to request an I/O resource to drive data onto the data bus during the cycle. See the LH7A404-11 CPLD Interface Specification for further details.
17	DGND	I	Digital Ground (0V)
18	3.3V_WRLAN	O	Power Supply (3.3V) from the 10/100 wired LAN circuit. This pin is used to power the impedance matching resistor network on the Ethernet's TX and RX lines. It should not be connected to anything else. It may be shut down when appropriate (software controlled to cut power off to the wired LAN circuit).
19	3.3V	I	Power Supply (3.3V)
20	BALE	O	Active High. This signal is driven high to indicate when the MA<19:0> signal lines are valid or the processor data bus is in use. See the LH7A404-11 CPLD Interface Specification for further details.
21	uP_WAKEUP	I	Triggers on rising edge. This CPU power mode signal causes run mode to be entered from standby mode. This signal is pulled up to 3.3V_uP_SDRAM through a 33K resistor. The onboard CPLD divides down a clock to toggle this pin after a Power On Reset. This signal will automatically wake up the processor and put it to run state. If the user desires to go into a low power state at a later time, the Auto Wakeup feature must be disabled to stop the WAKEUP pin from being toggled. The signal can be stopped by writing to a register in the onboard CPLD. Refer to the IO Controller specification for further information.

22	nCHRDY	O	Active Low. The I/O channel ready signal line serves to drive the asynchronous ready signal on the WIRED LAN circuit low when additional cycle time is required. See the LH7A404-11 CPLD Interface Specification for further details. This signal is pulled up to 3.3V through a 1K resistor.
23	uP_nIRQD	I	Active Low. Dedicated hardware interrupt on LH7A404-11. May also be configured as a GPIO pin (input only). This signal is pulled up to 3.3V_uP_SDRAM through a 33K resistor.
24	uP_TEST1	I	This is connected to Test Mode Pin 0 on the LH7A404 processor. This signal needs to be pulled high for normal operation and low for JTAG use. Please see the section on Operating Modes in the LH7A404 technical datasheet for detailed operation. This signal is pulled up to 3.3V_uP_SDRAM through a 33K resistor.
25	uP_nIRQC	I	Active Low. Dedicated hardware interrupt on LH7A404-11. May also be configured as a GPIO pin (input only). This signal is pulled up to 3.3V_uP_SDRAM through a 33K resistor, in addition to an internal pull-up.
26	uP_TEST2	I	This is connected to Test Mode Pin 1 on the LH7A404 processor. This signal needs to be pulled high for both normal operation and JTAG use. For more information, please see the section on Operating Modes in the LH7A404 technical datasheet for detailed operation. This signal is pulled up to 3.3V_uP_SDRAM through a 33K resistor.
27	uP_nIRQB	I	Active Low. Dedicated hardware interrupt on LH7A404-11. May also be configured as a GPIO pin (input only). This signal is pulled up to 3.3V_uP_SDRAM through a 33K resistor, in addition to an internal pull-up.
28	MSTR_nRST	I	Active Low. Driven low during power on in order to initiate a hard reset, erasing the contents of external memory. Refer to the reset description found in section 3.2.1 for more information on how this signal is driven. Every peripheral on the card engine with a reset line is reset with the assertion of this signal. Refer to LH7A404 processor datasheet for register states during or after power on reset. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor.
29	uP_nIRQA	I	Active Low. Dedicated hardware interrupt on LH7A404-11. May also be configured as a GPIO pin (input only). This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor.
30	uP_TMS	I	JTAG Test Mode Select Input. May leave unconnected if not using the JTAG port. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor.
31		NC	No internal connection (not implemented on the LH7A404-11)
32	uP_TDO	O	JTAG Test Data Serial Output. Leave unconnected when JTAG port is not in use. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor.
33		NC	No internal connection (not implemented on the LH7A404-11)
34	uP_TDI	I	JTAG Test Serial Data Input. May leave unconnected if not using the JTAG port. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor.
35		NC	No internal connection (not implemented on the LH7A404-11)
36	uP_TCK	I	JTAG Test Clock Input. May leave unconnected if not using the JTAG port. This signal is pulled up to 3.3V_uP_SDRAM through a 10K resistor.
37	uP_nWAIT	I	Active low. This is the processor's wait signal. This signal is driven low by the ISA I/O Ready signal in the CPLD. For more information, see the LH7A404 IO Controller Specification. This signal is pulled up to 3.3V_uP_SDRAM through a 1K resistor.

<table>
<tr><td>38</td><td>uP_MODE3</td><td>O</td><td>Boot select signal (0 = external boot device, 1 = on-board flash). This is accomplished in the CPLD: if signal uP_MODE3 is high, then flash_nCS = uP_nCS0 and BOOT_nCS = uP_nCS2 and vice-versa if uP_MODE3 is low. This defaults to the on-board flash if left unconnected (pulled to 3.3V through a 10K resistor).</td></tr>
<tr><td>39</td><td>uP_UARTA_RTS</td><td>O</td><td>This is a GPIO signal that is used to implement the Ready to Send line for the UART2 interface.</td></tr>
<tr><td>40</td><td>uP_MODE2</td><td>O</td><td>The LH7A404 processor only supports Little Endian memory operations. On development kits by Logic Product Development, the generic use of this pin is an Endian setting (0 = big endian, 1 = little endian). This defaults to high (little endian) if left unconnected (pulled to 3.3V through a 10K resistor). This pin can also be used as a General Purpose input and read from the CPLD register.</td></tr>
<tr><td>41</td><td>uP_UARTA_CTS</td><td>I</td><td>UART 2 clear to send on the LH7A404-11.</td></tr>
<tr><td>42</td><td>uP_MODE1</td><td>O</td><td><table><tr><td>Mode1</td><td>Mode0</td><td>Bus Width</td></tr><tr><td>0</td><td>0</td><td>8-bit</td></tr><tr><td>0</td><td>1</td><td>16-bit</td></tr><tr><td>1</td><td>0</td><td>32-bit</td></tr><tr><td>1</td><td>1</td><td>32-bit</td></tr></table>Mode1 defaults to high if left unconnected (pulled to 3.3V_uP_SDRAM through a 33K resistor).</td></tr>
<tr><td>43</td><td>uP_UARTA_TX</td><td>O</td><td>UART 2 transmit output signal. Internally pulled up on the LH7A404 processor.</td></tr>
<tr><td>44</td><td>uP_MODE0</td><td>O</td><td><table><tr><td>Mode1</td><td>Mode0</td><td>Bus Width</td></tr><tr><td>0</td><td>0</td><td>8-bit</td></tr><tr><td>0</td><td>1</td><td>16-bit</td></tr><tr><td>1</td><td>0</td><td>32-bit</td></tr><tr><td>1</td><td>1</td><td>32-bit</td></tr></table>Mode0 defaults to low if left unconnected (pulled to digital GND through a 33K resistor).</td></tr>
<tr><td>45</td><td>uP_UARTA_RX</td><td>I</td><td>UART 2 receive input signal on the LH7A404.</td></tr>
<tr><td>46</td><td>uP_DREQ1</td><td>O</td><td>The DMA Request 0 line. This signal is pulled to digital GND through a 33K resistor.</td></tr>
<tr><td>47</td><td></td><td>NC</td><td>No internal connection (not implemented on the LH7A404-11)</td></tr>
<tr><td>48</td><td>uP_DREQ0</td><td>O</td><td>The DMA Request 1 line. This signal is pulled to digital GND through a 33K resistor.</td></tr>
<tr><td>49</td><td>uP_UARTA_DSR</td><td>O</td><td>UART 2 data set ready on the LH7A404-11.</td></tr>
<tr><td>50</td><td></td><td>NC</td><td>No internal connection (not implemented on the LH7A404-11)</td></tr>
<tr><td>51</td><td>nSUSPEND</td><td>I</td><td>Active low. This signal is one of the CPLD interrupts and is used to suspend LH7A404 operations. This pin is connected directly to the CPLD and it is pulled up to 3.3V by a 10k resistor. Software is required for proper suspend operation.</td></tr>
<tr><td>52</td><td></td><td>NC</td><td>No internal connection (not implemented on the LH7A404-11)</td></tr>
<tr><td>53</td><td>uP_AUX_CLK</td><td>O</td><td>This signal is a programmable auxiliary clock that is set to 14.7456 (max value) by default.</td></tr>
<tr><td>54</td><td>uP_DACK1</td><td>O</td><td>The DMA Acknowledge 0 line. This signal is pulled to digital GND through a 33K resistor.</td></tr>
<tr><td>55</td><td>DGND</td><td>I</td><td>Digital Ground (0V)</td></tr>
<tr><td>56</td><td>uP_DACKO</td><td>O</td><td>The DMA Acknowledge 1 line. This signal is pulled to digital GND through a 33K resistor.</td></tr>
<tr><td>57</td><td>VCORE</td><td>I</td><td>CPU core voltage supply (on during low power, uP_SW_Reset). VCORE is fixed at 1.8V.</td></tr>
<tr><td>58</td><td>VCORE</td><td>I</td><td>CPU core voltage supply (on during low power, uP_SW_Reset). VCORE is fixed at 1.8V.</td></tr>
<tr><td>59</td><td>VCORE</td><td>I</td><td>CPU core voltage supply (on during low power, uP_SW_Reset). VCORE is fixed at 1.8V.</td></tr>
<tr><td>60</td><td>VCORE</td><td>I</td><td>CPU core voltage supply (on during low power,</td></tr>
</table>

			uP_SW_Reset). VCORE is fixed at 1.8V.
61	3.3V_uP_SDRAM	I	uP and SDRAM Power Supply (3.3 V) (on during low power, uP_SW_Reset). Recommend leaving this supply as the only powered supply during Standby power down mode.
62	3.3V_uP_SDRAM	I	uP and SDRAM Power Supply (3.3 V) (on during low power, uP_SW_Reset). Recommend leaving this supply as the only powered supply during Standby power down mode.
63	3.3V_uP_SDRAM	I	uP and SDRAM Power Supply (3.3 V) (on during low power, uP_SW_Reset). Recommend leaving this supply as the only powered supply during Standby power down mode.
64	3.3V_uP_SDRAM	I	uP and SDRAM Power Supply (3.3 V) (on during low power, uP_SW_Reset). Recommend leaving this supply as the only powered supply during Standby power down mode.
65	uP_SPI_FRM	O	Software controlled SPI framing signal. This signal may be used by application software to frame SPI data transmission or reception. This signal is pulled up to 3.3V through a 33K resistor.
66	uP_BUS_CLK	O	Synchronous Memory Clock. This clock operates at 100MHz and is connected to the SDRAM as well as the CPLD.
67	uP_SPI_TX	O	This output transmits synchronous SPI data. This signal is pulled down to digital GND through a 33K resistor.
68	DGND	I	Digital Ground (0V)
69	uP_SPI_RX	I	This input receives synchronous SPI data. This signal is pulled down to digital GND through a 33K resistor.
70	uP_nRAS	O	Synchronous Memory Row Address Strobe Signal. This signal is used in synchronizing all SDRAM into row addressing mode.
71	uP_SPI_SCK	O	SPI clock signal. SPI transmit/receive data is valid on the rising edge of this clock (data is output from one falling edge to the next and clocked in on the rising edge). This signal is pulled-down internally on the LH7A404 processor
72	uP_nCAS	O	Synchronous Memory Row Address Strobe Signal. This signal is used in synchronizing all SDRAM into column addressing mode.
73	uP_MD0	I/O	Buffered Data Bus bit 0.
74	uP_nMWE3	O	Active low. Buffered write enable for buffered data bus bits 16->31 to the Flash.
75	uP_MD1	I/O	Buffered Data Bus bit 1.
76	uP_nMWE2	O	This is the buffered Byte Lane Enable 2 signal. This enable is supplied for off-board use in order to implement memory devices of varying widths.
77	uP_MD2	I/O	Buffered Data Bus bit 2.
78	uP_nMWE1	O	This is the buffered Byte Lane Enable 1 signal. This enable is supplied for off-board use in order to implement memory devices of varying widths.
79	uP_MD3	I/O	Buffered Data Bus bit 3.
80	uP_nMWE0	O	Active low. Buffered write enable for buffered data bus bits 0->15 to the flash.
81	uP_MD4	I/O	Buffered Data Bus bit 4.
82	uP_nMWR	O	Active low. This buffered signal is the processor's write enable line.
83	uP_MD5	I/O	Buffered Data Bus bit 5.
84	uP_nMRD	O	Active low. This buffered signal is the read strobe that latches data output from external peripherals.
85	uP_MD6	I/O	Buffered Data Bus bit 6.
86	uP_MA27	O	Buffered Address Bus bit 27.
87	uP_MD7	I/O	Buffered Data Bus bit 7.

88	uP_MA26	O	Buffered Address Bus bit 26.
89	DGND	I	Digital Ground (0V)
90	uP_MA0	O	Buffered Address Bus bit 0.
91	uP_MD8	I/O	Buffered Data Bus bit 8.
92	uP_MA1	O	Buffered Address Bus bit 1.
93	uP_MD9	I/O	Buffered Data Bus bit 9.
94	uP_MA2	O	Buffered Address Bus bit 2.
95	uP_MD10	I/O	Buffered Data Bus bit 10.
96	uP_MA3	O	Buffered Address Bus bit 3.
97	uP_MD11	I/O	Buffered Data Bus bit 11.
98	uP_MA4	O	Buffered Address Bus bit 4.
99	uP_MD12	I/O	Buffered Data Bus bit 12.
100	uP_MA5	O	Buffered Address Bus bit 5.
101	uP_MD13	I/O	Buffered Data Bus bit 13.
102	uP_MA6	O	Buffered Address Bus bit 6.
103	uP_MD14	I/O	Buffered Data Bus bit 14.
104	uP_MA7	O	Buffered Address Bus bit 7.
105	uP_MD15	I/O	Buffered Data Bus bit 15.
106	uP_MA8	O	Buffered Address Bus bit 8.
107	3.3V	I	Power Supply (3.3V)
108	uP_MA9	O	Buffered Address Bus bit 9.
109	DGND	I	Digital Ground (0V)
110	uP_MA10	O	Buffered Address Bus bit 10.
111	uP_MD16	I/O	Buffered Data Bus bit 16.
112	uP_MA11	O	Buffered Address Bus bit 11.
113	uP_MD17	I/O	Buffered Data Bus bit 17.
114	uP_MA12	O	Buffered Address Bus bit 12.
115	uP_MD18	I/O	Buffered Data Bus bit 18.
116	uP_MA13	O	Buffered Address Bus bit 13.
117	uP_MD19	I/O	Buffered Data Bus bit 19.
118	uP_MA14	O	Buffered Address Bus bit 14.
119	uP_MD20	I/O	Buffered Data Bus bit 20.
120	uP_MA15	O	Buffered Address Bus bit 15.
121	uP_MD21	I/O	Buffered Data Bus bit 21.
122	uP_MA16	O	Buffered Address Bus bit 16.
123	uP_MD22	I/O	Buffered Data Bus bit 22.
124	uP_MA17	O	Buffered Address Bus bit 17.
125	uP_MD23	I/O	Buffered Data Bus bit 23.
126	uP_MA18	O	Buffered Address Bus bit 18.
127	DGND	I	Digital Ground (0V)
128	uP_MA19	I/O	Buffered Address Bus bit 19.
129	uP_MD24	I/O	Buffered Data Bus bit 24.
130	uP_MA20	O	Buffered Address Bus bit 20.
131	uP_MD25	I/O	Buffered Data Bus bit 25.
132	uP_MA21	O	Buffered Address Bus bit 21.
133	uP_MD26	I/O	Buffered Data Bus bit 26.
134	uP_MA22	O	Buffered Address Bus bit 22.
135	uP_MD27	I/O	Buffered Data Bus bit 27.

136	uP_MA23	O	Buffered Address Bus bit 23.
137	uP_MD28	I/O	Buffered Data Bus bit 28.
138	uP_MA24	O	Buffered Address Bus bit 24.
139	uP_MD29	I/O	Buffered Data Bus bit 29.
140	uP_MA25	O	Buffered Address Bus bit 25.
141	uP_MD30	I/O	Buffered Data Bus bit 30.
142	nAEN	O	Active low. Address Enable, this ISA signal is used to enable ISA-like devices.
143	uP_MD31	I/O	Buffered Data Bus bit 31.
144	3.3V	I	Power Supply (3.3V)

5.2 J1A Expansion Connector Pin Descriptions

Pin #	Signal Name	I/O	Description
1	LCD_VSYNC - LCD_SPS	O	LCD VSYNC (TFT Signal).
2	LCD_HSYNC - LCD_HRLP	O	LCD HSYNC (TFT Signal).
3	LCD_DCLK	O	LCD Panel Data Clock
4	LCD_DON	O	This is a GPIO signal that is used to implement the display on line for the LCD interface.
5	LCD_MDISP	O	LCD enable signal (TFT signal).
6	LCD_VEEEN	O	Active high. This signal is the enable for the LCD panel Vee. It is controlled in the CPLD; see the LH7A404-11 CPLD Interface Specification for further details.
7	LCD_VDDEN	O	Active high. This signal is the LCD panel Vcc enable.
8	LCD_CLK_RETURN	I	This is the external clock input line for LCD controller.
9	DGND	I	Digital Ground (0V)
10	LCD_CLS	O	LCDCLS Signal Output (Row Driver Clock)– This signal is only used with a HR-TFT interface.
11	LCD_VSYNC - LCD_SPS	O	LCD VSYNC (TFT Signal).
12	LCD_PSAVE	O	LCDPS Signal Output (Power Save)–This signal is only used with a HR-TFT interface.
13 (+)	LCD_SPL	O	LCDSPL Signal Output (Start Pulse Left) – This signal is only used with the HR-TFT interface. **NOTE:** This signal is only used when the jumper is connected to the positive terminal.
13 (-)	LCD_SPR	O	LCDSPR Signal Output (Start Pulse Right) – This signal is only used with the HR-TFT interface. **NOTE:** This signal is only used when the jumper is connected to the negative terminal.
14	LCD_HSYNC - LCD_HRLP	O	LCD HSYNC (TFT Signal).
15	LCD_MOD	O	MOD signal used by the row driver (TFT signal).
16	LCD_REV	O	LCDREV Signal Output (Grey Scale Voltage Reverse) – This signal is only used with the HR-TFT interface.
17	uP_STATUS_1	O	This signal is attached to GPIO on the processor. It can be used with BoLo/ LoLo, and also to debug code using LED's on the SDK/IDK.
18	uP_STATUS_2	O	This signal is attached to GPIO on the processor. It can be used with BoLo/ LoLo, and also to debug code using LED's on the SDK/IDK.
19	uP_AC97_BITCLK	O	Clock input from an AC97 compliant audio codec. This signal is pulled down to digital GND through a 33K resistor.
20	uP_AC97_nRESET	O	AC97 reset line to an AC97 compliant audio codec. This signal is pulled up to 3.3V through a 33K resistor.
21	uP_AC97_SYNC	O	This signal is the AC97 sync output to an AC97 compliant audio codec. The codec Frequency is set on codec to be 48Khz, while the default frequency for the sync is set up to be 2.9491Mhz (14.7456MHz / 5) on the processor.
22	uP_AC97_SD_IN	I	This signal is the AC97 output from the processor to the AC97 compliant audio codec. This signal is pulled down to digital GND through a 33K resistor.
23	uP_AC97_SD_OUT	O	This signal is the AC97 input from the processor to the AC97 compliant audio codec.
24	DGND	I	Digital Ground (0V)
25	uP_A/D1	I	This signal is the input to channel 4 of the Processor's 10-bit A/D converter.
26	uP_A/D2	I	This signal is the input to channel 5 of the Processor's 10-bit A/D converter.
27	AGND	I	Analog Ground (0V)
28	MFP39 - uP_A/D3	I	This signal is the input to channel 6 of the Processor's 10-bit A/D converter.

29	MFP40 - uP_A/D4	I	This signal is the input to channel 7 of the Processor's 10-bit A/D converter.
30	3.3VA	I	Analog Power Supply (3.3V)
31	CODEC_INL	I	Left channel stereo line input of the audio codec.
32	CODEC_INR	I	Right channel stereo line input of the audio codec.
33	CODEC_OUTL	O	Left stereo mixer-channel line output. Please see the Wolfson #WM9708 AC97 Revision 2.1 Audio Codec Technical Datasheet for more details.
34	CODEC_OUTR	O	Right stereo mixer-channel line output. Please see the Wolfson #WM9708 AC97 Revision 2.1 Audio Codec Technical Datasheet for more details.
35	AGND	I	Analog Ground (0V)
36	TOUCH_LEFT	I	This is the Y+ position input to the four-wire resistive touch screen controller.
37	TOUCH_RIGHT	I	This is the Y- position input to the four-wire resistive touch screen controller.
38	TOUCH_BOTTOM	I	This is the X+ position input to the four-wire resistive touch screen controller.
39	TOUCH_TOP	I	This is the X- position input to the four-wire resistive touch screen controller.
40	3.3VA	I	Analog Power Supply (3.3V)
41	R0	O	The LCD data bus used to transmit data to the LCD module. Note that R0 is an intensity bit for the LCD display and therefore is connected to the other intensity bits, B0 and G0, which are connected to LCD_D15 on the processor
42	R1	O	The LCD data bus used to transmit data to the LCD module. RED 1 is connected to LCD_D0.
43	R2	O	The LCD data bus used to transmit data to the LCD module. RED 2 is connected to LCD_D1.
44	DGND	I	Digital Ground (0V)
45	R3	O	The LCD data bus used to transmit data to the LCD module. RED 3 is connected to LCD_D2.
46	R4	O	The LCD data bus used to transmit data to the LCD module. RED 4 is connected to LCD_D3.
47	R5	O	The LCD data bus used to transmit data to the LCD module. RED 5 is connected to LCD_D4.
48	G0	O	The LCD data bus used to transmit data to the LCD module. Note that G0 is an intensity bit for the LCD display and therefore is connected to the other intensity bits, B0 and R0, which are connected to LCD_D15 on the processor
49	G1	O	The LCD data bus used to transmit data to the LCD module. GREEN 1 is connected to LCD_D5.
50	G2	O	The LCD data bus used to transmit data to the LCD module. GREEN 2 is connected to LCD_D6.
51	G3	O	The LCD data bus used to transmit data to the LCD module. GREEN 3 is connected to LCD_D7.
52	G4	O	The LCD data bus used to transmit data to the LCD module. GREEN 4 is connected to LCD_D8.
53	G5	O	The LCD data bus used to transmit data to the LCD module. GREEN 5 is connected to LCD_D9.
54	B0	O	The LCD data bus used to transmit data to the LCD module. Note that B0 is an intensity bit for the LCD display and therefore is tied to the other intensity bits, G0 and R0, which are connected to LCD_D15 on the processor.
55	DGND	I	Digital Ground (0V)
56	B1	O	The LCD data bus used to transmit data to the LCD module. BLUE 1 is connected to LCD_D10.
57	B2	O	The LCD data bus used to transmit data to the LCD module. BLUE 2 is connected to LCD_D11.
58	B3	O	The LCD data bus used to transmit data to the LCD module. BLUE 3 is connected to LCD_D12.
59	B4	O	The LCD data bus used to transmit data to the LCD module. BLUE 4 is connected to LCD_D13.
60	B5	O	The LCD data bus used to transmit data to the LCD module. BLUE 5 is connected to LCD_D14.

61	CF_nCE	O	Active low. This signal is the chip/card select for the memory-only CF card. It indicates a word read/write to the card. See the LH7A404-11 CPLD Interface Specification for further details.
62	uP_PCC_RDYA	I	This signal is the PC Card ready signal input for a 2nd PCMCIA slot when 2 devices are used. This signal has a 33K pull up.
63	CPLD_GPIO_1	O	This signal is a general purpose output, which in this case, is used to drive the GPIO LED on the application board (such as the SDK). For more information on how this signal is driven, see the LH7A404-11 CPLD Interface Specification .
64	CPLD_GPIO_2	I/O	This signal is a general purpose I/O. It is controlled by a memory-mapped address in the CPLD. See the LH7A404-11 CPLD Interface Specification for further details.
65	uP_USB2_OVR_CRNT	O	Active high. This is the data carrier detect signal for the second USB port. It is used to determine whether or not the USB interface is currently in use.
66	DGND	I	Digital Ground (0V)
67	uP_USB1_OVR_CRNT	I	Active high. This is the data carrier detect signal for the main USB port. It is used to determine whether or not the USB interface is currently in use.
68	uP_USB2_PWR_EN	O	Active high. Enables power supply for USB port 2.
69	uP_USB1_PWR_EN	O	Active high. Enables power supply for USB port 1.
70	uP_USB2_M	I/O	USB port 2 data I/O minus. Route as a differential pair with uP_USB2_P.
71	uP_USB2_P	I/O	USB port 2 data I/O plus. Route as a differential pair with uP_USB2_M.
72	uP_USB1_M	I/O	USB port 1 data I/O minus. Route as a differential pair with uP_USB1_P.
73	uP_USB1_P	I/O	USB port 1 data I/O plus. Route as a differential pair with uP_USB1_M.
74	BUFF_nOE	I	Active low. This signal is the output enable for all five buffers on the card engine. This signal is pulled up to 3.3V through a 10K resistor in order to ensure the buffers are tri-stated upon powering up the card engine. When low, the buffers are active. See the LH7A404-11 CPLD Interface Specification for further details on how this signal is driven.
75	BUFF_DIR_ADDRESS	O	The BUFF_DIR_ADDRESS is high for the A404 card engine. Check with Logic for updated information.
76	BUFF_DIR_DATA	I	Active high. Controls the direction of the data lines through the two data bus buffers. When low, the data lines are driven out from the processor (write cycle). When high, the data lines are driven in to the processor (read cycle). See the LH7A404-11 CPLD Interface Specification for further details.
77	DGND	I	Digital Ground (0V)
78	MIC_IN	I	This signal is the microphone input to the AC97 compliant audio codec. Please see the Wolfson #WM9708 AC97 Revision 2.1 Audio Codec Technical Datasheet for more details.
79	POWER_SENSE1	O	These two pins are used to set the core voltage of the card engine. Please reference the ZOOM SDK or IDK reference schematics for details on implementation if the design may require support for different card engines.
80	POWER_SENSE2	O	These two pins are used to set the core voltage of the card engine. Please reference the ZOOM SDK or IDK reference schematics for details on implementation if the design may require support for different card engines.

5.3 J1B Expansion Connector Pin Description

Pin #	Signal Name	I/O	Description
1	CPLD_TCK	I	This is the test clock input for the CPLD JTAG port. It is used for reprogramming the CPLD. If CPLD_JTAG_nOE is driven low, in the field CPLD programming updates are possible.
2	CPLD_TDO	O	This input transmits data out of the CPLD JTAG port. It is used for reprogramming the CPLD. If CPLD_JTAG_nOE is driven low, in the field CPLD programming updates are possible.
3	CPLD_TMS	I	This input indicates the mode of CPLD JTAG port. It is used for reprogramming the CPLD. If CPLD_JTAG_nOE is driven low, in the field CPLD programming updates are possible.
4	CPLD_TDI	I	This input receives data on the CPLD JTAG port. It is used for reprogramming the CPLD. If CPLD_JTAG_nOE is driven low, in the field CPLD programming updates are possible.
5	uP_PCC_nOE	O	This signal is PC Card Output Enable, Attribute, and Common Memory space read control.
6	uP_PCC_nWE	O	This signal is for PC Card Enable, Attribute and Common Memory space write control.
7	uP_PCC_nIORD	O	This signal is for PC Card IO Read Output.
8	uP_PCC_nIOWR	O	This signal is for PC Card IO Write Output.
9	DGND	I	Digital Ground (0V)
10	uP_PCC_RESET	O	This signal is PC Card Reset Card 1. This signal is pulled up to 3.3V_uP_SDRAM through a 33K resistor.
11	uP_PCC_nCE1B	O	This signal is PC Card Enable 1 and is used with uP_PCC_nCE2B to decode low and high byte accesses for slot two only.
12	uP_PCC_nCE2B	O	This signal is PC Card Enable 2 and is used with uP_PCC_nCE1B to decode low and high byte accesses for slot two only.
13	uP_PCC_nIOIS16	O	Active low. PCMCIA IOIS16 signal. When low, this specifies that either a 16-bit IO card or a write-protected memory-only card is being used. This signal is pulled up to 3.3V_uP_SDRAM through a 33K resistor.
14	uP_PCC_RDYB	I	This is the PC Card ready input for slot one in dual card mode. This signal is pulled up to 3.3V_uP_SDRAM through a 33K resistor.
15	uP_PCC_nWAIT	I	This is the PC Card wait signal input in dual card mode. This signal is pulled up to 3.3V_uP_SDRAM through a 33K resistor.
16	uP_PCC_BVD2	I	This signal is the Battery Sense 2 signal and is connected to GPIO Port A bit 6.
17	uP_PCC_BVD1	I	This signal is the Battery Sense 1 signal and is connected to GPIO Port A bit 7.
18	uP_PCC_nCD2	I	This signal is connected to GPIO Port A bit 3. It can be used to sense the Card Detect input 2. The processor should be interrupted when this signal goes low. This signal is pulled up to 3.3V_uP_SDRAM through a 33K resistor.
19	uP_PCC_nCD1	I	This signal is connected to GPIO Port H bit 7. It can be used to sense the Card Detect input 1. The processor should be interrupted when this signal goes low. This signal is pulled up to 3.3V_uP_SDRAM through a 33K resistor.
20	uP_PCC_nREG	O	This signal is for PC Card Register Memory Accesses.
21	DGND	I	Digital Ground (0V)
22	uP_PCC_VS1	I	This is the PC Card Voltage Sense 1 signal.
23	uP_PCC_VS2	I	This is the PC Card Voltage Sense 2 signal.

24	uP_PCC_nDRV	O	This is the PC Card drive output signal. This signal is pulled up to 3.3V through a 33K resistor.
25	uP_PCC_PCDIR	O	This signal is used for PC Card data direction.
26	uP_DQM3	O	This signal is connected to UDQM pin on a SDRAM chip to enable uP_D[24:32].
27	uP_DQM2	O	This signal is connected to LDQM pin on a SDRAM chip to enable uP_D[16:23].
28	uP_DQM1	O	This signal is connected to UDQM pin on a SDRAM chip to enable uP_D[8:15].
29	uP_DQM0	O	This signal is connected to LDQM pin on a SDRAM chip to enable uP_D[0:7].
30	uP_IRTX	O	This is the IrDA Transmit signal, which is used for the Infrared Mode on UARTC.
31	uP_IRRX	I	This is the IrDA Receive signal, which is used for the Infrared Mode on UARTC.
32	DGND	I	Digital Ground (0V)
33	MFP1	O	See J1B Jumper Table Below.
34	MFP2	O	See J1B Jumper Table Below.
35	MFP3	O	See J1B Jumper Table Below.
36	MFP4	O	See J1B Jumper Table Below.
37	MFP5	O	See J1B Jumper Table Below.
38	MFP6	O	See J1B Jumper Table Below.
39	MFP7	O	See J1B Jumper Table Below.
40	MFP8	O	See J1B Jumper Table Below.
41	uP_UARTB_TX	O	UART 3 transmit output signal on the LH7A404-11. This signal is internally pulled-down on the LH7A404 if UART 3 is enabled.
42	uP_UARTB_RX	I	UART 3 receive input signal on the LH7A404-11.
43	uP_UARTB_CTS	O	UART 3 clear to send on the LH7A404-11.
44	DGND	I	Digital Ground (0V)
45	uP_UARTB_	O	UART 3 request to send on the LH7A404-11.
46	uP_UARTC_TX	O	UART 1 transmit output signal on the LH7A40410.
47	uP_UARTC_RX	I	UART 1 receive input signal on the LH7A404-11.
48	MFP9	O	See J1B Jumper Table Below.
49	MFP10	I/O	See J1B Jumper Table Below.
50	MFP11	O	See J1B Jumper Table Below.
51	MFP12	O	See J1B Jumper Table Below.
52	MFP13	O	See J1B Jumper Table Below.
53	MFP14	O	See J1B Jumper Table Below.
54	MFP15	O	See J1B Jumper Table Below.
55	DGND	I	Digital Ground (0V)
56	MFP16	O	See J1B Jumper Table Below.
57	MFP17	O	See J1B Jumper Table Below.
58	MFP18	O	See J1B Jumper Table Below.
59	MFP19	O	See J1B Jumper Table Below.
60	MFP20	I/O	See J1B Jumper Table Below.
61	MFP21	O	See J1B Jumper Table Below.
62	MFP22	O	See J1B Jumper Table Below.
63	MFP23 - uP_BMICLK - PB7	I/O	This signal is the Smart Battery Clock.
64	MFP24 - uP_BMISW - BMIIO - PB6	I/O	This signal is the Smart Battery Single Wire data line.
65	MFP25 - uP_nBATCHG	I/O	This is the Battery Charge signal. This signal is pulled up to 3.3V through a 33K resistor.
66	DGND	I	Digital Ground (0V)

67	MFP26 - uP_BATOK	I/O	This is the Battery OK signal. When the board is not plugged into external power, a transition to the run state may not occur unless a valid battery is present and the BATOK signal is high. This signal is pulled up to 3.3V through a 10K resistor.
68	MFP27 - uP_PWM1	I/O	DC-DC Converter 1 Output (Pulse Width Modulated)
69	MFP28 - uP_nMCS2	I/O	Active low. This is the buffered Chip Select 2 signal for off-board use.
70	MFP29 – uP_SDCKE	I/O	This signal is the processors SDKE signal which is used for accessing external SDRAM.
71	MFP30 - uP_nSDCS2	I/O	Active low. This signal is the processor's Synchronous Memory Chip Select 2.
72	MFP31 - uP_nSDCS1	I/O	Active low. This signal is the processor's Synchronous Memory Chip Select 1.
73	MFP32 - uP_nEXTPWR	I/O	Active low. This is the Power Supply signal. When the board is plugged into external power, this signal is asserted and the card engine is allow to transition to the run state (which also may occur if the battery is in use). This signal is pulled down to digital ground through a 33K resistor.
74	MFP33 - uP_BUZZER	I/O	This signal is the timer buzzer (254kHz Max) output signal that is controlled by internal registers. The MFP33 - uP_BUZZER signal comes from the processor.
75	MFP34 - MONO_OUT	I/O	The signal is the main mono output from the AC97 codec.
76	MFP35 - PC_BEEP	I/O	This is an analog input to the AC97 codec, typically used for PCBEEP signal.
77	DGND	I	Digital Ground (0V)
78	MFP36 - CD_IN_L	I/O	This is an analog input to the AC97 codec, typically used for CD line-in left signal.
79	MFP37 - CD_IN_R	I/O	This is an analog input to the AC97 codec, typically used for CD line-in right signal.
80	MFP38 - CD_GND	I/O	This signal is the CD input common mode reference (ground) to the AC97 codec.

5.4 J1B Jumper Table

Pin #	Jumper Setting (+/-)	MFP Pin	Signal Name	I/O	Description
33	+	MFP1	uP_KEY_COL0	O	This signal is Column 0 of the keyboard column drivers.
	-		uP_BATCNTL	O	This signal is Battery Control for A/D controller battery monitor.
34	+	MFP2	uP_KEY_COL1	O	This signal is Column 1 of the keyboard column drivers.
	-		uP_KMICLK	O	This is the Keyboard/Mouse Interface clock signal.
35	+	MFP3	uP_KEY_COL2	O	This signal is Column 2 of the keyboard column drivers.
	-		uP_KMIDAT	O	This is the Keyboard/Mouse Interface data line. This interface implements both PS2 and AT-compatible standards.
36	+	MFP4	uP_KEY_COL3	O	This signal is Column 3 of the keyboard column drivers.
	-		uP_INTBOOT	O	This is the Internal Boot ROM select signal. This signal is pulled down to digital GND through a 33K resistor.
37	+	MFP5	uP_KEY_COL4	O	This signal is Column 4 of the keyboard column drivers.
	-		uP_MMC_DATA3	O	This is the MultiMediaCard Data 2 signal.
38	+	MFP6	uP_KEY_COL5	O	This signal is Column 5 of the keyboard column drivers.
	-		uP_MMC_DATA2	O	This is the MultiMediaCard Data 2 signal.
39	+	MFP7	uP_KEY_COL6	O	This signal is Column 6 of the keyboard column drivers.
	-		uP_MMC_DATA1	O	This is the MultiMediaCard Data 1 signal.

40	+	MFP8	uP_KEY_COL7	O	This signal is Column 7 of the keyboard column drivers.
	-		uP_PWMSYNC	O	This is the Pulse Width Modulation Synchronizing input signal. This signal is pulled down to digital GND through a 33K resistor.
48	+	MFP9	uP_MMC_CMD - SPIDI	O	This signal is pulled up to 3.3V through a 33K resistor. This signal is the MultiMediaCard "Command" signal.
	-		uP_CFA8 - CFA24 - CFRESETB - PH1	O	If a compact FLASH interface is not needed, this signal can also be used as Port H bit 1 I/O.
49	+	MFP10	uP_MMC_nSELECT - nCS3	I/O	This signal can either be used as Chip Select 3 or as the MultimediaCard SPI mode chip select.
	-		uP_nCFSTATEN - PH7	O	This is the CompactFlash Status Read Enable signal. If a compact FLASH interface is not needed, this signal can also be used as Port H bit 7 I/O.
50	+	MFP11	uP_MMC_DATA0 - SPIDO	O	This is the MultiMediaCard/SPI data 0 signal. This signal is pulled up through a 33K resistor to 3.3V
	-		LCD_LBR	O	This is the output for reverse scanning (TFT signal).
51	+	MFP12	uP_MMC_CLK - SPICLK	O	This signal is the MultiMediaCard/SPI clock.
	-		LCD_UBL	O	This is the up and down signal for reverse scanning (TFT signal).
52	+	MFP13	uP_SCI_CLK	O	This signal is the Smart Card Interface clock.
	-		uP_USB_HN1	O	This signal is USB Data Host Negative 1 (Differential Pair).
53	+	MFP14	uP_SCI_IO	O	This is the Smart Card Interface data I/O line. This signal is pulled down to digital GND through a 33K resistor.
	-		uP_USB_HP1	O	This signal is USB Data Host Positive 1 (Differential Pair).
54	+	MFP15	uP_MEDCHG	O	Boot Media Device Change used with the uP_MODE0 and uP_MODE1 signals to specify the boot memory device. In this case, both MODE0 and MODE1 are pulled up and therefore the processor is prepared to boot up from a 32Kbit source on reset. This signal is pulled down to digital GND through a 33K resistor.
	-		uP_DEOT0	O	This is the DMA End of Transfer 1 signal. This signal is pulled down to digital GND through a 33K resistor.
56	+	MFP16	uP_SCI_DETECT - PF5	O	This signal is the Smart Card Detection signal. Upon Smart card insertion, this signal is asserted to notify the LH7A404 that a new card is preset. If the SCI interface is not needed, this signal can also be used as Port B bit 5 I/O. This signal is pulled down to digital GND through a 33K resistor.
	-		uP_USB_DCP	O	This signal is the USB device control.
57	+	MFP17	uP_SCI_VCCEN	O	This is the Smart Card Supply Voltage Enable signal
	-		uP_A/D5	O	This signal is the input to channel 8 of the Processor's 10-bit A/D converter.
58	+	MFP18	uP_SCI_RESET	O	This is the Smart Card Interface reset signal.
	-		uP_A/D6	O	This signal is the input to channel 9 of the Processor's 10-bit A/D converter.
59	+	MFP19	uP_PWMEN0	O	Active low. This signal is the DC-Dc converter pulse width modulator 0 enable.
	-		uP_CTCLKIN	O	This is the Counter Timer Clock input signal.
60	+	MFP20	uP_PCC_nCE1A	O	This is the PCMCIA card enable 2 signal. nPCCE1 and nPCCE2 are used by the PC Card for decoding low and high byte accesses.
	-		uP_UARTB_DSR	I/O	UART 3 Data Send Ready signal on the LH7A404-11.
61	+	MFP21	uP_PWM0	O	This signal is the DC-DC converter pulse width modulator 0 output.
	-		uP_UARTB_DCD - PB4	O	UART 3 Data Carrier Detect signal on the LH7A404-11. If the not needed, this signal can also be used as Port B bit 4 I/O.
62	+	MFP22	uP_PCC_nCE2A	O	This is the PCMCIA card enable 1 signal. nPCCE1 and nPCCE2 are used by the PC Card for decoding low and high byte accesses.

	-		uP_UARTA_DCD	O	UART 2 Data Carrier Detect signal on the LH7A404-11.

5.5 Multiplexed Signal Trade-Offs

5.5.1 J1C Connector SO-DIMM 144-Pin Multiplexing

Pin	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
17	uP_STATUS_1	PE6	Drives Status 1 LED	PE6	Port E bit 6 I/O
18	uP_STATUS_2	PE7	Drives Status 2 LED	PE7	Port E bit 7 I/O
23	uP_IRQD	INT3	Interrupt 3 input	PF3	Port F bit 3 I/O
25	uP_IRQC	INT2	Interrupt 2 input	PF2	Port F bit 2 I/O
27	uP_IRQB	INT1	Interrupt 1 input	PF1	Port F bit 1 I/O
29	uP_IRQA	INT0	Interrupt 0 input	PF0	Port F bit 0 I/O
39	UP_UARTA_RTS	PC4	UART 2 Ready to Send	PC4	Port C bit 4 I/O

5.5.2 J1A Expansion Connector Pin Multiplexing

Pin	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
1	LCD_VSYNC - LCD_SPS	LCDFP	LCD Vertical Sync Pulse Output (TFT)	LCDFP or LCDSPS	Frame Pulse Output (STN) or LCD Row Reset (HR-TFT)
2	LCD_HSYNC - LCD_HRLP	LCDLP	LCD Horizontal Sync Pulse Output (TFT)	LCDHRLP or LCDLP	LCD Horizontal Sync Pulse (HR-TFT) Output or Line Sync Pulse (STN)
4	LCD_DON	PC5	LCD display on	PC5	Port C bit 5 I/O
5	LCD_MDISP	LCDENAB	TFT data enable	LCDM	LCD AC bias signal
7	LCD_ VEEEN	C3	Digital supply enable	PC3	Port C bit 3 I/O
11	LCD_VSYNC - LCD_SPS	LCDFP	LCD Vertical Sync Pulse Output (TFT)	LCDFP or LCDSPS	Frame Pulse Output (STN) or LCD Row Reset (HR-TFT)
13	LCD_SPL	LCDSPL	LCDSPL Signal Output (line start pulse left)	LCDSPR	LCDSPR Signal Output (line start pulse Right) **NOTE:** Depends on the jumper setting
14	LCD_HSYNC - LCD_HRLP	LCDLP	LCD Horizontal Sync Pulse Output (TFT)	LCDHRLP or LCDLP	LCD Horizontal Sync Pulse (HR-TFT) Output or Line Sync Pulse (STN)
20	uP_AC97_RESET	AC97RESET	AC97 reset signal	PH6	Port H bit 6 I/O
41	R0	LCDVD15	LCD Intensity	PD7	Port D bit 7 I/O
47	R5	LCDVD4	LCD Data 4 I/O	PE0	Port E bit 0 I/O
48	G0	LCDVD15	LCD Intensity	PD7	Port D bit 7 I/O
49	G1	LCDVD5	LCD Data 5 I/O	PE1	Port E bit 1 I/O
50	G2	LCDVD6	LCD Data 6 I/O	PE2	Port E bit 2 I/O
51	G3	LCDVD7	LCD Data 7 I/O	PE3	Port E bit 3 I/O
52	G4	LCDVD8	LCD Data 8 I/O	PD0	Port D bit 0 I/O
53	G5	LCDVD9	LCD Data 9 I/O	PD1	Port D bit 1 I/O
54	B0	LCDVD15	LCD Intensity	PD7	Port D bit 7 I/O

56	B1	LCDVD10	LCD Data 10 I/O	PD2	Port D bit 2 I/O
57	B2	LCDVD11	LCD Data 11 I/O	PD3	Port D bit 3 I/O
58	B3	LCDVD12	LCD Data 12 I/O	PD4	Port D bit 4 I/O
59	B4	LCDVD13	LCD Data 13 I/O	PD5	Port D bit 5 I/O
60	B5	LCDVD14	LCD Data 14 I/O	PD6	Port D bit 6 I/O
67	uP_USB1_OVR_CRNT	PC2	USB Port 1 Data Carrier Detect	PC2	Port C bit 2 I/O
69	uP_USB2_PWR_EN	PC1	USB Port 1 Power Enable	PC1	Port C bit 1 I/O

5.5.3 J1B Expansion Connector Pin Multiplexing

Pin	Logic's Signal Name	Default Use	Default Description	Optional Configuration	Alternate Description
5	uP_PCC_nOE	nPCOE	PC Card Output Enable	PG0	Port G bit 0 I/O
6	uP_PCC_nWE	nPCWE	PC Card Write Enable	PG1	Port G bit 1 I/O
7	uP_PCC_nIORD	nPCIOR	PC Card IO Write Output	PG2	Port G bit 2 I/O
8	uP_PCC_nIOWR	nPCIOW	PC Card IO READ Output	PG3	Port G bit 3 I/O
10	uP_PCC_RESET	PCRESET1	PC Card Reset 1	PH0	Port H bit 0 I/O
13	uP_PCC_nIOIS16	nCFWAITB	PCMCIA IOIS16 Signal	PH5 or CFA10 or PCMCIAA24	Port H bit 5 I/O or Compact Flash Address bit 10 or Compact Flash Address bit 24
14	uP_PCC_RDY	A2	PC Card ready signal	A2	Port A bit 2 I/O
15	uP_PCC_nWAIT	nPCWAIT1	PC Card wait signal	PH4	Port H bit 4 I/O
16	UP_PCC_BVD2	PA6	Battery Sense 2	PA6	Port A bit 6 I/O
16	UP_PCC_BVD2	PA7	Battery Sense 2	PA7	Port A bit 7 I/O
18	uP_PCC_nCD2	PF7	PC Card Detect 2 Input	PF7	Port F bit 7 I/O or Interrupt 7 input only
19	uP_PCC_nCD1	PF6	PC Card Detect 1 Input	PF6	Port F bit 6 I/O or Interrupt 6 input only
20	uP_PCC_REG	nPCREG	PC Card Register Memory Access	PG4	Port G bit 4 I/O
21	uP_PCC_VS1	A4	PC Card Voltage sense 1 Input	PA4	Port A bit 4 I/O
22	uP_PCC_VS2	A5	PC Card Voltage Sense 2 Input	PA5	Port A bit 5 I/O
23	uP_PCC_nDRV	A3	PC Card Drive Output	PA3	Port A bit 3 I/O
24	uP_PCC_PCDIR	PCDIR	CF and PCMCIA Direction	PG7	Port G bit 7 I/O
41	uP_UARTB_TX	UARTTX3	UART B TX Output Only	PB1	Port B bit 1 I/O
42	uP_UARTB_RX	UARTRX3	UART B RX input Only	PB2	Port B bit 2 I/O
43	uP_UARTB_CTS	UARTCTS3	UART B RX Clear To Send	PB3	Port B bit 3 I/O

45	uP_UARTB_RTS	UARTRTS3	UART B Request To Send	PE5	Port E bit 5 I/O
46	UP_UARTC_TX	UARTTX1	UART C TX Output Only	PC0	Port C bit 0 I/O
46	UP_UARTC_RX	UARTRX1	UART C RX Input Only	PB0	Port B bit 0 I/O
48+	uP_MMC_CMD – SPIDI	MMCCMD	MMC Command	SPIDI	MMC SPI Mode Data input
48-	uP_CFA8 - CFA24 - CFRESETB - PH1	CFA8	Compact Flash Address Bit 8	PH1 or PCRESET2	Port H bit 1 I/O or PC Card reset 2
49+	uP_MMC_nSELECT - nCS3	nMMSPICS	MMC SPI Mode Chip Select	nCS3	Asynchronous memory Chip Select 3
49-	uP_nCFSTATEN - PH7	nCFSTATEN	Compact Flash Status Enable	PH7	Port H bit 7 I/O
50+	uP_MMC_DATA0 - SPID0	MMCDATA0	MMC bi-directional data channel 0	SPIDO	MMC SPI Mode Data Output
51+	uP_MMC_CLK - SPICLK	MMCCLK	MMC Clock	SPICLK	MMC SPI Mode Clock
56+	uP_SCI_DETECT - PF5	SCDETECT	Smart Card detection	PF5 or INT5	Port F bit 5 I/O or Interrupt 5 input only
61-	UP_UARTB_DCD - PB4	UARTBDCD3	UART 3 Data Carrier Detect	PB4	Port B bit 4 I/O
63	MFP23 - uP_BMI_CLK - PB7	SMBCLK	Smart Battery Clock	PB7	Port B bit 7 I/O
64	MFP24 - uP_BMISW - BMIIO - PB6	SWID	Smart Battery Single Wire Data Line	PB6 or SMBD	Port B bit 6 I/O or Smart Battery Data

6 Mechanical Specifications

6.1 Interface Connectors

The LH7A404-11 Card Engine connects to a PCB board through an industry standard 144-pin SO-DIMM connector (J1C) and two high-density 80-pin connectors (J1A and J1B).

IMPORTANT NOTE: SO-DIMM Connector must be 3.7mm mating height.

REF	Manufacturer	Card Engine P/N	Mating Connector P/N
J1A, J1B	Hirose	DF12(3.0)-80DP-0.5V(81)	DF12(3.0)-80DS-0.5V(81)
J1C	Amp	Card Edge	390112-1

Figure 6.1: Card Engine Mechanical Drawing

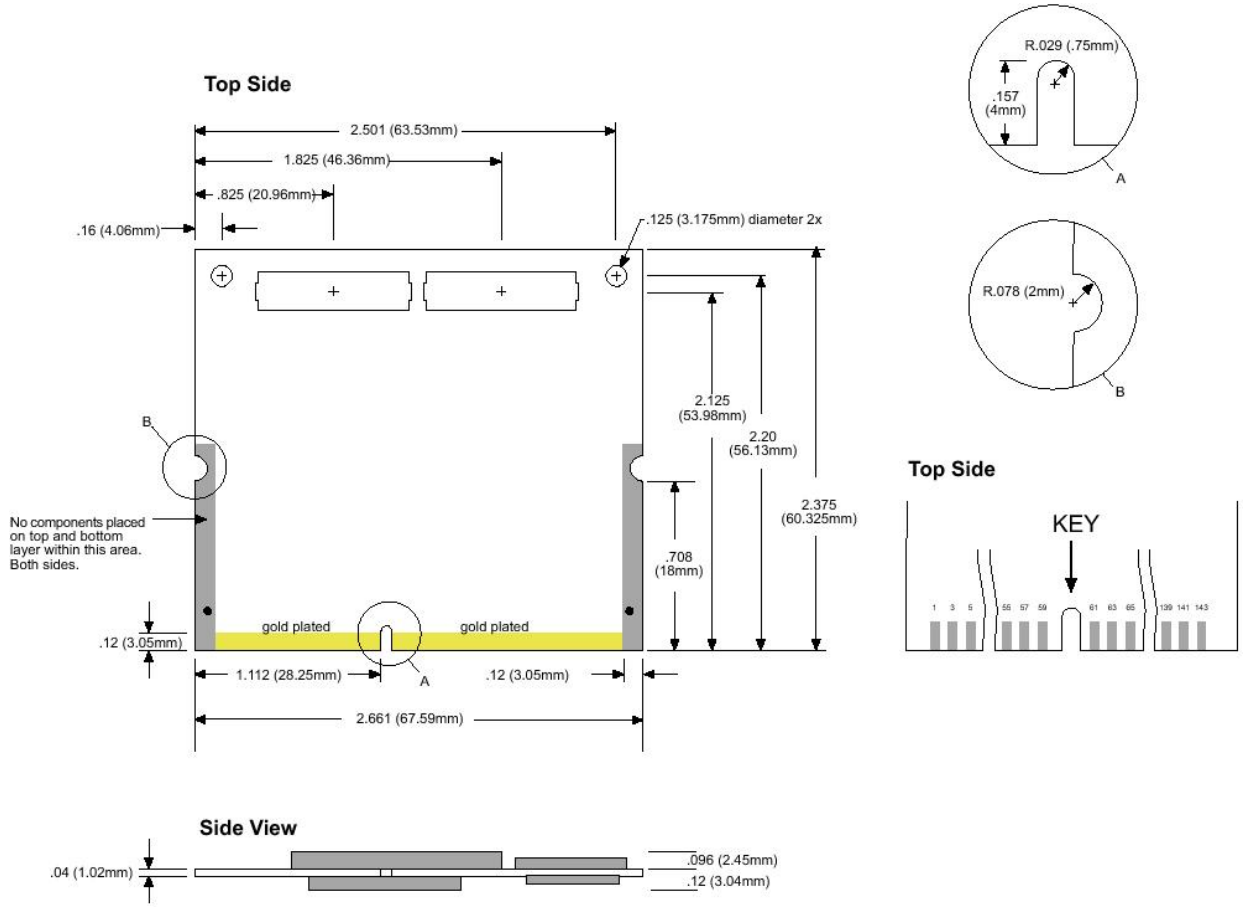


Figure 6.2: SO-DIMM Connector Specification

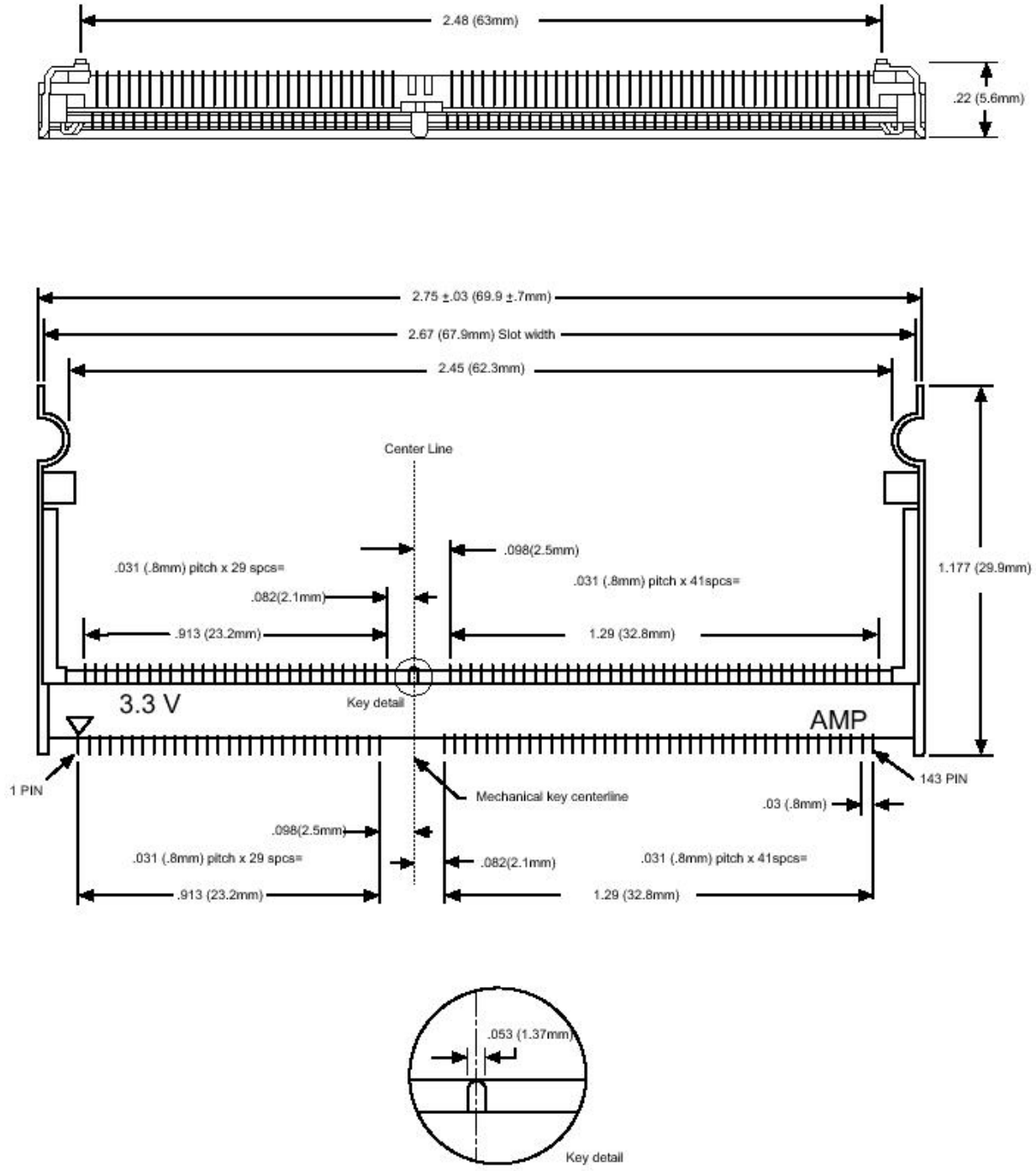


Figure 6.3: Recommended PCB Layout