# Device Package User Guide

UG112 (v2.0) May 31, 2006

XILINX®

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The following table shows the revision history for this document.

| Date | Version | Revision |
|---|---|---|
| 01/31/04 | 1.0 | Initial release |
| 02/04/05 | 1.1 | Added Pb-free packaging information. |
| 05/31/06 | 2.0 | Extensive updates and new material added. |

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## Chapter 5: Recommended PCB Design Rules

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# Package Information

## Package Overview

### Introduction to Xilinx Packaging

Electronic packages are interconnectable housings for semiconductor devices. The major functions of the electronic packages are to provide electrical interconnections between the IC and the board and to efficiently remove heat generated by the device.

Feature sizes are constantly shrinking, resulting in increased number of transistors being packed into the device. Today's submicron technology is also enabling large-scale functional integration and system-on-a-chip solutions. In order to keep pace with these new advancements in silicon technologies, semiconductor packages have also evolved to provide improved device functionality and performance.

Feature size at the device level is driving package feature sizes down to the design rules of the early transistors. To meet these demands, electronic packages must be flexible to address high pin counts, reduced pitch and form factor requirements. At the same time, packages must be reliable and cost effective.

### Packaging Technology at Xilinx

Xilinx provides a wide range of leaded and array packaging solutions for our advanced silicon products. Xilinx advanced packaging solutions include overmolded PBGAs, small form factor Chip Scale Packages, “Cavity-Down” BGAs, Flip-Chip BGAs, Flip-Chip CCGAs, as well as the newer lead frame packages such as Quad Flat No-Lead (QFN) Packages to meet various pin counts and density requirements. Packages from Xilinx have been designed, optimized, and characterized to support the long-term mechanical reliability requirements as well as to support the cutting-edge electrical and thermal performance requirements for our high-speed advanced FPGA products.

#### Pb-free Packaging Solutions from Xilinx

Xilinx has also developed packaging solutions that are safer for the environment. Today, standard packages from Xilinx do not contain substances that have been identified as harmful to the environment including cadmium, hexavalent chromium, mercury, PBB, and PBDE. Pb-free solutions take that one step further and also do not contain lead (Pb). This makes Pb-free solutions from Xilinx RoHS (Reduction of Hazardous Substances) compliant. Pb-free packages from Xilinx are also JEDEC J-STD-020 compliant, meaning that the packages have been made to be more robust so they are capable of withstanding higher reflow temperatures. Xilinx is now ready to support the industry requirements for Pb-free packaging solutions.

## Package Drawings

Package drawings are mechanical specifications that include exact dimensions for the placement of pins, height of the package, and related information.

Package drawings are available online at the Package Drawings page on xilinx.com.

## Material Data Declaration Sheet (MDDS)

The MDDS template used by Xilinx is based on the Electronic Industries Alliance (EIA) September 19, Material Composition Declaration Guide dated September 19, 2003 for Level A and Level B materials of interest.

As per EIA, "Level A" List is composed of materials and substances subject to currently enacted legislation that:

a. Prohibits their use and/or marketing
b. Restricts their use and/or marketing
c. Requires reporting or results in other regulatory effect.

As per EIA, "Level B" List is composed of materials and substances that the industry has determined relevant for disclosure because they meet one or more of the following criteria:

a. Precious materials/substances that provide economic value for end-of-life management purposes
b. Materials/substances that are of significant environmental, health, or safety interest
c. Materials/substances that would trigger hazardous waste management requirements
d. Materials/substances that could have a negative impact on end-of-life management.

See the EIA standard for more specific information.

The Xilinx Packaging Material Content Data for Standard (Non Pb-free) Packages can be found at: http://www.xilinx.com/system_resources/lead_free/material_table_std.htm.

The Xilinx Packaging Material Content Data for Pb-Free/RoHS Packages can be found at: http://www.xilinx.com/system_resources/lead_free/material_table_pbfree.htm.

# Specifications and Definitions

## Inches vs. Millimeters

The JEDEC standards for PLCC, CQFP, and PGA packages define package dimensions in inches. The lead spacing is specified as 25, 50, or 100 mils (0.025", 0.050" or 0.100").

The JEDEC standards for PQFP, HQFP, TQFP, VQFP, CSP, and BGA packages define package dimensions in millimeters. The lead frame packages have lead spacings of 0.5 mm, 0.65 mm, or 0.8 mm. The CSP and BGA packages have ball pitches of 0.5, 0.8, 1.00, or 1.27 mm.

Because of the potential for measurement discrepancies, this Data Book provides measurements in the controlling standard only, either inches or millimeters.

## Pressure Handling Capacity

For mounted BGA packages, including Flip-Chips, a direct compressive (non varying) force applied normally to the lid or top of package with a tool head that coincides with the lid (or is slightly bigger) will not induce mechanical damage to the device including external balls, provided the force is not over 5.0 grams per external ball, and the device and board are supported to prevent any flexing or bowing.

These components are tested in sockets with loads in the 5 to 10 gm/ball range for short durations. Analysis using a 10g/ball (e.g., 10 kg for FF1148) showed little impact on short-term but some creep over time. 20 gm/ball and 45 gm/ball loads at 85°C over a six week period has shown the beginning of bridging of some outer balls; these were static load tests. The component may survive forces greater than the 5 gm limit while in short-term situations. However, sustained higher loads should be avoided (particularly if they are overlaid with thermal or power cycle loads). Within the recommended limits, circuit board needs to be properly supported to prevent any flexing resulting from force application. Any flexing or bowing resulting from such a force can likely damage the package-to-board connections. Besides the damage that can occur from bending, the only major concern is long-term creep and bulging of the solder balls in compression to cause bridging. For the life of a part, staying below the recommended limit will ensure against that remote possibility.

## Clockwise or Counterclockwise

The orientation of the die in the package and the orientation of the package on the PC board affect the PC board layout. PLCC and PQFP packages specify pins in a counterclockwise direction, when viewed from the top of the package (the surface with the Xilinx logo). PLCCs have pin 1 in the center of the beveled edge while all other packages have pin 1 in one corner, with one exception: The 100-pin and 165-pin CQFPs (CB100 and CB164) for the XC3000 devices have pin 1 in the center of one edge.

CQFP packages specify pins in a clockwise direction, when viewed from the top of the package. The user can make the pins run counterclockwise by forming the leads such that the logo mounts against the PC board. However, heat flow to the surrounding air is impaired if the logo is mounted down.

## ‘Cavity-Up’ or ‘Cavity-Down’

Most Xilinx devices attach the die against the inside bottom of the package (the side that does not carry the Xilinx logo). Called “Cavity-Up,” this has been the standard IC assembly method for over 25 years. This method does not provide the best thermal characteristics. Pin Grid Arrays (greater than 130 pins), copper based BGA packages, and Ceramic Quad Flat Packs are assembled “Cavity-Down,” with the die attached to the inside top of the package, for optimal heat transfer to the ambient air. More information on Xilinx's “Cavity-Up” packages and “Cavity-Down” packages can be found in the “Package Technology Descriptions” section.

For most packages this information does not affect how the package is used because the user has no choice in how the package is mounted on a board. For Ceramic Quad Flat Pack (CQFP) packages however, the leads can be formed to either side. Therefore, for best heat transfer to the surrounding air, CQFP packages should be mounted with the logo up, facing away from the PC board.

# Part Marking

Xilinx part marking follows generalized marking schemes that are different for small and large packages. Within each group, some minor variations exist due to device family branding.

The large package template consists of the Xilinx Logo, the family brand logo (Figure 1-1), and 4 lines of information.


*Figure 1-1:* **Top Marking (for large device packages)**

**Xilinx Logo**

Xilinx logo, Xilinx name with trademark and trademark-registered status.

**Family Brand Logo**

Family name with trademark and trademark-registered status (this line is optional and might appear blank).

**Line 1**

Part name (XC4VLX60).

**Line 2**

Package type and pin count (FF668), circuit design revision (D), the location code for the wafer fab (G), the geometry code (Q), and date code (0540).

A "G" in the third letter of a package type indicates a Pb-free RoHS compliant package.

The 4-digit date code indicates the year and workweek the device was assembled. For example, "0540" is the 40th week of 2005.

**Line 3**

Five to ten alphanumeric characters for Assembly, Lot, and Step information. For devices that use silicon stepping, the last number on this line indicates the stepping level of the device (2).

***Note:*** Virtex™-4 LX and SX Step 1 devices might not have the "1" marked in the package top mark.

**Line 4**

Device speed grade (10) and temperature grade (C). If a grade is not marked on the package, the product is considered commercial grade.

In addition to the mark shown above, Line 4 can contain a few other variations as shown below:

10C xxxx
The "xxxx" indicates the SCD for the device.
An SCD is a special ordering code that is not always marked in the device top mark.

10CES
The "ES" indicates an Engineering Sample (as opposed to a production device).

10CESn
The "n" is a numeral (1, 2, 3, etc.)
The "ESn" indicates an Engineering Sample "n", for example ES1, ES2, ES3, etc.

The second template is used on smaller packages that do not have enough room for six lines of marking (Figure 1-2). This marking is used mainly for PROMs, and may be found on some medium size packages as well.


*Figure 1-2:* **Top Marking (for small to medium device packages)**

**Line 1**

Product Name Code: Eight characters; the five or six (1765D) characters designate the product name representation - usually the name without the "XC." The name is followed by the PROM package designator (usually single character). The last letter represents the temperature range (e.g., M, I, C).

**Line 2**

Six numeric characters preceded by the "X" of the Xilinx logo. The first numeric character after the "X" designates the last digit of the year in which the product was assembled; this will be the same every 10 years. The next two numeric characters identify the assembly work week. The last three characters are the final three digits of the Assembly number for the lot.

**Line 3**

This line is usually left blank for customer PROM designator marking.

# Package Technology Descriptions

## Pb-Free Packaging

Recent legislative directives and corporate driven initiatives around the world have called for the elimination of Pb and other hazardous substances in electronics used in many

sectors of the electronics industry. The Pb-free program at Xilinx was established in 1999 as a proactive effort to develop and qualify suitable material sets and processes for Pb-free applications. Xilinx has taken the leadership position by quickly forming partnerships with our customers, suppliers, and participating in industry consortiums to provide technical solutions that are aligned with industry requirements.

### Pb-free Material Set

Xilinx has researched alternatives for Pb compounds and has selected matte Sn lead finish for lead-frame packages and SnAgCu solder balls for BGA packages. In addition, suitable material sets have been chosen and qualified for higher reflow temperatures (245ºC – 260ºC) that are required by Pb-free soldering processes. Pb-free products from Xilinx are designated with an additional "G" in the package designator portion of the part number. For example, FGG1152 is the Pb-free version of FG1152.

### Features

- RoHS compliant
- Compliant to JEDEC-J-STD-020 standard for peak reflow temperature (245ºC - 260ºC)
- Packages marked with Pb-free identifier

### Backward Compatibility

Backward compatibility, as described in this chapter, refers only to the soldering process. Pb-free devices from Xilinx have the same form, fit and function as standard Pb-based products. No changes are required for board design when using Pb-free products from Xilinx. However, finish materials for boards may need to be adjusted.

Lead frame packages (PQG, TQG, VQG, PCG, QFG, etc.) from Xilinx are backward compatible, meaning that the component can be soldered with Sn/Pb solder using Sn/Pb soldering process. Lead-frame packages from Xilinx use a matte Sn plating on the leads which is compatible with both Pb-free soldering alloys and Sn/Pb soldering alloy.

BGA packages (CPG, FTG, FGG, BGG, etc.), however, are not recommended to be soldered with SnPb solder using a Sn/Pb soldering process. The traditional Sn/Pb soldering process usually has a peak reflow temperature of 205ºC - 220ºC. At this temperature range, the SnAgCu BGA solder balls do not properly melt and wet to the soldering surfaces. As a result, reliability and assembly yields may be compromised.

For more information on Xilinx Pb-free solutions, refer to http://www.xilinx.com/pbfree, and for more information on the Pb-free reflow process, refer to the *"Implementation and Solder Reflow Guidelines for Pb-Free Packages"* Application Note (XAPP427).

## 'Cavity-Up' Plastic BGA Packages

BGA is a plastic package technology that utilizes area array solder balls at the bottom of the package to make electrical contact with the system circuit board. The area array format of solder balls reduces package size considerably when compared to leaded products. It also results in improved electrical performance as well as having higher manufacturing yields.

The substrate is made of a mutilayer BT (bismaleimide triazene) epoxy-based material. Power and ground pins are grouped together and the signal pins are assigned in the perimeter format for ease of routing on to the board. The package is offered in a die up format and contains a wirebonded device that is covered with a mold compound.

### Package Construction

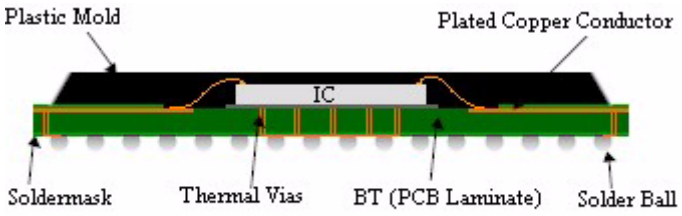


*Figure 1-3:* **'Cavity-Up' Ball Grid Array Package**

As shown in the cross section of Figure 1-3, the BGA package contains a wire bonded die on a single-core printed circuit board with an overmold. Beneath the die are the thermal vias which can dissipate the heat through a portion of the solder ball array and ultimately into the power and ground planes of the system circuit board. This thermal management technique provides better thermal dissipation than a standard PQFP package. Metal planes also distribute the heat across the entire package, enabling a 15–20% decrease in thermal resistance to the case.

### Key Features/Advantages of Xilinx 'Cavity-Up' BGA Packages

- High board assembly yield since board attachment process is self-centering
- SMT compatible, resulting in minimum capital investment
- Extendable to multichip modules
- Low profile and small footprint
- Improved electrical performance (short wire length)
- Enhanced thermal performance
- Excellent board level reliability

## 'Cavity-Down' Thermally Enhanced BGA Packages

Copper-based "Cavity-Down" BGAs are high-performance, low-profile packages that offer superior electrical and thermal characteristics. This technology is especially applicable for high-speed, high-power semiconductors such as Xilinx's Virtex device family.

### Package Construction

Figure 1-4 depicts the cross-section of the "Cavity-Down" BGA package. It should be noted that this is a solid construction without any internal cavity. The backside die is attached directly to the copper heat spreader and conducts heat out of the package through an epoxy die attach adhesive. The larger the die size and the package body size, the better the thermal performance. The incorporation of the copper heat spreader also results in thermal resistance values that are lowest among the packages offered by Xilinx.

Attached to the heatspreader is a copper stiffener with cavity out to accommodate the die. Along with the heatspreader, this stiffener provides the mechanical flexural strength and warpage control for the package. On the exposed surface of the stiffener is a laminate or build-up structure that contains the circuit traces, the power and ground planes if any, and the sites for the connecting solder balls. The laminate is made of either a glass reinforced

high glass transition Temperature (Tg) Bismaleimide Triazine (BT) or Build up structure. Xilinx uses laminate with up to four layers, including PWR and GND planes.

### Key Features/Advantages of Xilinx 'Cavity-Down' BGAs

- Lowest Thermal Resistance ($\theta_{JA}$ < 13°C/W)
- Superior Electrical Performance
- Low Profile and Light Weight Construction
- Excellent board-level reliability

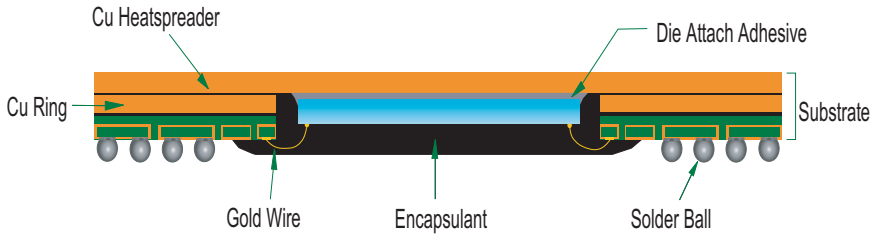


*Figure 1-4:* **'Cavity-Down' BGA Package**

## Flip-Chip BGA Packages

Flip-Chip is a packaging interconnect technology that replaces peripheral bond pads of traditional wirebond interconnect technology with area array interconnect technology at the die/substrate interface. The bond pads are either redistributed on the surface of the die or in some very limited cases, they are directly dropped from the core of the die to the surface. Because of this inherent distribution of bond pads on the surface of the device, more bond pads and I/Os can be packed into the device.

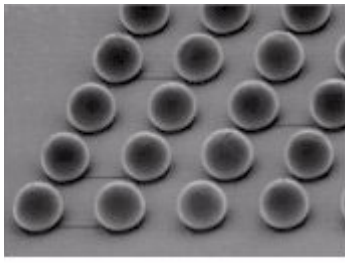

*Figure 1-5:* **Eutectic Bumps**

Xilinx flip chip BGA package is offered for Xilinx high-performance FPGA products. Unlike traditional packaging in which the die is attached to the substrate face up and the connection is made by using wire, the solder bumped die in flip chip BGA is flipped over and placed face down, with the conductive bumps connecting directly to the matching metal pads on the laminate substrate.

Unlike traditional packaging technology in which the interconnection between the die and the substrate is made possible using wire, Flip-Chip utilizes conductive bumps that are placed directly on the area array pads of the die surface. The area array pads contain wettable metallization for solders (either eutectic or high lead) where a controlled amount of solder is deposited either by plating or screen-printing. These parts are then reflowed to

yield bumped dies with relatively uniform solder bumps over the surface of the device. The device is then flipped over and reflowed on a ceramic or organic laminate substrate. The solder material at molten stage is self-aligning and produces good joints even if the chips are placed offset to the substrates. After the die is soldered to the substrate, the gap (standoff) formed between the chip and the substrate is filled with an organic compound called underfill. The underfill is a type of epoxy that helps distribute stresses from these solder joints to the surface of the whole die and hence improve the reliability and fatigue performance of these solder joints.

This interconnect technology has emerged in applications related to high performance communications, networking and computer applications as well as in consumer applications where miniaturization, high I/O count, and good thermal performance are key attributes.

## Package Construction

Flip-Chip BGA Packages for high performance applications are built on high-density multi-layers organic laminate substrates. Since the Flip-Chip bump pads are in area array configuration, it requires very fine lines and geometry on the substrates to be able to successfully route the signals from the die to the periphery of the substrates. Multilayer build up structures offers this layout flexibility on Flip-Chip packages.

Figure 1-6 and Figure 1-7 show cross-section views of the package constructions. Note that two types of lids are used to assemble Flip-Chip BGA packages; Type I Lids (as shown in Figure 1-6) and Type II Lids (as shown in Figure 1-7), depending on the package type.

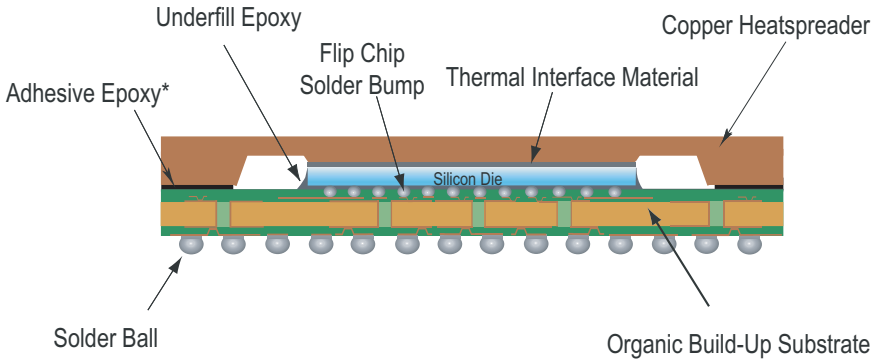


*Figure 1-6:* **Flip-Chip BGA Package with Type I Lid**

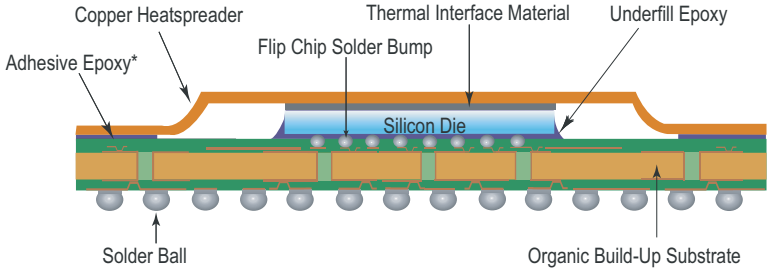


*Figure 1-7:* **Flip-Chip BGA Package With Type II Lid**

*Xilinx flip chip packages are not hermetically sealed and exposure to cleaning solvents/ chemicals or excessive moisture during boards assembly could pose serious package

reliability concerns. Small vents are kept by design between the heatspreader (lid) and the organic substrate to allow for outgassing and moisture evaporation. Solvents or other corrosive chemicals could seep through these vents and attack the organic materials and components inside the package and hence are strongly discouraged during board assembly of Xilinx flip chip BGA packages.

### Key Features/Advantages of Flip-Chip BGA Packages

- Easy access to core power/ground, resulting in better electrical performance
- Excellent Thermal Performance (Direct heatsinking to backside of the die)
- Higher I/O density since bond pads are in area array format
- Higher frequency switching with better noise control

## Assembling Flip Chip BGAs

The Xilinx Flip Chip BGAs conform to JEDEC body sizes and footprint standards. These packages follow the EIA moisture level classification for plastic surface mount components (PSMC). Standard surface mount assembly process should be used with consideration for the slightly higher thermal mass for these packages.

Like other SMT components, flip chip BGA assembly involves the following process: screen printing, solder reflow, post reflow washing. The following will serve as a guideline on how to assemble flip chip BGAs onto PCBs.

### Screen Printing Machine Parameters

Below is an example of the parameters that were used for the screen printing process. Note that these may not be optimized parameters. Optimized parameters may depend on user's applications and setup.

- Equipment: MPM Ultraprint 2000
- Squeegee Type: Metal
- Squeegee Angle: 45°
- Squeegee Pressure: 24 lbs/sq. in.
- Squeegee Speed: 0.7 in/sec
- Print Cycle: One pass
- Stencil Snap Off: 0.10 inches
- Stencil Lift Off Speed: Slow

### Screen Printing Process Parameters

- Solder Paste: Alpha Metals WS609 (Water Soluble)
- Stencil Aperture: 0.0177 inches Diameter
- Stencil Thickness: 0.006 inches
- Aperture Creation: Laser cut

*It is highly recommended to use either a no-clean solder paste or a water soluble solder paste.* If cleaning is required, then a water soluble solder paste should be used.

## Chip Scale Packages

Chip Scale Packages have emerged as a dominant packaging option for meeting the demands of miniaturization while offering improved performance. Applications for Chip Scale Packages are targeted to portable and consumer products where real estate is of utmost importance, miniaturization is key, and power consumption/dissipation must be low. A Chip Scale Package is defined as a package that fits the definition of being between 1 to 1.2 times the area of the die that the package contains while having a pitch of less than 1 mm.

By employing Xilinx's CSP packages, system designers can dramatically reduce board real estate and increase the I/O counts.

### Package Construction

Although there are currently more than 50 different types of CSPs available in the market, Xilinx CSP packages fall into two categories, as shown in Figure 1-8: (1) Flex-based substrates and (2) Rigid BT-based substrates. Although, both types meet the reliability requirement at the component and board level, BT-based substrate was chosen for the newer devices because of the large vendor base producing/supporting the BT-based substrates.

### Key Features/Advantages of CSP Packages

- An extremely small form factor which significantly reduces board real estate for such applications as PCMCIA cards, portable and wireless designs, and PC add-in cards
- Lower inductance and lower capacitance
- The absence of thin, fragile leads found on other packages
- A very thin, light-weight package


*Figure 1-8:* **Rigid BT-based Substrate Chip Scale Packages, left; Flex-Based Tape Substrate, right**

## Quad Flat No-Lead (QFN) Packages

Quad Flat No-Lead (QFN) or MLF package is a robust and low-profile lead frame-based plastic package that has several advantages over traditional lead frame packages. The exposed die-attach paddle enables efficient thermal dissipation when directly soldered to the PCB. Additionally, this near chip scale package offers improved electrical performance, smaller package size, and an absence of external leads. Since the package has no external leads, coplanarity and bent leads are no longer a concern.

Xilinx Quad Flat No-Lead packages are ideal for portable applications where size, weight, and performance matter.

### Package Construction

The QFN is a molded leadless package with land pads on the bottom of the package. Electrical contact to the PCB is made by soldering the land pads to the PCB. The backside of the die is attached to the exposed paddle through the die attach material which is electrically conductive. The exposed pad therefore represents a weak ground and should be left floating or connected to a ground net.

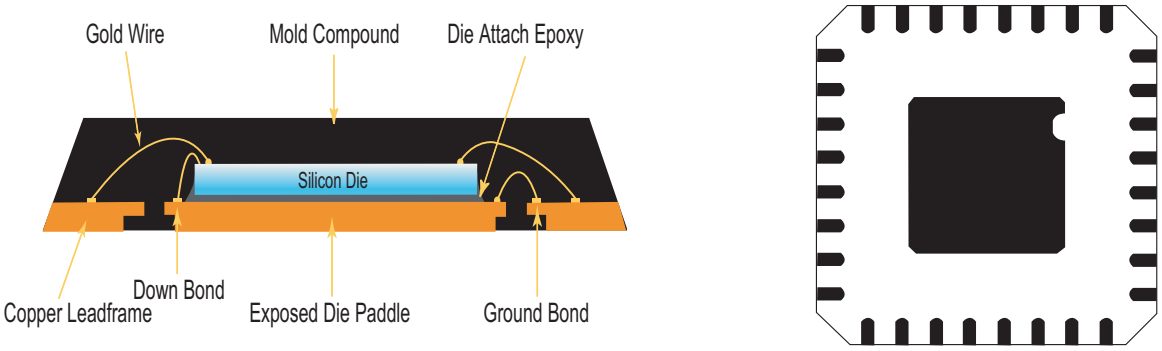


*Figure 1-9:* **On the Left is the QFN Cross-Section. On the Right is the Bottom View.**

### Key Features/Advantages of QFN Packages

- Small size and light weight
- Excellent thermal and electrical performance
- Compatible with conventional SMT processes

## Ceramic Column Grid Array (CCGA) Packages

Ceramic Column Grid Array (CCGA) packages are surface-mount-compatible packages that use high-temperature solder columns as interconnections to the board. Compared to the solder spheres, the columns have lower stiffness and provide a higher stand-off. These features significantly increase the reliability of the solder joints. When combined with a high-density, multilayer ceramic substrate, this packaging technology offers a high density, reliable packaging solution. Ceramic offers the following benefits:

### Key Features/Advantages of CCGA Packages

- High planarity and excellent thermal stability at high temperature
- CTE matches well with the silicon die
- Low moisture absorption

Xilinx offers 3 different formats of CCGA: "Cavity-Down" wire-bonded CCGA, "Cavity-Up" wire-bonded CCGA, and Flip-Chip CCGA.

### 'Cavity-Down' Wire-Bonded CCGA – CG560 Package Construction

CG560 is offered with the Xilinx XQV1000 and XQVR1000 devices. It is pin-compatible with the plastic BG560 package. Below are additional attributes of CG560.

- Interconnect: 90Pb/10Sn hard solder column interposer, attached with 63Sn/37Pb soft solder.
- Hermetically sealed with eutectic Sn/Au

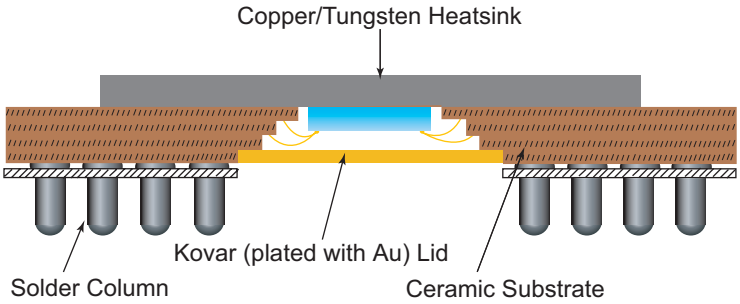


*Figure 1-10:* **CG560 Package**

### 'Cavity-Up' Wire-Bonded BGA – CG717 Package Construction

CG717 is offered with the Xilinx XQ2V3000 and XQR2V3000 devices. It is pin-compatible with the plastic BG728 package. Below are additional attributes of CG717.

- Interconnect: 80Pb/20Sn hard solder column, attached with 63Sn/37Pb soft solder.
- Hermetically sealed with eutectic Sn/Au

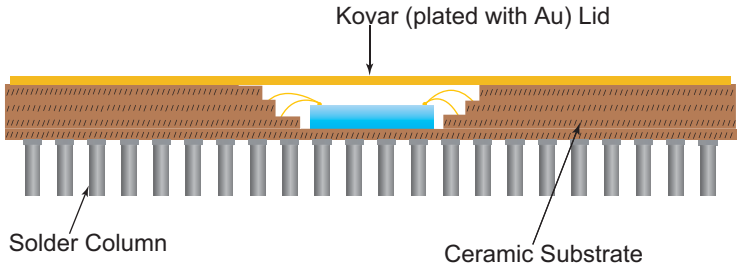


*Figure 1-11:* **CG717 Package**

### Flip-Chip CCGA – CF1144 Package Construction

Flip-Chip CCGA is targeted for applications that require high performance, density, and high reliability. CF1144 is offered with the Xilinx XQ2V6000 and XQR2V6000 devices. The CF1144 package is pin-compatible with the plastic Flip-Chip FF1152 package. Below are additional attributes of CF1144:

- 95Pb/5Sn Flip-Chip solder bumps
- 90Pb/10Sn hard solder column

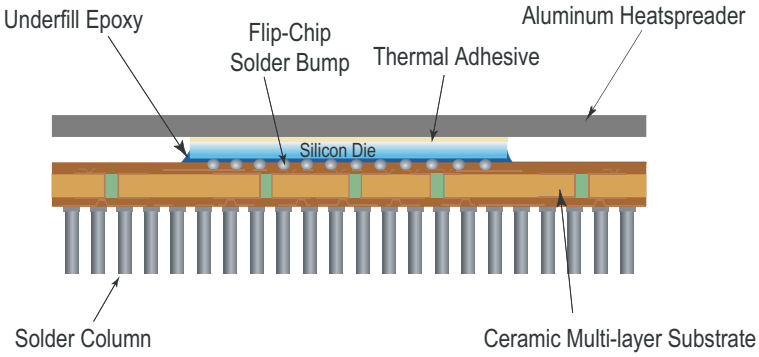


*Figure 1-12:* **CF1144 Package**

## Thermally Enhanced Lead Frame Packaging

Xilinx offers thermally enhanced quad flat pack packages on XC4000 Series devices and some earlier Virtex devices. This section discusses the performance and usage of these packages (designated HQ).

### Key Features/Advantages of Thermally Enhanced Lead Frame Packages

- The HQ-series and the regular PQ packages conform to the same JEDEC drawings.
- The HQ and PQ packages use the same PCB land patterns.
- The HQ packages have more mass
- Thermal performance is better for the HQ packages

### Applications of HQ Packages

- HQ packages are offered as the thermally enhanced equivalents of PQ packages. They are used for high gate count or high I/O count devices in packages, where heat dissipation without the enhancement may be a handicap for device performance. Such devices include XC4013E, XC4020E, XC4025E, and XC5215.
- The HQ series at the 240-pin count level or below are offered with the heatsink at the bottom of the package. This was done to ensure pin to pin compatibility with the existing PQ packages.

At the 304-pin count level, the HQ is offered with the heatsink up. This arrangement offers a better potential for further thermal enhancement by the designer.

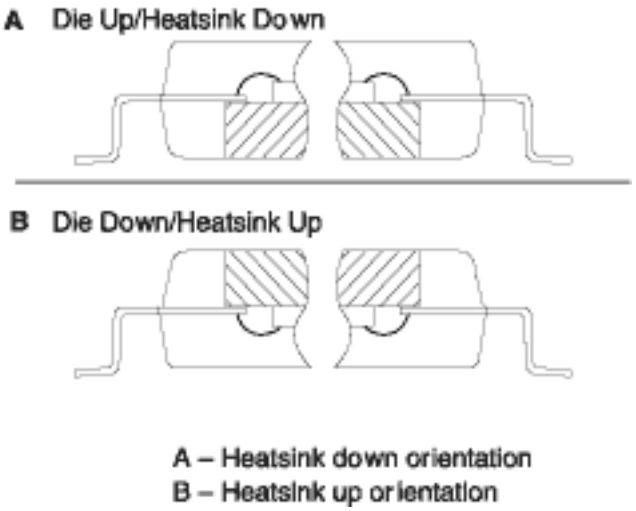


*Figure 1-13:* **Heatsink Orientation**

- In the die-up/heatsink-down configuration, the heatsink surface is insulated.

# Package Mass Table

The numbers provided in Table 1-1 represent average values for typical devices used in the package. Die size variation from device to device, slight changes in moisture content, number of specific layers used in the specific substrate etc., will provide some variation. In some cases the data accuracy may be up to ±10%. More precise numbers for specific devices in a lot may be obtained from insitu weighing. If this is critical, specific lot information may be requested.

*Table 1-1:* **Package Mass (Weight) by Package Type**

| Package | Description | Mass (g) |
|---|---|---|
| BF957, BFG957 | 957 Ball - Flip-Chip BGA 40x40 Body (1.27mm Pitch) | 18.5 |
| BG225, BGG225 | Molded BGA 27mm Full Matrix | 2.2 |
| BG256, BGG256 | Molded BGA 27mm Peripheral | 2.2 |
| BG352, BGG352 | SuperBGA - 35 x 35mm Peripheral | 7.1 |
| BG388 | MPM BGA - 35 x 35mm (1.27mm Pitch) | 4.64 |
| BG432, BGG432 | SuperBGA - 40 x 40mm Peripheral | 9.1 |
| BG492, BGG492 | Molded BGA - 35mm - 1.27mm Pitch | 4.6 |
| BG560, BGG560 | SuperBGA - 42.5 x 42.5mm SQ | 12.3 |
| BG575, BGG575 | 575 BGA 31 x 31mm Body (1.27mm Pitch) | 4.4 |
| BG728, BGG728 | 728 BGA 35 X 35mm Body (1.27mm Pitch) | 6.2 |
| CB100 | NCTB Top Braze 3K / 4K VER | 10.8 |

*Table 1-1:* **Package Mass (Weight) by Package Type *(Continued)***

| Package | Description | Mass (g) |
|---|---|---|
| CB164 | NCTB Top Braze 3K / 4K VER | 11.5 |
| CB196 | NCTB Top Braze 4K VER | 15.3 |
| CB228 | NCTB Top Braze 4K VER | 17.6 |
| CC20 | Ceramic Leaded Chip Carrier | 8.4 |
| CC44 | Ceramic Leaded Chip Carrier | 2.9 |
| CD48 | Ceramic Side Braze - DIP | 8.0 |
| CD8 | Ceramic Side Braze - DIP | 0.9 |
| CF1144 | Ceramic Column Flip-Chip, 35 x 35mm, 1.0 mm Pitch | 44.0 |
| CG560 | Ceramic SPGA 42.5 X 42.5 | 44.0 |
| CG717 | Ceramic Column Grid Array, 35 x 35mm, 1.27 mm Pitch | 13.27 |
| CP56, CPG56 | CSP 56 BGA - 6mm (0.5mm pitch) | 0.1 |
| CP132, CPG132 | CSP 132 BGA - 8x8mm, 0.5mm ball pitch | 0.1 |
| CS48, CSG48 | CSP 48 BGA - 7mm (0.8 pitch) | 0.2 |
| CS144, CSG144 | CSP 144 BGA - 12mm (0.8 pitch) | 0.3 |
| CS280, CSG280 | CSP 280 BGA - 16mm (0.8 pitch) | 0.5 |
| DD8 | 300 Cerdip Package | 1.1 |
| FF668, FFG668 | 668 Ball - Flip-Chip BGA, 27 x 27mm, 1.0 mm Ball Pitch | 4.4 |
| FF672, FFG672 | 672 Ball - Flip-Chip BGA, 27 x 27mm, 1.0 mm Ball Pitch | 4.4 |
| FF676 | 676 Ball - Flip-Chip BGA, 27 x 27mm, 1.0 mm Pitch Full | 4.4 |
| FF896, FFG896 | 896 Ball - Flip-Chip BGA 31 X 31mm Body (1.0 mm Pitch) | 11.2 |
| FF1136 | Flip-Chip BGA, 35 x 35mm, 1.0 mm | 14.0 |
| FF1148, FFG1148 | 1148 Ball - Flip-Chip BGA 35 X 35mm Body (1.0mm Pitch) | 14.0 |
| FF1152, FFG1152 | 1152 Ball - Flip-Chip BGA 35 X 35mm Body (1.0mm Pitch) | 14.0 |
| FF1153 | Flip-Chip BGA 35mm x 35mm 1.0 mm | 14.0 |
| FF1513, FFG1513 | 1513 Ball - Flip-Chip BGA 40 X 40mm Body (1.0mm Pitch) | 17.0 |
| FF1517, FFG1517 | 1517 Ball - Flip-Chip BGA 40 X 40mm Body (1.0mm Pitch) | 17.2 |

*Table 1-1:* **Package Mass (Weight) by Package Type *(Continued)***

| Package | Description | Mass (g) |
|---|---|---|
| FF1696, FFG1696 | 1696 Ball - Flip-Chip BGA 42.5 X 42.5mm Body (1.0mm Pitch) | 20.5 |
| FF1704, FFG1704 | 1704 Ball - Flip-Chip BGA 42.5 X 42.5mm Body (1.0mm Pitch) | 21.1 |
| FF1738 | Flip-Chip BGA 42.5 x 42.5mm 1.0 mm Pitch | 22.0 |
| FF1760 | Flip-Chip BGA 42.5 x 42.5mm 1.0 mm Pitch | 22.0 |
| FG256, FGG256 | Fine Pitch BGA 17 x 17 mm, 1.0 mm ball pitch | 0.8 |
| FG320, FGG320 | Fine Pitch BGA 19 x 19 mm, 1.0 mm ball pitch | 1.4 |
| FG324, FGG324 | Molded BGA 23 mm - 1.0 mm Pitch | 2.2 |
| FG456, FGG456 | Fine Pitch BGA 23 x 23 mm, 1.0 mm ball pitch | 2.2 |
| FG400, FGG400 | Fine Pitch BGA 21 x 21mm, 1.0 mm ball pitch | 2.2 |
| FG484 | Molded BGA 23 mm - 1.0 mm Pitch | 2.2 |
| FG556, FGG556 | Fine Pitch BGA 31 x 31 mm, 1.0 mm ball pitch | 3.9 |
| FG580 | SuperBGA 35 x 35 mm, 1.0 mm Pitch | 7.1 |
| FG676, FGG676 | Fine Pitch BGA 27 x 27 mm, 1.0 mm ball pitch | 3.4 |
| FG680, FGG680 | Fine Pitch BGA 40 x 70 mm, 1.0 mm ball pitch | 10.6 |
| FG860, FGG860 | Fine Pitch BGA 42.5 x 42.57 mm, 1.0 mm ball pitch | 13.8 |
| FG900, FGG900 | Fine Pitch BGA 31 x 31 mm, 1.0 mm ball pitch | 4.2 |
| FG1156, FGG1156 | Fine Pitch BGA 35 x 35 mm, 1.0 mm Ball Pitch | 6.2 |
| FS48, FSG48 | CSP 48BGA, 6 x 8mm, 0.8 mm Ball Pitch | 0.1 |
| FT256, FTG256 | 256 Thin PBGA 17 X 17mm Body (1.0mm Pitch) | 0.9 |
| HQ160, HQG160 | Metric 28 x 28 - 0.65mm 1.6H/S Die Up | 10.8 |
| HQ208, HQG208 | Metric 28 x 28 - H/S Die Up | 10.8 |
| HQ240, HQG240 | Metric QFP 32 x 32 H/S Die Up | 15.0 |
| HQ304, HQG304 | Metric QFP 40 x 40 - H/S Die Down | 26.2 |
| HT144 | Thin QFP 1.4 H/S - (HQ) Die Up | 2.6 |
| HT176 | Thin QFP 1.4 H/S - (HQ) Die Up | 3.5 |
| PC20, PCG20 | PLCC JEDEC MO-047 | 0.8 |
| PC28, PCG28 | PLCC JEDEC MO-047 | 1.1 |
| PC44, PCG44 | PLCC JEDEC MO-047 | 1.2 |
| PC68, PCG68 | PLCC JEDEC MO-047 | 4.8 |
| PC84, PCG84 | PLCC JEDEC MO-047 | 6.8 |

*Table 1-1:* **Package Mass (Weight) by Package Type *(Continued)***

| Package | Description | Mass (g) |
|---|---|---|
| PD8 | DIP .300 Standard | 0.5 |
| PD48 | DIP .600 Standard | 7.9 |
| PG68 | Ceramic PGA “Cavity Up” 11 x 11 | 7.0 |
| PG84 | Ceramic PGA “Cavity Up” 11 x 11 | 7.2 |
| PG84 | Windowed CPGA “Cavity Up” 11 x 11 | 7.5 |
| PG120 | Ceramic PGA 13 x 13 Matrix | 11.5 |
| PG132 | Ceramic PGA 14 x 14 Matrix | 11.8 |
| PG156 | Ceramic PGA 16 x 16 Matrix | 17.1 |
| PG175 | Ceramic PGA 16 x 16 Standard Version | 17.7 |
| PG191 | Ceramic PGA 18 x 18 Standard - All | 21.8 |
| PG223 | Ceramic PGA 18 x 18 Type | 26.0 |
| PG299 | Ceramic PGA 20 x 20 Heatsink | 37.5 |
| PG299 | Ceramic PGA 20 x 20 Matrix | 29.8 |
| PG411 | Ceramic PGA 39 x 39 Stagger | 36.7 |
| PG475 | Ceramic PGA 41 x 41 Stagger | 39.5 |
| PG559 | Ceramic PGA 43 x 43 | 44.5 |
| PQ44, PQG44 | EIAJ 10 x 10 x 2.0 QFP | 0.5 |
| PQ100, PQG100 | EIAJ 14 x 20 QFP - 1.60 (default) | 1.6 |
| PQ100, PQG100 | EIAJ 14 x 20 QFP - 1.80 (not used) | 1.6 |
| PQ100, PQG100 | EIAJ 14 x 20 QFP - 1.95 (old version) | 1.6 |
| PQ160, PQG160 | EIAJ 28 x 28 0.65mm 1.60 | 5.8 |
| PQ208, PQG208 | EIAJ 28 x 28 0.5mm 1.30 | 5.3 |
| PQ240, PQG240 | EIAJ 32 x 32 0.5mm | 7.1 |
| SF363 | Flip-Chip BGA 17 x 17, 0.8mm Pitch | 1.6 |
| SO8 | Version 1 - 0.150/50 mil | 0.1 |
| SO20 | 300 mil SOIC | 0.5 |
| SO24 | 300 mil SOIC | 0.6 |
| TQ100, TQG100 | Thin QFP 1.4mm thick | 0.7 |
| TQ128, TQG128 | Thin QFP 1.4mm thick - RECT | 0.8 |
| TQ144, TQG144 | Thin QFP 1.4mm thick | 1.4 |
| TQ176, TQG176 | Thin QFP 1.4mm thick | 1.9 |
| VO8, VOG8 | Thin SOIC - II | 0.1 |
| VO20, VOG20 | Thin SSOP, 4.4 mm | 0.1 |

*Table 1-1:* **Package Mass (Weight) by Package Type *(Continued)***

| Package | Description | Mass (g) |
|---|---|---|
| VO48, VOG48 | Thin SOP | 0.5 |
| VQ44, VQG44 | Thin QFP 1.0 thick | 0.4 |
| VQ64, VQG64 | THIN QFP 1.0 thick | 0.5 |
| VQ100, VQG100 | Thin QFP 1.0 thick | 0.6 |

Chapter 2

# Pack and Ship

## Introduction

Xilinx offers several packing options for our through-hole and surface-mount products. The devices are packed in either tubes, trays, or tape and reel.

## Tape and Reel

Xilinx offers a tape and reel packing for PLCC, BGA, QFP, and SO packages. The packing material is made of black conductive polystyrene and protects the packages from mechanical and electrical damage. The reel material provides a suitable medium for pick and place equipment.

The tape and reel packaging consists of a pocketed carrier tape, sealed with a protective cover. The device sits on pedestals (for PLCC, QFP packages) to protect the leads from mechanical damage. All devices loaded into the tape carriers are baked, lead scanned before the cover tape is attached and sealed to the carrier. In-line mark inspection for mark quality and package orientation is used to ensure shipping quality.

### Benefits

- Increased quantity of devices per reel versus tubes improves cycle time and reduces the amount of time to index spent tubes.
- Tape and reel packaging enables automated pick and place board assembly.
- Reels are uniform in size enabling equipment flexibility.
- Transparent cover tape allows device verification and orientation.
- Antistatic reel materials provides ESD protection.
- Carrier design include a pedestal to protect package leads during shipment.
- Bar code labels on each reel facilitate automated inventory control and component traceability.
- All tape and reel shipments include desiccant pouches and humidity indicators to ensure products are safe from moisture.
- Compliant to Electronic Industries Association (EIA) 481. Material and Construction Carrier Tape.
- The pocketed carrier tape is made of conductive polystyrene material, or equivalent, with a surface resistivity level of less than 106 ohms per square inch.
- Devices are loaded “live bug” or leads down, into a device pocket.
- Each carrier pocket has a hole in the center for automated sensing of whether a unit is in the pocket or not.

- Sprocket holes along the edge of the carrier tape enable direct feeding into automated board assembly equipment.

## Cover Tape

An anti-static, transparent, polyester cover tape, with heat activated adhesive coating, sealed to the carrier edges to hold the devices in the carrier pockets.

Surface resistivity on both sides is less than 1011 ohms per square inch.

## Reel

The reel is made of anti-static polystyrene material. The loaded carrier tape is wound onto this conductive plastic reel.

A protective strip made of conductive polystyrene material is placed on the outer part of the reel to protect the devices from external pressure in shipment.

Surface resistivity is less than 1011 ohms per square inch.

Device loading orientation is in compliance with EIA Standard 481.

## Bar Code Label

The bar code label on each reel provides customer identification, device part number, date code of the product and quantity in the reel.

Print quality are in accordance with ANSI X3.182-1990 Bar Code Print Quality Guidelines. Presentation of Data on labels are EIA-556-A compliant.

The label is an alphanumeric, medium density Code 39 labels.

This machine-readable label enhances inventory management and data input accuracy.

## Shipping Box

The shipping container for the reels are in a 13" x 13" x 3" C-flute, corrugated, #3 white “pizza box,” rated to 200 lb. test.

*Table 2-1:* **Tape and Reel Packaging**

| Package Code | Qty. Per Reel | Reel Size (inches) | Carrier Width (mm) | Cover Width (mm) | Pitch (mm) |
|---|---|---|---|---|---|
| BG225(1), BGG225(1) | 500 | 13 | 44 | 37.5 | 32 |
| BG256(1), BGG256(1) | 500 | 13 | 44 | 37.5 | 32 |
| BG272(1), BGG272(1) | 500 | 13 | 44 | 37.5 | 32 |
| CP56(1), CPG56(1) | 4000 | 13 | 12 | 9.2 | 8 |
| CS48(1), CSG48(1) | 1500 | 13 | 16 | 13.3 | 12 |
| CS144(1), CSG144(1) | 2000 | 13 | 24 | 21.0 | 16 |
| FG256(1), FGG256(1) | 1000 | 13 | 24 | 21.0 | 20 |
| FG456(1), FGG456(1) | 500 | 13 | 44 | 37.5 | 32 |
| FG676(1), FGG676(1) | 500 | 13 | 44 | 37.5 | 32 |
| FT256, FTG256 | 1000 | 13 | 24 | 21 | 20.0 |
| PC20(1), PCG20(1) | 750 | 13 | 16 | 13.3 | 12 |
| PC44(1), PCG44(1) | 500 | 12 | 32 | 25.5 | 14 |
| PC68(1), PCG68(1) | 250 | 13 | 44 | 37.5 | 32 |
| PC84(1), PCG84(1) | 250 | 13 | 44 | 37.5 | 36 |
| PQ100, PQG100 | 250 | 13 | 44 | 37.5 | 32 |
| PQ160, PQG160 | 200 | 13 | 44 | 37.5 | 40 |
| BG352(1), BGG352(1) | 200 | 13 | 56 | 49.5 | 40 |
| BG432(1), BGG432(1) | 200 | 13 | 56 | 49.5 | 48 |
| BG560(1), BGG560(1) | 200 | 13 | 56 | 49.5 | 48 |
| SO8 | 750 | 7 | 12 | 9.2 | 8 |
| SO20 | 1000 | 13 | 24 | 21.0 | 12 |
| TQ100, TQG100 | 1000 | 13 | 24 | 21.0 | 32 |
| TQ144, TQG144 | 750 | 13 | 44 | 37.5 | 24 |
| VO8, VOG8 | 750 | 7 | 12 | 9.2 | 8 |
| VO20, VOG20 | 2500 | 13 | 16 | 13.3 | 12.0 |
| VQ44, VQG44 | 2000 | 13 | 24 | 21.0 | 16 |
| VQ64, VQG64 | 2000 | 13 | 24 | 21.0 | 16 |
| VQ100, VQG100 | 1000 | 13 | 24 | 21.0 | 32 |

**Note:**

1. In-house capability.

## Standard Bar Code Label Locations

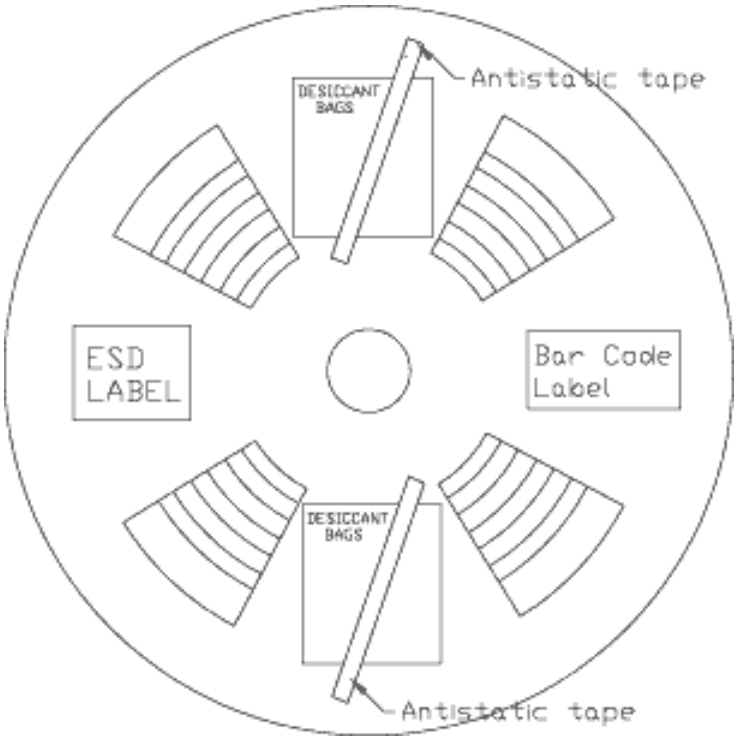


*Figure 2-1:* **Standard Bar Code Label Locations**

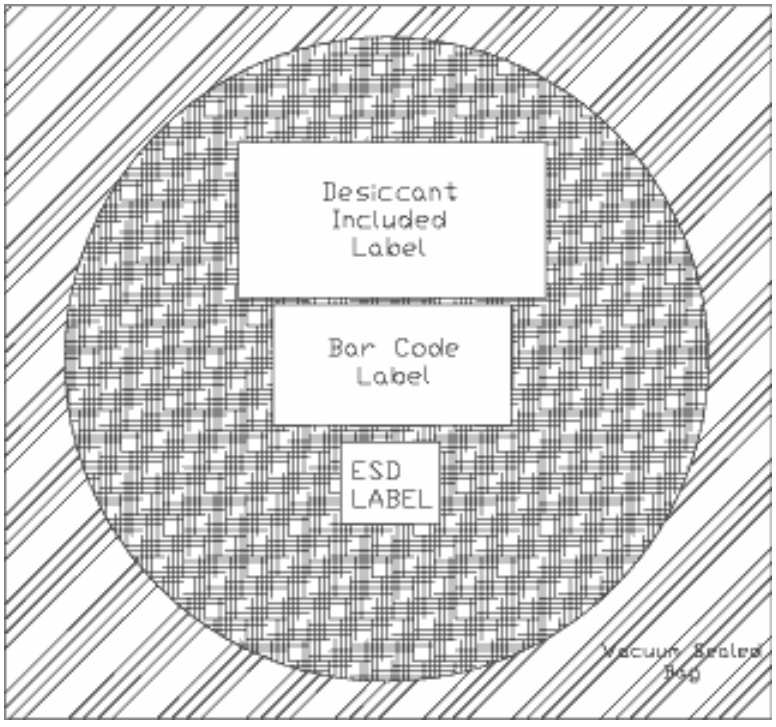


*Figure 2-2:* **Standard Bar Code Label Locations**

# Tubes

Tubes are used as unit carriers for most of Xilinx smaller packages. All of our tubes are coated with an antistatic material to protect the product from ESD damage.

*Table 2-2:* **Standard Device Quantities per Tube**

| Package | Full Tube Quantity | Max. Tube Qty. per ESD Bag (8.5" x 27") | Max. Tube Qty. per ESD Bag (12" X 27") |
|---|---|---|---|
| PC84, PCG84, WC84 | 15 | 24 | 40 |
| PC68, PCG68, WC68 | 18 | 36 | 50 |
| PC44, PCG44, CC44, WC44 | 26 | 40 | 50 |
| PC28, PCG28 | 37 | 40 | 50 |
| PC20, PCG20, CC20 | 46 | 50 | 60 |
| CD48 | 7 | 24 | 30 |
| PD48 | 7 | 24 | 30 |
| CD8 | 37 | 10 | 15 |
| PD8 | 50 | 50 | 60 |
| DD8 | 50 | 50 | 60 |
| SO24 | 31 | 40 | 50 |
| SO20 | 37 | 60 | 100 |
| SO8 | 98 | 240 | 350 |
| VO20, VOG20 | 74 | 240 | 350 |
| VO24 | 62 | 240 | 350 |
| VO8, VOG8 | 98 | 240 | 350 |

# Trays

Trays are used to pack most of Xilinx surface-mount devices since they provide excellent protection from mechanical damage. In addition, they are coated with antistatic material to provide protection against ESD damage and can withstand operation temperature of up to 150º C.

*Table 2-3:* **Standard Device Counts per tray and Box**

| Package | Max # of device per Tray | Max # of units in one internal box |
|---|---|---|
| BF957/BFG957 | 21 | 105 |
| BG225/BGG225, BG256/BGG256 | 40 | 200 |

*Table 2-3:* **Standard Device Counts per tray and Box *(Continued)***

| Package | Max # of device per Tray | Max # of units in one internal box |
|---|---|---|
| BG352/BGG352, BG492/BGG492, BG728/BGG728 | 24 | 120 |
| BG432/BGG432 | 21 | 105 |
| BG560/BGG560 | 12 | 60 |
| BG575/BGG575 | 27 | 135 |
| CB100, CB164, CB196, CB228 | 4 | 20 |
| CP56/CPG56 | 360 | 1800 |
| CP132/CPG132 | 360 | 1800 |
| CS48/CSG48 | 416 | 2080 |
| CS144/CSG144 | 198 | 990 |
| CS280/CSG280 | 119 | 595 |
| FG256/FGG256 | 90 | 450 |
| FG320/FGG320 | 84 | 420 |
| FG324/FGG324 | 60 | 300 |
| FG456/FGG456 | 60 | 300 |
| FG676/FGG676 | 40 | 200 |
| FG860 | 12 | 60 |
| FG900/FGG900 | 27 | 135 |
| FG680/FGG680 | 21 | 105 |
| FG1156/FGG1156 | 24 | 120 |
| FF668 / FFG668 | 40 | 200 |
| FF672/FFG672 | 40 | 200 |
| FF896/FFG896 | 27 | 135 |
| FF1148/FFG1148, FF1152/FFG1152 | 24 | 120 |
| FF1513/FFG1513, FF1517/FFG1517 | 21 | 105 |
| FF1696/FFG1696, FF1704/FFG1704 | 12 | 60 |
| FS48/FSG48 | 108 | 525 |

*Table 2-3:* **Standard Device Counts per tray and Box *(Continued)***

| Package | Max # of device per Tray | Max # of units in one internal box |
|---|---|---|
| FT256/FTG256 | 90 | 450 |
| HQ160/HQG160, HQ208/HQG208 | 24 | 120 |
| HQ240/HQG240 | 24 | 120 |
| HQ304 | 12 | 60 |
| HT144 | 60 | 300 |
| HT176 | 40 | 200 |
| PG68, PG84 | 40 | 200 |
| PG120 | 24 | 120 |
| PG132/PP132 | 21 | 105 |
| PG144 | 18 | 90 |
| PG156/PP156, PG175/PP175 | 14 | 70 |
| PG191, PG223 | 12 | 60 |
| PG299 | 10 | 50 |
| PG411, PG475, PG559 | 10 | 50 |
| PQ44/PQG44 | 96 | 480 |
| PQ100/PQG100 | 66 | 330 |
| PQ160/PQG160, PQ208/PQG208 | 24 | 120 |
| PQ240/PQG240 | 24 | 120 |
| QFG32 | 490 | 2450 |
| QFG48 | 260 | 1300 |
| SF363/SFG363 | 90 | 450 |
| TQ144, TQG144 | 60 | 300 |
| TQ160, TQ176 | 40 | 200 |
| TQ100/TQG100 | 90 | 450 |
| TQ128 | 72 | 360 |
| VO48/VOG48 | 96 | 480 |

*Table 2-3:* **Standard Device Counts per tray and Box *(Continued)***

| Package | Max # of device per Tray | Max # of units in one internal box |
|---|---|---|
| VQ44/VQG44, VQ64/VQG64 | 160 | 800 |
| VQ100/VQG100 | 90 | 450 |

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Chapter 3

# Thermal Management & Thermal Characterization Methods & Conditions

## Introduction

This chapter addresses the need to manage the heat generated in CMOS logic devices, an industrywide pursuit, and describes the measures Xilinx uses and recommends to its customers to quantify and manage potential thermal problems in FPGAs.

## Thermal Management

Modern high-speed logic devices consume an appreciable amount of electrical energy. This energy invariably turns into heat. Higher device integration drives technologies to produce smaller device geometry and interconnections. With chip sizes getting smaller and circuit densities at their highest levels, the amount of heat generated on these fast-switching CMOS circuits can be very significant. As an example, Xilinx Virtex-II Pro FPGA devices incorporate multiple processors, multiple-gigabit transceivers, digital-controlled impedance I/Os, and I/Os capable of supporting various high current standards. Special attention must be paid to addressing the heat removal needs for these devices.

The need to manage the heat generated in a modern CMOS logic device is not unique to Xilinx. This is a general industry pursuit. However, unlike the power needs of a typical industry application-specific integrated circuit (ASIC) gate array, the field-programmable device's power requirement is not determined in the factory. Customers' designs can vary in power as well as physical needs. This is the challenge in predicting FPGA thermal management needs.

There is no sure way of anticipating accurate power dissipation of an FPGA device short of actual measurement. Xilinx has developed several software-based power-estimator tools to help the end user predict power consumption. The tools can be useful as a first step. Like most tools, however, the predicted output depends on the work put into the predicting effort. In assigning packages to devices, effort has been made to tailor the packages to the power needs of typical users. For each device, suitable packages are typically chosen to handle "typical" designs and gate utilization for the device. For the most part, the choice of a package as the primary or internal heat removal casing works well without any external heat management. Increasingly, with highly integrated devices, the need arises for customers to utilize an FPGA device beyond "typical" design parameters. For these situations, the use of the primary package without external enhancement may not be adequate to address the heat removal needs of the device. It is for these cases that the need to manage the heat removal through external means becomes essential.

Heat has to be removed from a device to ensure that the device is maintained within its functional and maximum design temperature limits. If heat buildup becomes excessive,

the device's temperature may exceed the temperature limits. A consequence of this is that the device may fail to meet speed-files performance specifications. In addition to performance considerations, there is also the need to satisfy system reliability objectives by operating at a lower temperature. Failure mechanisms and failure rate of devices have an exponential dependence on devices' operating temperatures. Thus, the control of the package, and by extension device temperature, is essential to ensure product reliability.

# Package Thermal Characterization Methods and Conditions

## Characterization Methods

Xilinx uses several methods to obtain thermal performance characteristics of integrated circuit packages. The methods include thermal simulation using finite element software tools, and an indirect electrical method utilizing an isolated diode on a special thermal test die or even on a Xilinx FPGA housed in the package of interest. The majority of the data reported by Xilinx is based on the indirect diode method. Simulation tools, calibrated with actual measurement data, are used to supplement thermal collateral data generation. Most published compact thermal model data is based on such an effort.

## Calibration of Isolated Diode

In the direct electrical method, the forward-voltage drop of an isolated diode residing on a special test die or the temperature diode of the Xilinx FGPA is calibrated by applying a constant forcing current (from 0.100 mA to 0.500 mA) over a temperature range of 0 - 125 °C (degrees Celsius). The calibrated packaged device is then mounted on an appropriate board and placed in the testing environment — *e.g.*, still air or forced convection. Power ($\mathbf{P_D}$) is applied to the device through diffused resistors on the same thermal die. In the FPGA case, a known self-heating program is loaded and clocked to generate the monitored power. Usually, between 0.5 Watts to 4 Watts may be applied. Higher power (up to 10 watts) is possible, depending on the package. The resulting rise in junction temperature is monitored with the forward-voltage drop of the precalibrated diode.

## Simulation Methods

In the simulation effort, finite element (FEA) methodology is used to represent the packages of interest. The package geometrical details (based on CAD data), as well as the board stack-up details are captured. Published material properties are used as input to derive the thermal characteristics based on JEDEC environment and boundary conditions. Using sample test data, the FEA inputs and assumptions are optimized to minimize variation between measurement and simulation.

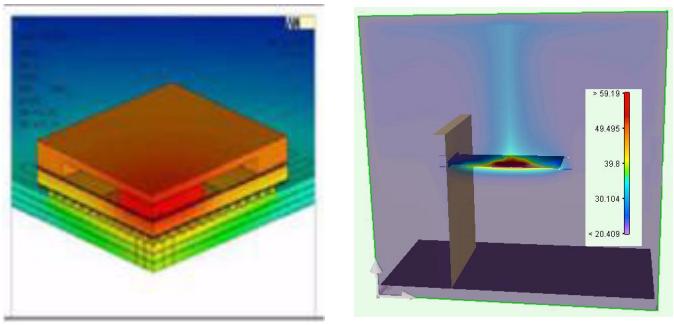



*Figure 3-1:* **Simulation Tool Outputs: a) Quarter Model of a Package, b) CTM in JEDEC Enclosure**

Once the simulation inputs and assumptions have been refined, the FEA method is used to obtain the thermal characteristics including thermal models of devices in a family using the same material set and construction details.

## Measurement Standards

Previously, Xilinx Thermal lab used the SEMI thermal test methods (#G38-87) and associated SEMI-based boards (#G42-87) to perform thermal characterization. Most of our recent measurements and simulations are based on provision of the JEDEC and EIA Standard — JESD51-n series specifications. It is our assessment that the latter standard offers some options that are not available in the SEMI method. We will continue to quote the SEMI-based data (designated by SEMI in the comment column) for older packages measured in the earlier era, and when we quote new data, they will be designated as JESD in the comment section.

It is also essential to note that these standard-based measurements give characterization results that allow packages and conditions to be compared. Like miles per gallon (MPG) figures quoted on new cars, the numbers should be used with caution. As specific user environments will not be identical to the conditions used in the characterization, the numbers quoted may not precisely predict the performance of the package in an application-specific environment.

For better in-system $\mathbf{T_J}$ prediction, Xilinx provides compact thermal models for its devices. Some of these are available in model libraries for download at the Download Center: http://www.xilinx.com/xlnx/xil_sw_updates_home.jsp

Models for older products may be requested from ctm_team@xilinx.com.

## Definition of Terms

$\mathbf{T_J}$ Junction Temperature, defined as the maximum temperature on the die, expressed in °C (degrees Celsius).

$\mathbf{T_A}$ Ambient Temperature, defined as the temperature of the surrounding environment, expressed in °C (degrees Celsius).

$\mathbf{T_C}$ Temperature of the package taken at a defined location on the body. In most situations, it is taken at the primary heat flow path on the package and will represent the hottest part on the package, expressed in °C. See the next item for when $\mathbf{T_C}$ is taken at the top.

**$T_t$** Temperature of the package body taken at the top location on the package. This is a special case of **$T_C$**.

**$T_B$** This is the board Temperature taken at a predefined location on the board near the component under test, expressed in °C.

**$T_I$** This is the isothermal fluid temperature when junction to case temperature is taken, expressed in °C.

**$P_D$** The total device power dissipation, expressed in Watts.

## Junction-to-Reference General Setup

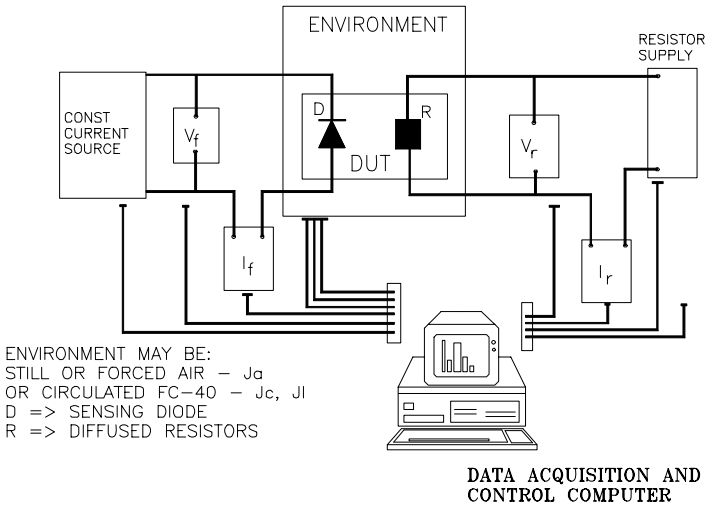



*Figure 3-2:* **Thermal Measurement Setup (Schematic for Junction to Reference)**

## Junction-to-Case Measurement — $\theta_{JC}$

**Theta-jc ($\theta_{JC}$)** measures the heat flow resistance between the die surface and the surface of the package (case). This data is relevant for packages used with external heatsinks. It assumes that heat is flowing through the top to the exclusion of the others. In the ideal case, all the heat is forced to escape the package at the path where **$T_C$** is taken. The lateral heat flow is not allowed or minimized so that the source of temperature differential will be attributable to the total known heat input.

*Figure 3-3:* **Theta JC Measurement Setup**

A copper heatsink plate at the top of the package is used in $\theta_{JC}$ methods to achieve the forced preferred directional flow.

Prior to 1999, the junction-to-case characterization on some heatsink packages was accomplished in a 3M Flourinert (FC-40) isothermal circulating fluid stabilized at 25°C. Current Xilinx data on $\theta_{JC}$ is simulated using the cold plate approach.

With applied power ($\mathbf{P_D}$) and under stabilized conditions, case temperature ($\mathbf{T_C}$) is measured with a low gauge thermocouple (36-40 AWG) at the primary heat-flow path of the particular package. Junction temperature ($\mathbf{T_J}$) is calculated from the diode forward-voltage drop from the initial stable condition before power is applied, *i.e.*,

$$\theta_{JC} = (T_J - T_C)/P_D$$

where the terms are as defined above. A poorly defined $\theta_{JC}$ condition usually leads to lower numbers being reported. In such cases, the recorded temperature difference (Tj-Tc) is the result of having a fraction of the power going through the path. However, in the calculation, the full power is used.

## Junction-to-Top Measurement — $\Psi_{JT}$

**Psi-jt ($\Psi_{JT}$)** is a junction to the top thermal parameter (*not thermal resistance*), defined in the JEDEC specification that shadows $\theta_{JC}$ in a real-world situation. This parameter provides correlation between chip junction temperature and the temperature of the package at the top. It is measured on a defined FR4-based PC board as described under $\theta_{JA}$. The reference temperature is the temperature monitored at the top of the component, $\mathbf{T_t}$. Though the cause of the temperature rise may not be caused by all the power applied, the full power is used in the calculation, *i.e.*,

$$\Psi_{JT} = (T_J - T_t)/P_D$$

where $\mathbf{P_D}$ is the full applied power.

The parameter value depends on airflow conditions. In heatsink type packages (some BGs and most FF packages) where the primary heat flow is almost one dimensional and the heat flux is confined to the top, $\mathbf{T_C}$ and $\mathbf{T_t}$ are taken at the same point and $\Psi_{JT}$ approaches $\theta_{JC}$.

In molded packages like Xilinx FG676, FG900 and FG1156, the one-dimensional condition is difficult to meet. At best, a fraction of the heat flux (~40 – 60%) goes to the top in the standardized setup. In an end-user application, the heat flux division may follow a similar pattern. Under such cases, psi-jt ($\Psi_{JT}$) and theta-jc ($\theta_{JC}$) tend to diverge from each other. If the total power is known, and the top temperature can be carefully measured, $\Psi_{JT}$ is used to predict the $T_J$ in application environment.

Xilinx does not provide **Psi-jt** numbers as they strongly depend on the application conditions.

## Junction-to-Ambient Measurement — $\theta_{JA}$

*Figure 3-4:* **Theta JA Measurement Setup**

SEMI method: Some of the data reported are based on the SEMI standard methods and associated board standards. $\theta_{JA}$ data reported as based on SEMI were measured on FR4-based PC boards measuring 4.5" x 6.0 x .0625" (114.3mm x 152.4mm x 1.6mm) with edge connectors. Several versions are available to handle various surface mount (SMT) devices. They are, however, grouped into two main types. Type I board (the equivalent of the JEDEC low-conductivity board) is single layer with two signal planes (one on each surface) and no internal Power/GND planes. This is the 2L/0P or 2S/0P board and the trace density on this board is less than 10% per side. The type II board (the equivalent of the JEDEC 2S/2P board) has two internal copper planes — one power and one ground. These planes are in addition to the two signal trace layers on both surfaces. This is the 4L/2P (four-layer, also referred to as 2S/2P) board.

JEDEC measurements: Packages are measured in a one foot-cube enclosure based on JEDS51-2. Test boards are fashioned per test board specification JESD51-3 and JESD51-7. The board sizes depend on the package and are typically 76.2mm x 114.3mm x 1.6mm or 101.6mm x 114.3mm x 1.6mm. These come in low-conductivity as well as high-conductivity versions.

Thermal resistance data may be taken with the package mounted in a socket or with the package mounted directly on traces on the board. Socket measurements typically use the 2S/0P or low-conductivity boards. SMT devices, on the other hand, may use either board. Published data always reflect the board and mount conditions used (ref 2S/0P or 4L/2P).

The board with the device under test (DUT) is mounted in the test enclosure and data is taken at the prevailing temperature and pressure conditions — between 20°C and 30°C ambient ($T_A$). Appropriate power is used, depending on the anticipated thermal resistance of the package. Applied power, signal monitoring — including the enclosure (ambient) temperatures are noted. The junction to ambient thermal resistance is calculated as follows:

$$\theta_{JA} = (T_J - T_A)/P_D$$

In the case of airflow measurement, this is done in a special airflow enclosure section of a suction-type low-velocity wind tunnel. Airflow velocities from 0-1000 Linear Feet per Minute (LFM), *i.e.*, 0-5.08 m/s, are used with very low turbulence. The controlling specification is JESD51-6. Airflow measurements use similar boards as $\theta_{JA}$ with air conditions noted with hot wire anemometer.

## Thermal Resistance: Junction-to-Board — $\theta_{JB}$

This is defined as:

$$\theta_{JB} = (T_J - T_B)/P_D$$

where $T_B$ is the board temperature at steady state measured at specified location on the board. $P_D$ is the actual power in Watts that produces the change in temperature.

$T_B$ is monitored on a board with a 40-gauge thermocouple at specific location in the proximity of the package leads or balls. As an example, for BGA package, the thermocouple is attached to a trace midway along the side of the package with the attachment point within 1mm of the package body.

Like $\theta_{JC}$, $\theta_{JB}$ depends on constrained flow in a preferred direction. In actual measurement or simulations the heat flow is forced to go preferably through the board by excluding other paths with insulation. The measurement conditions are not likely to be reproduced in a real application.

## Junction-to-Board Measurement — $\Psi_{JB}$

Junction-to-board thermal parameter — $\Psi_{JB}$ is a thermal parameter (*not thermal resistance*) defined by JEDEC specification that approximates $\theta_{JB}$ in a real-world situation. This parameter provides correlation between chip junction temperature and the temperature of the board. It is measured on a high effective thermal conductivity board as described under $\theta_{JA}$. The reference temperature is the temperature monitored on the board, $T_B$. Though the temperature rise may not be caused entirely by all the power applied, the full power is used in the calculation, *i.e.*,

$$\Psi_{JB} = (T_J - T_B)/P_D$$

where $P_D$ is the full applied power. This parameter is used to obtain chip temperature ($T_J$) in applications where the board temperature can be monitored as described.

Starting in 2005, Xilinx started providing $\Psi_{JB}$ for all new products. As a result, some limited theta-JB data exists, particularly for newer products. For older devices not sharing similar packages with the newer ones, $\Psi_{JB}$ based on our JEDEC board can be derived for them and these can be requested for the specific device package combination through Xilinx Technical Support.

## Data Acquisition and Package Thermal Database

Data for a package type is gathered for various die sizes, power levels, cooling modes (air flow and sometimes heatsink effects) with a Data Acquisition and Control System (DAS). The system controls and conditions the power supplies and other ancillary equipment for hands-free data taking. A package is completely characterized with respect to the major variables that influence the thermal resistance. A database is generated for the package. From the database, thermal resistance data is interpolated as typical values for the individual Xilinx devices that are assembled in the characterized package. Table 3-1 shows the typical values for various packages. It must be noted that specific device data may not be the same as the typical data listed for the package. However, the data will fall within the

min. and max. ranges given. The more widely a package is used across FPGA and CPLD families, the wider the range quoted here. If specific device data is required, customers may contact the Xilinx Technical Support for a detailed listing applicable to the device.

Data sheets for newer products may list device/package specific thermal data. Though data from such tables will be consistent with an updated version of this table, the data in those tables will be more device specific than the summary provided below.

*Table 3-1:* **Summary of Thermal Resistance for Packages**

| Pkg-Code | $\theta_{JA}$ still air (Max) | $\theta_{JA}$ still air (Typ) | $\theta_{JA}$ still air (Min) | $\theta_{JA}$ 250 LFM (Typ) | $\theta_{JA}$ 500 LFM (Typ) | $\theta_{JA}$ 750 LFM (Typ) | $\theta_{JC}$ (Typ) | Comments |
|---|---|---|---|---|---|---|---|---|
| | °C/Watt | °C/Watt | °C/Watt | °C/Watt | °C/Watt | °C/Watt | °C/Watt | |
| BF957 | 11.5 | 10.9 | 10.3 | 6.7 | 5.3 | 4.6 | 0.5 | JESD: 4L/2P-SMT Simulation |
| BFG957 | 11.4 | 10.9 | 10.6 | 6.8 | 5.3 | 4.6 | 0.5 | JESD: 4L/2P-SMT Simulation |
| BG225 | 37.2 | 30.6 | 23.9 | 22.1 | 19.5 | 18.7 | 3.6 | SEMI: 4L/2P-SMT |
| BG256 | 38.8 | 26.5 | 20.7 | 19.1 | 16.9 | 16.2 | 3.8 | SEMI: 4L/2P-SMT |
| BG313 | 19.2 | 19.2 | 19.2 | 13.9 | 12.3 | 11.8 | 1.5 | SEMI: 4L/2P-SMT |
| BG352 | 13.3 | 12.7 | 11.8 | 8.8 | 7.2 | 6.5 | 1.1 | SEMI: 4L/2P-SMT |
| BG432 | 12.8 | 11.3 | 10.7 | 7.9 | 6.5 | 5.9 | 0.9 | SEMI: 4L/2P-SMT |
| BG492 | 17.2 | 17.2 | 17.2 | 12.2 | 11.9 | 11.9 | 0.8 | SEMI: 4L/2P-SMT |
| BG560 | 11.2 | 10.6 | 10.2 | 7.5 | 6.1 | 5.6 | 0.8 | SEMI: 4L/2P-SMT |
| BG575 | 15.0 | 14.6 | 14.0 | 10.4 | 10.1 | 9.9 | 2.0 | JESD: 4L/2P-SMT Simulation |
| BG728 | 14.5 | 14.0 | 13.2 | 10.7 | 9.6 | 8.8 | 2.0 | JESD: 4L/2P-SMT Simulation |
| BGG256 | 29.6 | 27.3 | 24.5 | 19.7 | 17.4 | 16.7 | 4.7 | SEMI: 4L/2P-SMT |
| BGG352 | 13.3 | 12.9 | 12.5 | 9.0 | 7.3 | 6.7 | 1.1 | SEMI: 4L/2P-SMT |
| BGG432 | 11.8 | 11.4 | 11.1 | 8.0 | 6.6 | 6.0 | 0.9 | SEMI: 4L/2P-SMT |
| BGG560 | 10.7 | 10.6 | 10.4 | 7.5 | 6.1 | 5.6 | 0.8 | SEMI: 4L/2P-SMT |
| BGG575 | 14.7 | 14.5 | 14.0 | 10.3 | 10.1 | 9.4 | 2.0 | JESD: 4L/2P-SMT Simulation |
| BGG728 | 14.5 | 14.3 | 14.2 | 11.1 | 9.7 | 8.8 | 1.9 | JESD: 4L/2P-SMT Simulation |
| CB100 | 48.8 | 41.8 | 38.5 | 25.3 | 19.7 | 17.7 | 5.8 | SEMI: Socketed |
| CB164 | 29.8 | 26.7 | 25.0 | 16.6 | 12.4 | 10.6 | 3.7 | SEMI: Socketed |
| CB196 | 26.2 | 24.8 | 23.8 | 15.5 | 11.6 | 9.9 | 2.4 | SEMI: Socketed |
| CB228 | 21.3 | 18.6 | 16.3 | 11.6 | 8.7 | 7.4 | 1.7 | SEMI: Socketed |
| CC20 | 105.0 | 105.0 | 105.0 | 72.8 | 57.7 | 35.0 | 7.0 | SEMI: Socketed |
| CC44 | 48.6 | 46.5 | 44.5 | 38.2 | 31.2 | 25.6 | 9.3 | SEMI: Socketed |
| CD48 | 40.0 | 40.0 | 40.0 | | | | 5.0 | SEMI: Socketed |
| CD8 | 121.0 | 112.9 | 103.9 | 80.0 | 65.7 | 58.0 | 7.1 | SEMI: Socketed |
| CF1144 | 9.8 | 9.8 | 9.8 | 6.4 | 5.7 | 5.3 | 0.5 | JESD: 4L/2P-SMT Simulation |

*Table 3-1:* **Summary of Thermal Resistance for Packages *(Continued)***

| Pkg-Code | $\theta_{JA}$ still air (Max) °C/Watt | $\theta_{JA}$ still air (Typ) °C/Watt | $\theta_{JA}$ still air (Min) °C/Watt | $\theta_{JA}$ 250 LFM (Typ) °C/Watt | $\theta_{JA}$ 500 LFM (Typ) °C/Watt | $\theta_{JA}$ 750 LFM (Typ) °C/Watt | $\theta_{JC}$ (Typ) °C/Watt | Comments |
|---|---|---|---|---|---|---|---|---|
| CG1156 | 10.7 | 10.7 | 10.7 | 8.0 | 7.6 | 6.8 | 1.0 | JESD: 4L/2P-SMT Simulation |
| CG560 | 14.3 | 14.3 | 14.3 | 9.2 | 7.2 | 6.3 | 1.6 | SEMI: Socketed |
| CG717 | 11.4 | 11.4 | 11.4 | 8.6 | 7.9 | 7.7 | 4.2 | JESD: 4L/2P-SMT Simulation |
| CP132 | 72.4 | 54.8 | 41.4 | 48.8 | 46.5 | 44.8 | 12.9 | JESD: 4L/2P-SMT Simulation |
| CP56 | 66.0 | 65.4 | 63.0 | 59.8 | 57.7 | 56.6 | 14.7 | JESD: 4L/2P-SMT Simulation |
| CPG132 | 62.3 | 55.3 | 53.0 | 49.5 | 47.1 | 45.4 | 13.6 | JESD: 4L/2P-SMT Simulation |
| CPG56 | 66.0 | 66.0 | 65.5 | 60.1 | 58.1 | 57.0 | 14.8 | JESD: 4L/2P-SMT Simulation |
| CS144 | 34.0 | 34.0 | 34.0 | 25.9 | 23.9 | 23.2 | 2.8 | JESD: 4L/2P-SMT Simulation |
| CS280 | 30.5 | 30.5 | 30.5 | 25.0 | 23.1 | 23.2 | 0.8 | JESD: 4L/2P-SMT Simulation |
| CS48 | 45.0 | 45.0 | 45.0 | | | | 5.0 | Estimated |
| CSG144 | 34.0 | 34.0 | 34.0 | 26.0 | 23.9 | 23.2 | 2.8 | SEMI: 4L/2P-SMT |
| CSG280 | 30.5 | 30.5 | 30.5 | 25.0 | 23.1 | 23.2 | 1.9 | SEMI: 4L/2P-SMT |
| CSG48 | 45.0 | 45.0 | 45.0 | | | | 5.0 | Estimated |
| DD8 | 115.9 | 108.4 | 94.0 | 89.0 | 72.8 | 59.6 | 8.0 | SEMI: Socketed |
| FF1148 | 11.0 | 10.7 | 9.7 | 6.5 | 5.2 | 4.5 | 0.4 | JESD: 4L/2P-SMT Simulation |
| FF1152 | 11.5 | 10.9 | 9.9 | 6.7 | 5.3 | 4.4 | 0.5 | JESD: 4L/2P-SMT Simulation |
| FF1513 | 9.7 | 9.3 | 9.1 | 5.6 | 4.5 | 4.1 | 9.53E-02 | JESD: 4L/2P-SMT Simulation |
| FF1517 | 11.4 | 10.8 | 8.6 | 6.8 | 5.4 | 4.6 | 0.5 | JESD: 4L/2P-SMT Simulation |
| FF1696 | 8.6 | 8.6 | 8.6 | 5.4 | 4.2 | 3.6 | 0.4 | JESD: 4L/2P-SMT Simulation |
| FF1704 | 9.0 | 8.8 | 8.6 | 5.5 | 4.3 | 3.7 | 0.4 | JESD: 4L/2P-SMT Simulation |
| FF1760 | 7.7 | 7.7 | 7.7 | 4.6 | 3.7 | 3.3 | 0.1 | JESD: 4L/2P-SMT Simulation |
| FF668 | 14.2 | 13.3 | 12.4 | 8.7 | 7.3 | 6.7 | 0.4 | JESD: 4L/2P-SMT Simulation |
| FF672 | 15.7 | 13.9 | 12.0 | 9.7 | 8.1 | 7.2 | 0.5 | JESD: 4L/2P-SMT Simulation |

*Table 3-1:* **Summary of Thermal Resistance for Packages *(Continued)***

| Pkg-Code | $\theta_{JA}$ still air (Max) | $\theta_{JA}$ still air (Typ) | $\theta_{JA}$ still air (Min) | $\theta_{JA}$ 250 LFM (Typ) | $\theta_{JA}$ 500 LFM (Typ) | $\theta_{JA}$ 750 LFM (Typ) | $\theta_{JC}$ (Typ) | Comments |
|---|---|---|---|---|---|---|---|---|
| | °C/Watt | °C/Watt | °C/Watt | °C/Watt | °C/Watt | °C/Watt | °C/Watt | |
| FF676 | 14.1 | 13.7 | 13.3 | 9.0 | 7.5 | 6.9 | 0.5 | JESD: 4L/2P-SMT Simulation |
| FF896 | 11.8 | 11.5 | 11.1 | 7.4 | 6.2 | 5.4 | 0.6 | JESD: 4L/2P-SMT Simulation |
| FFG1148 | 11.0 | 11.0 | 10.9 | 6.7 | 5.2 | 4.5 | 0.6 | JESD: 4L/2P-SMT Simulation |
| FFG1152 | 11.2 | 10.9 | 10.5 | 6.8 | 5.3 | 4.4 | 0.6 | JESD: 4L/2P-SMT Simulation |
| FFG1517 | 11.3 | 10.7 | 10.4 | 6.7 | 5.3 | 4.6 | 0.5 | JESD: 4L/2P-SMT Simulation |
| FFG1696 | 8.6 | 8.6 | 8.6 | 5.4 | 4.2 | 3.6 | 0.4 | JESD: 4L/2P-SMT Simulation |
| FFG1704 | 9.0 | 8.7 | 8.6 | 5.5 | 4.3 | 3.7 | 0.4 | JESD: 4L/2P-SMT Simulation |
| FFG896 | 11.8 | 11.4 | 11.1 | 7.0 | 6.0 | 5.2 | 0.6 | JESD: 4L/2P-SMT Simulation |
| FFR1152 | 11.2 | 11.0 | 10.7 | 6.8 | 5.3 | 4.5 | 0.6 | JESD: 4L/2P-SMT Simulation |
| FFR896 | 11.1 | 11.1 | 11.1 | 6.1 | 5.8 | 5.2 | 0.6 | JESD: 4L/2P-SMT Simulation |
| FG1156 | 14.7 | 13.7 | 12.6 | 10.4 | 9.4 | 8.6 | 2.0 | JESD: 4L/2P-SMT Simulation |
| FG256 | 32.1 | 22.3 | 15.7 | 16.9 | 15.6 | 14.8 | 4.4 | SEMI: 4L/2P-SMT |
| FG320 | 30.0 | 23.4 | 20.3 | 17.9 | 16.7 | 16.0 | 10.5 | SEMI: 4L/2P-SMT |
| FG324 | 39.3 | 32.5 | 26.9 | 23.2 | 20.8 | 19.9 | 4.4 | SEMI: 4L/2P-SMT |
| FG400 | 25.1 | 22.7 | 20.1 | 17.6 | 16.4 | 15.8 | 10.2 | SEMI: 4L/2P-SMT |
| FG456 | 23.5 | 19.6 | 16.5 | 14.6 | 13.3 | 12.7 | 4.8 | SEMI: 4L/2P-SMT |
| FG484 | 20.6 | 18.8 | 16.7 | 13.7 | 12.6 | 12.0 | 8.9 | SEMI: 4L/2P-SMT |
| FG556 | 13.7 | 13.6 | 13.5 | 9.7 | 9.4 | 9.4 | 2.0 | SEMI: 4L/2P-SMT |
| FG580 | 12.5 | 12.2 | 12.1 | 8.5 | 6.9 | 6.3 | 1.0 | SEMI: 4L/2P-SMT |
| FG676 | 18.1 | 15.0 | 12.5 | 10.4 | 9.1 | 8.5 | 3.8 | SEMI: 4L/2P-SMT |
| FG680 | 11.1 | 10.8 | 10.4 | 7.6 | 6.2 | 5.7 | 1.1 | SEMI: 4L/2P-SMT |
| FG860 | 10.5 | 10.3 | 10.0 | 7.2 | 5.9 | 5.4 | 0.9 | SEMI: 4L/2P-SMT |
| FG900 | 15.7 | 12.9 | 11.2 | 9.0 | 8.0 | 7.5 | 2.8 | SEMI: 4L/2P-SMT |
| FGG1156 | 14.7 | 14.0 | 13.3 | 11.0 | 9.6 | 8.7 | 1.9 | SEMI: 4L/2P-SMT |
| FGG256 | 31.4 | 22.9 | 19.6 | 17.4 | 16.1 | 15.3 | 4.7 | SEMI: 4L/2P-SMT |
| FGG320 | 24.5 | 22.2 | 20.3 | 16.7 | 15.5 | 14.8 | 9.4 | SEMI: 4L/2P-SMT |
| FGG324 | 35.5 | 34.5 | 33.5 | 25.0 | 22.1 | 21.1 | 4.1 | SEMI: 4L/2P-SMT |
| FGG456 | 22.6 | 19.0 | 17.1 | 13.9 | 12.7 | 12.1 | 5.7 | SEMI: 4L/2P-SMT |

*Table 3-1:* **Summary of Thermal Resistance for Packages *(Continued)***

| Pkg-Code | $\theta_{JA}$ still air (Max) | $\theta_{JA}$ still air (Typ) | $\theta_{JA}$ still air (Min) | $\theta_{JA}$ 250 LFM (Typ) | $\theta_{JA}$ 500 LFM (Typ) | $\theta_{JA}$ 750 LFM (Typ) | $\theta_{JC}$ (Typ) | Comments |
|---|---|---|---|---|---|---|---|---|
| | °C/Watt | °C/Watt | °C/Watt | °C/Watt | °C/Watt | °C/Watt | °C/Watt | |
| FGG676 | 18.1 | 14.9 | 12.5 | 10.3 | 9.0 | 8.4 | 3.8 | SEMI: 4L/2P-SMT |
| FGG680 | 11.1 | 10.8 | 10.4 | 7.6 | 6.2 | 5.7 | 1.1 | SEMI: 4L/2P-SMT |
| FGG860 | 10.5 | 10.3 | 10.1 | 7.2 | 5.9 | 5.4 | 0.9 | SEMI: 4L/2P-SMT |
| FGG900 | 14.3 | 12.9 | 11.2 | 9.0 | 7.9 | 7.4 | 2.8 | SEMI: 4L/2P-SMT |
| FS48 | 45.0 | 45.0 | 45.0 | 38.2 | 35.2 | 33.2 | 3.7 | SEMI: 4L/2P-SMT |
| FT256 | 35.8 | 25.8 | 19.7 | 20.2 | 19.0 | 18.5 | 6.3 | SEMI: 4L/2P-SMT |
| FTG256 | 35.0 | 25.6 | 19.7 | 19.9 | 18.7 | 18.3 | 6.1 | SEMI: 4L/2P-SMT |
| HQ160 | 16.5 | 15.7 | 14.7 | 10.8 | 8.7 | 7.8 | 2.0 | SEMI: 4L/2P-SMT |
| HQ208 | 16.7 | 15.8 | 14.4 | 10.9 | 8.8 | 7.8 | 2.1 | SEMI: 4L/2P-SMT |
| HQ240 | 14.5 | 13.2 | 11.8 | 9.1 | 7.3 | 6.6 | 1.5 | SEMI: 4L/2P-SMT |
| HQ304 | 11.3 | 10.6 | 10.0 | 7.1 | 5.6 | 4.9 | 1.1 | SEMI: 4L/2P-SMT |
| HQG208 | 16.3 | 16.3 | 16.3 | 11.3 | 9.1 | 8.1 | 2.4 | SEMI: 4L/2P-SMT |
| HQG240 | 13.9 | 12.9 | 12.5 | 8.9 | 7.1 | 6.4 | 1.4 | SEMI: 4L/2P-SMT |
| HT144 | 19.1 | 18.6 | 18.2 | 12.7 | 10.8 | 10.2 | 2.1 | SEMI: 4L/2P-SMT |
| HT176 | 15.6 | 15.4 | 15.2 | 10.5 | 8.9 | 8.4 | 2.0 | SEMI: 4L/2P-SMT |
| HT208 | 13.6 | 13.5 | 13.3 | 9.1 | 7.7 | 7.2 | 1.9 | SEMI: 4L/2P-SMT |
| MQ208 | 18.4 | 17.8 | 17.4 | 14.0 | 12.6 | 11.9 | 1.3 | SEMI: 4L/2P-SMT |
| MQ240 | 16.8 | 16.7 | 16.4 | 12.0 | 10.8 | 10.5 | 1.2 | SEMI: 4L/2P-SMT |
| PC20 | 87.3 | 80.9 | 72.0 | 61.0 | 54.6 | 50.9 | 21.6 | SEMI: Socketed |
| PC28 | 67.6 | 66.1 | 63.0 | 49.8 | 44.6 | 41.6 | 17.8 | SEMI: Socketed |
| PC44 | 55.1 | 47.1 | 42.3 | 35.5 | 31.8 | 29.7 | 16.1 | SEMI: Socketed |
| PC68 | 46.2 | 41.8 | 38.4 | 31.5 | 28.2 | 26.3 | 9.4 | SEMI: Socketed |
| PC84 | 41.7 | 33.2 | 27.9 | 25.7 | 20.8 | 16.8 | 5.5 | SEMI: Socketed |
| PCG20 | 82.1 | 77.1 | 72.0 | 58.1 | 52.0 | 48.5 | 15.9 | SEMI: Socketed |
| PCG44 | 55.1 | 50.3 | 43.2 | 37.9 | 33.9 | 31.7 | 22.7 | SEMI: Socketed |
| PCG84 | 37.7 | 37.0 | 36.3 | 28.6 | 23.2 | 18.7 | 8.1 | SEMI: Socketed |
| PD48 | 43.2 | 43.2 | 43.2 | 32.6 | 29.1 | 27.2 | 11.6 | SEMI: Socketed |
| PD8 | 83.0 | 77.7 | 71.3 | 58.6 | 52.4 | 48.9 | 19.7 | SEMI: Socketed |
| PDG8 | 82.9 | 76.4 | 71.5 | 57.6 | 51.5 | 48.0 | 17.5 | SEMI: Socketed |
| PG120 | 37.8 | 27.6 | 24.6 | 19.1 | 15.1 | 13.1 | 3.9 | SEMI: Socketed |
| PG132 | 32.0 | 28.6 | 23.9 | 20.3 | 16.6 | 14.7 | 2.9 | SEMI: Socketed |
| PG144 | 25.8 | 24.5 | 23.3 | 17.4 | 14.3 | 12.6 | 3.7 | SEMI: Socketed |
| PG156 | 25.6 | 24.0 | 20.7 | 15.0 | 11.6 | 10.4 | 2.7 | SEMI: Socketed |
| PG175 | 25.2 | 23.3 | 19.9 | 14.5 | 11.3 | 10.0 | 2.6 | SEMI: Socketed |
| PG191 | 25.7 | 21.7 | 18.5 | 15.4 | 12.6 | 11.2 | 1.5 | SEMI: Socketed |
| PG223 | 25.3 | 21.0 | 17.7 | 14.9 | 12.2 | 10.8 | 1.5 | SEMI: Socketed |
| PG299 | 21.0 | 17.1 | 15.1 | 10.5 | 8.6 | 8.0 | 2.0 | SEMI: Socketed |

*Table 3-1:* **Summary of Thermal Resistance for Packages *(Continued)***

| Pkg-Code | $\theta_{JA}$ still air (Max) | $\theta_{JA}$ still air (Typ) | $\theta_{JA}$ still air (Min) | $\theta_{JA}$ 250 LFM (Typ) | $\theta_{JA}$ 500 LFM (Typ) | $\theta_{JA}$ 750 LFM (Typ) | $\theta_{JC}$ (Typ) | Comments |
|---|---|---|---|---|---|---|---|---|
| | °C/Watt | °C/Watt | °C/Watt | °C/Watt | °C/Watt | °C/Watt | °C/Watt | |
| PG411 | 16.1 | 14.7 | 14.3 | 9.5 | 7.4 | 6.5 | 1.5 | SEMI: Socketed |
| PG475 | 15.1 | 14.4 | 14.3 | 9.3 | 7.2 | 6.4 | 1.5 | SEMI: Socketed |
| PG559 | 13.7 | 13.3 | 13.2 | 8.6 | 6.7 | 5.9 | 1.4 | SEMI: Socketed |
| PG68 | 38.8 | 37.0 | 34.1 | 25.6 | 19.9 | 17.3 | 7.8 | SEMI: Socketed |
| PG84 | 38.5 | 34.4 | 31.3 | 23.8 | 18.5 | 16.1 | 6.0 | SEMI: Socketed |
| PP132 | 35.4 | 33.9 | 29.1 | 23.1 | 17.6 | 16.7 | 5.7 | SEMI: Socketed |
| PP175 | 29.5 | 28.9 | 28.1 | 19.5 | 14.9 | 12.8 | 2.6 | SEMI: Socketed |
| PQ100 | 35.0 | 33.4 | 32.0 | 29.5 | 27.5 | 26.6 | 5.5 | SEMI: 4L/2P-SMT |
| PQ160 | 38.1 | 31.4 | 20.6 | 23.1 | 20.5 | 19.0 | 5.0 | SEMI: 2L/0P-SMT |
| PQ208 | 37.7 | 30.3 | 18.9 | 22.3 | 19.7 | 18.3 | 4.9 | SEMI: 2L/0P-SMT |
| PQ240 | 28.5 | 19.4 | 14.0 | 14.3 | 12.7 | 11.7 | 3.8 | SEMI: 2L/0P-SMT |
| PQ44 | 52.2 | 51.3 | 50.1 | 39.8 | 36.4 | 35.4 | 12.4 | SEMI: 4L/2P-SMT |
| PQG100 | 34.4 | 33.8 | 33.3 | 29.8 | 27.9 | 26.9 | 5.8 | SEMI: 4L/2P-SMT |
| PQG160 | 36.4 | 29.7 | 24.1 | 21.9 | 19.4 | 17.9 | 7.0 | SEMI: 2L/0P-SMT |
| PQG208 | 37.5 | 34.7 | 31.1 | 25.6 | 22.6 | 21.0 | 6.9 | SEMI: 2L/0P-SMT |
| PQG240 | 29.9 | 24.9 | 22.1 | 18.4 | 16.3 | 15.1 | 5.4 | SEMI: 2L/0P-SMT |
| QF32 | 45.8 | 45.8 | 45.8 | 40.0 | 35.9 | 34.8 | 7.8 | SEMI: 2L/0P-SMT |
| QF48 | 36.8 | 36.8 | 36.8 | 32.1 | 28.8 | 28.0 | 5.3 | SEMI: 2L/0P-SMT |
| QFG32 | 45.8 | 45.8 | 45.8 | 40.0 | 35.9 | 34.8 | 7.8 | SEMI: 2L/0P-SMT |
| QFG48 | 36.8 | 36.8 | 36.8 | 32.1 | 28.8 | 28.0 | 5.3 | SEMI: 2L/0P-SMT |
| SF363 | 20.8 | 20.2 | 19.0 | 14.3 | 12.5 | 11.6 | 0.5 | SEMI: 2L/0P-SMT |
| SO16 | 106.0 | 106.0 | 106.0 | - | - | - | 47.0 | Vendor data |
| SO20 | 86.0 | 86.0 | 86.0 | 65.4 | 61.1 | 57.6 | 36.0 | Vendor data |
| SO24 | 80.0 | 80.0 | 80.0 | 60.8 | 56.8 | 53.6 | 28.0 | Vendor data |
| SO8 | 147.1 | 147.1 | 147.1 | 112.1 | 104.5 | 98.6 | 48.3 | IEEE(ref) |
| SOG20 | 86.0 | 86.0 | 86.0 | 65.4 | 61.1 | 57.6 | 36.0 | IEEE(ref) |
| SOG8 | 147.1 | 147.1 | 147.1 | 111.8 | 104.4 | 98.5 | 48.3 | IEEE(ref) |
| TQ100 | 39.5 | 31.9 | 30.6 | 25.9 | 24.1 | 23.5 | 7.5 | SEMI: 4L/2P-SMT |
| TQ128 | 31.5 | 30.6 | 30.0 | 26.9 | 25.2 | 24.3 | 5.3 | SEMI: 4L/2P-SMT |
| TQ144 | 52.1 | 32.8 | 29.8 | 25.5 | 21.8 | 20.4 | 5.6 | SEMI: 4L/2P-SMT |
| TQ160 | 28.9 | 28.9 | 28.9 | 21.8 | 18.5 | 17.0 | 5.6 | SEMI: 4L/2P-SMT |
| TQ176 | 29.7 | 28.1 | 26.7 | 21.3 | 18.0 | 16.5 | 5.3 | SEMI: 4L/2P-SMT |
| TQ44 | 44.7 | 44.3 | 43.8 | 36.8 | 34.4 | 33.6 | 8.2 | SEMI: 4L/2P-SMT |
| TQG100 | 39.5 | 34.2 | 30.7 | 27.7 | 25.8 | 25.2 | 8.0 | SEMI: 4L/2P-SMT |
| TQG144 | 50.0 | 35.4 | 30.7 | 27.5 | 23.5 | 22.1 | 6.5 | SEMI: 4L/2P-SMT |
| VO8 | 160.0 | 160.0 | 160.0 | 137.6 | 129.6 | 123.2 | 60.0 | Estimated |
| VO20 | 73.2 | 73.2 | 73.2 | 66.6 | 63.5 | 60.5 | 17.0 | Vendor data |

*Table 3-1:* **Summary of Thermal Resistance for Packages *(Continued)***

| Pkg-Code | $\theta_{JA}$ still air (Max) | $\theta_{JA}$ still air (Typ) | $\theta_{JA}$ still air (Min) | $\theta_{JA}$ 250 LFM (Typ) | $\theta_{JA}$ 500 LFM (Typ) | $\theta_{JA}$ 750 LFM (Typ) | $\theta_{JC}$ (Typ) | Comments |
|---|---|---|---|---|---|---|---|---|
| | °C/Watt | °C/Watt | °C/Watt | °C/Watt | °C/Watt | °C/Watt | °C/Watt | |
| VO24 | 76.0 | 76.0 | 76.0 | 57.8 | 54.0 | 50.9 | 28.0 | Estimated |
| VO48 | 63.4 | 62.9 | 62.4 | - | - | - | 14.5 | Vendor data |
| VOG8 | 160.0 | 160.0 | 160.0 | 137.6 | 129.6 | 123.2 | 60.0 | Estimated |
| VQ100 | 53.2 | 39.3 | 32.4 | 32.7 | 30.5 | 29.7 | 9.5 | SEMI: 4L/2P-SMT |
| VQ44 | 47.7 | 42.8 | 38.9 | 35.6 | 33.3 | 32.5 | 8.2 | SEMI: 4L/2P-SMT |
| VQ64 | 46.9 | 42.3 | 39.3 | 35.2 | 32.9 | 32.1 | 8.2 | SEMI: 4L/2P-SMT |
| VQG100 | 53.2 | 44.8 | 39.0 | 37.3 | 34.7 | 33.9 | 11.5 | SEMI: 4L/2P-SMT |
| VQG44 | 47.7 | 43.3 | 39.1 | 36.1 | 33.7 | 32.9 | 8.2 | SEMI: 4L/2P-SMT |
| VQG64 | 46.9 | 45.6 | 43.9 | 38.0 | 35.5 | 34.6 | 8.2 | SEMI: 4L/2P-SMT |

**Notes:**

- The maximum, typical and minimum numbers reported here are based on numbers for all the devices for the specific package at the time of compilation. The numbers do not necessarily reflect the absolute limits of that package. Specific device data should lie within the limits. Packages used for a broader spectrum of devices have a wider range in the table. Specific device data in a package may be obtained from Technical Support.
- Data is listed alphabetically by the Xilinx package code. Package configurations and drawings corresponding to these codes can be found in the section of the databook with package outline drawings.
- In the comment section, 2L/0P-SMT implies that the data was taken from a surface-mount type I board or low-conductivity type board — no internal planes on the board.
- 4L/2P-SMT (2S/2P) implies that the data was taken from a four-layer SMT board incorporating two internal planes. We have included SEMI and JESD to designate what method the data came from.
- Socketed data is also specified where applicable.
- Thermal data is in degrees Celsius/Watt. JA refers to $\theta_{JA}$. Airflow is in linear feet per minute (LFM). 500 LFM = 2.5 meters per second.

# Support for Compact Thermal Models (CTM)

Table 3-1 provides the traditional thermal resistance data for all Xilinx packages. This resistance data is measured using a prescribed JEDEC standard that might not necessarily reflect the actual user environment. The quoted $\theta_{JA}$, and $\theta_{JC}$ numbers are environmentally dependent, and JEDEC has traditionally recommended that these be used with that awareness. For more accurate junction temperature prediction, these might not be enough, and a system level thermal simulation might be required.

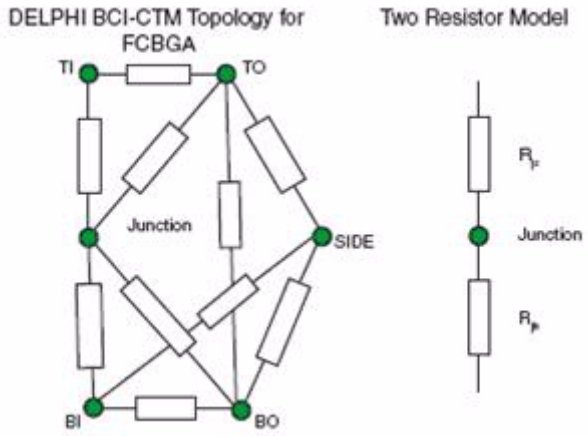



*Figure 3-5:* **Compact Thermal model Topologies**

Though Xilinx will continue to support these figure of merit data, for newer high performance devices such as Virtex-4, boundary condition independent compact thermal models (BCI-CTM) are available to assist end users in their thermal simulations. Two resistor models, as well as 8 to 10 resistor network models, are offered for these devices. These compact models seek to capture the thermal behavior of the packages more accurately at pre-determined critical points (junction, case, top, leads, etc.) with the reduced set of nodes. Unlike a full 3-D model, these are computationally efficient and work well in an integrated system simulation environment. Delphi CTMs for newer high performance devices are available on Xilinx Support Download Center: http://www.xilinx.com/xlnx/xil_sw_updates_home.jsp.

Models for older products can be requested from: ctm_team@xilinx.com.

# Application of Thermal Resistance Data

Thermal resistance data is used to gauge the IC package thermal performance. There are several ways to express the thermal resistance between two points. The following are a few of them:

- $\theta_{JA}$ = Junction to ambient thermal resistance (°C/W).
- $\theta_{JC}$ = Junction to case thermal resistance (°C/W)
- $\theta_{JB}$ = Junction to board thermal resistance (°C/W)
- $\theta_{CA}$ = Case to ambient thermal resistance (°C/W)
- $\theta_{CS}$ = Case to heatsink thermal resistance (°C/W)
- $\theta_{SA}$ = Heatsink to ambient thermal resistance (°C/W)

Other thermal parameters include

- $\Psi_{JB}$ = Junction to board thermal characteristic parameter (°C/W)
- $\Psi_{JT}$ = Junction to package thermal characteristic parameter (°C/W)

$\theta_{JC}$ measures the internal package resistance to heat conduction from the die surface, through the die mount material to the package exterior. $\theta_{JC}$ strongly depends on the package material's heat conductivity and geometrical considerations.

$\theta_{JA}$ measures the total package thermal resistance including $\theta_{JC}$. $\theta_{JA}$ depends on the package material properties and such external conditions as convective efficiency and board mount conditions. For example, a package mounted on a socket may have a $\theta_{JA}$ value 20% higher than the same package mounted on a four-layer board with power and ground planes.

In general, $\theta_{MN}$ expresses the thermal resistance between points **M** and **N**. In the above expression, the "source" and "end" points are indicated.

In situations where a heatsink is used with a heatsink compound, thermal resistance of heatsink is referenced as $\theta_{SA}$ (sink-to-ambient) and the attached material as $\theta_{CS}$ (case-to-heatsink). These thermal resistances may be added. For example, $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$ is an expression used in heatsink situations with interface material resistance $\theta_{CS}$.

# Thermal Data Usage

***Note:*** Actual thermal resistance in a system can be impacted by several user conditions. In the examples that follow, it should be noted that unique user conditions will impact predictions and estimates. Such user conditions have not been taken into consideration in the examples. One of the main influences on thermal resistance is board conditions. Figure 3-8 shows a table that illustrates how the thermal resistance of a Flip-Chip package (FF1148) is influenced by the board characteristics. The package with a high conductivity JEDEC board-based measured theta-ja of 9.1°C/watt can exhibit almost a 50% reduction in theta-ja if a 10" square board with 16 copper layers is used. Other user boundary conditions can also affect the effective thermal resistance in a system. Figure 3-7 depicts the impact when airflow is applied to packages. In general, as users work their way through these examples, external influences have not been taken into account in the estimates.

The following are some data requirements for using thermal resistance in an application.

- Xilinx-supplied data:
  - $\theta_{JA}$ — quoted from Xilinx database. Data may be obtained by contacting Xilinx Technical Support.
  - $\theta_{JC}$ — quoted from Xilinx database. Data may be obtained by contacting Xilinx Technical Support.
  - $\theta_{SA}$ — quoted by heatsink supplier.
- Items that the user may need to supply.
  - $\mathbf{T_J}$-max:
    - This may go as high as the absolute maximum temperature for the package — typically 125°C to 135°C for plastic
    - Note that components are tested to meet the speed file specifications at the temperatures associated with them - 85°C for C grade, and higher I and M grades. Running the parts at higher $\mathbf{T_J}$ than specified may not meet the specifications.
    - The user will have to pick a $\mathbf{T_J}$-max for reliability considerations, and plan the thermal budget around that
  - $\mathbf{T_A}$: Ambient in a system
    - This is also another variable that the user can control. Typically, this is set to approximately 45°C to 55°C.
- Items usually estimated:
  - Power dissipation. The thermal equation may be used to determine a power range that can satisfy some given conditions
  - Also, if power is known, $\mathbf{T_J}$-max may be calculated from the equations
  - If the temperature on the top of a bare part is well monitored in a system (not the way $\theta_{JC}$ is measured), the thermal parameter $\Psi_{JT}$ can be used to get junction temperature
  - Similarly, a well monitored board temperature can be used to predict junction with the $\Psi_{JB}$ parameter

In non-heatsink situations, the following inequality formula should hold:

$$\mathbf{T_J}(\text{max}) > \theta_{JA} * \mathbf{P_D} + \mathbf{T_A}$$

The two examples below illustrate the use of the above inequality formula. Specific packages have been used in the examples, but any package—Quad, BGA, FGs, or even Flip-Chip-based BGs—will be applicable.

## Example 1

The manufacturer's goal is to achieve Tj (max) < 85°C

A module is designed for a Ta = 45°C max.

An XCV300 in a FG456 has a $\theta_{JA}$ = 16.5°C/watt. $\theta_{JC}$ = 2.0°C/Watt.

Given a XCV300 with a logic design with a rated power $\mathbf{P_D}$ of 2.0 Watts.

With this information, the maximum die temperature can be calculated as:

$\mathbf{T_J}$ = 45 + (16.5 x 2.0) = 78°C.

The system manufacturer's goal of $\mathbf{T_J}$ < 85°C is met in this case.

## Example 2

A module has a $\mathbf{T_A}$ = 55°C max.

The Xilinx FPGA XCV400E is in a PQ240 package.

A logic design in XCV400E is determined to be 2.70 Watts. The module manufacturer's goal is to achieve $\mathbf{T_J}$(max.) < 100°C.

Table 3-2 shows the package and thermal enhancement combinations required to meet the goal of $\mathbf{T_J}$ < 100°C.

*Table 3-2:* **Thermal Resistance for XC4013E in PQ240 and HQ240 Packages**

| Device Name | Package | $\theta_{JA}$ still air | $\theta_{JA}$ (250 LFM) | $\theta_{JA}$ (500 LFM) | $\theta_{JA}$ (750 LFM) | $\theta_{JC}$ | Comments |
|---|---|---|---|---|---|---|---|
| XCV400E | PQ240 | 17.9 | 13.2 | 11.7 | 10.8 | 3.2 | Cu, SMT 2L/0P |

For all solutions, the junction temperature is calculated as: $\mathbf{T_J}$ = Power x $\theta_{JA}$ + $\mathbf{T_A}$. All solutions meet the module requirement of less than 100°C, with the exception of the PQ240 package in still air. In general, depending on ambient and board temperatures conditions, and most importantly the total power dissipation, thermal enhancements such as forced air cooling, heat sinking, etc., may be necessary to meet the $\mathbf{T_J}$ (max) conditions set.

Possible Solutions to meet the module requirements of 100°C:

a. Using the standard PQ240: $\mathbf{T_J}$ = 55 + (17.9 x 2.70) = 103.33 °C.

b. Using standard PQ240 with 250 LFM forced air: $\mathbf{T_J}$ = 55 + (13.2 x 2.70) = 90.64 °C.

## Heatsink Calculation

Example illustrating the use of heatsink:

Device is **XCV1000E-FG680 –**

There is a need for external thermal enhancements.

Data supplied from Xilinx on XCV1000E-FG680 is shown in Table 3-3

*Table 3-3:* **Data supplied from Xilinx on XCV1000E-FG680**

| Package Code | $\theta_{JA}$ still air | JC °C/W | $\theta_{JA}$ (250 LFM) | $\theta_{JA}$ (500 LFM) | $\theta_{JA}$ (750 LFM) |
|---|---|---|---|---|---|
| FG680 | 10.6 | 0.9 | 7.5 | 6.1 | 5.6 |

- Customer requirements
  - Ta = 50°C
  - Power = 8.0 Watts (user's estimate)
  - User does not want to exceed $\mathbf{T_J}$(max) of 100°C
- Determination with base Still Air data:
  - $\mathbf{T_J} = \mathbf{T_A} + (\theta_{JA}) * P$
  - $\mathbf{T_J} = 50 + 8 * 10.6 = 134.8°C$
  - Unacceptable! $\theta_{JA}$ in still air will not work since the 134.8°C is beyond the stated goal of 100°C or less.
- Calculating acceptable thermal resistance:
  - Determine what $\theta_{JA}$ will be required to stay below 100°C with the 8 Watts power?
  - Thermal budget = $(\mathbf{T_J} - \mathbf{T_A}) = 50°C$.
  - $\theta_{JA} = (50)/8 = 6.25°C/Watt$.
  - The package and any enhancement to it need to have an effective thermal resistance from the junction to ambient less than 6.25°C/Watt. That becomes the goal any thermal solution ought to meet.
- **Solution Options**:
  - The bare package with 500 LFM (2.54 meters/s) of air will give $\theta_{JA} = 6.1°C/Watt$. (from the data table above). That will be a workable option, if that much airflow will be tolerable.
  - Heatsink calculation. With a heatsink, heat will now pass through the package ($\theta_{JC}$) then through an interface material ($\theta_{CS}$), and from the heatsink to ambient ($\theta_{SA}$). This can be expressed as follows:
    - $\theta_{JA} \geq \theta_{JC} + \theta_{CS} + \theta_{SA}$
    - $6.25 \geq 0.9+0.1+ \theta_{SA}$

    where
    - 6.25°C/Watt is the condition to be met
    - 0.9°C/Watt — $\theta_{JC}$ from data
    - 0.1°C/Watt — $\theta_{CS}$ from interface material data
  - From above $\theta_{SA} \leq 5.25°C/Watt$
  - Objective will be to look for a heatsink with $\theta_{SA}$ **< 5.25°C/Watt** that meets the physical constraints in the system
  - Passive heatsink with some air flow — 250 LFM (1.25m/s) can be selected
  - Active heatsinks — it may be possible to use small low-profile heatsinks with DC fans

# Thermal Data Comparison

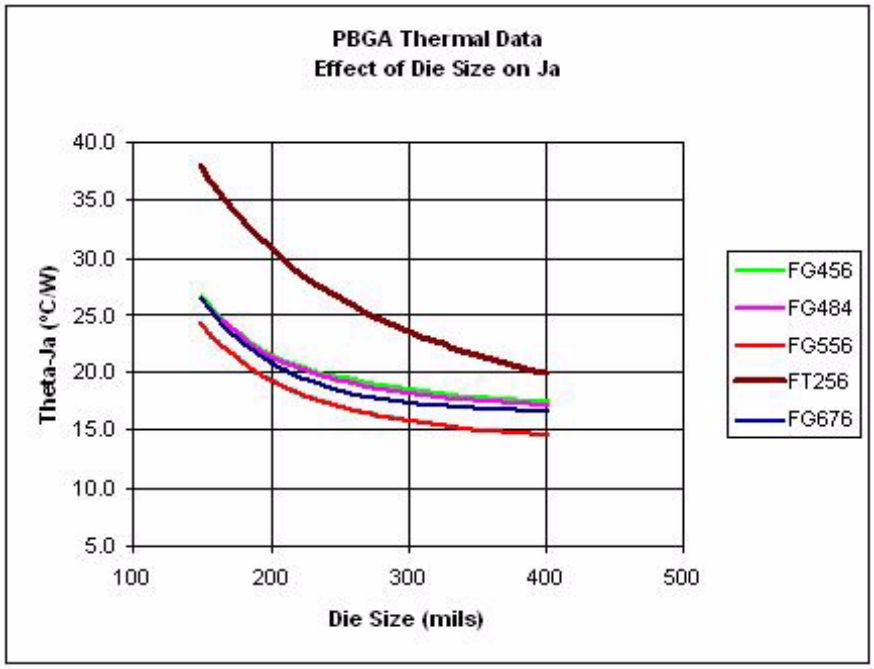



*Figure 3-6:* **PBGA Packages - Impact of Die Size on $\theta_{JA}$**

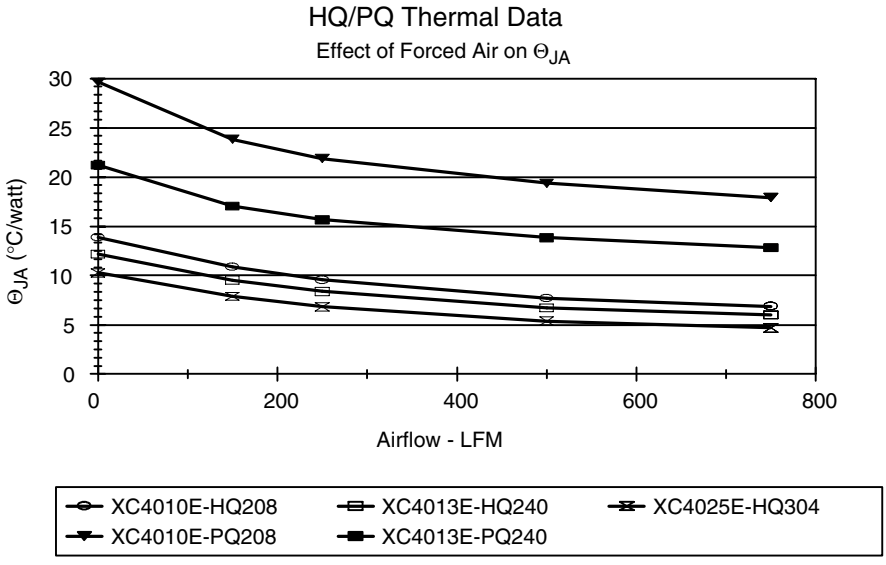



*Figure 3-7:* **HQ/PQ Thermal Data**

| | | Board Size | | |
|---|---|---|---|---|
| Xilinx 35x35mm FF1148-4VLX100 | | 4" x 4" Board | 10" x 10" Board | 20" x 20" Board |
| Layer Count of Mounted Board | 4 | 10.1* (100%) | 9.2 (91%) | - |
| | 8 | 8.9 (88%) | 6.1 (60%) | 5.5 (54%) |
| | 12 | 8.3 (82%) | 5.2 (51%) | 4.9 (48%) |
| | 16 | 8.0 (79%) | 5.0 (50%) | 4.6 (46%) |
| | 24 | - | 4.7 (47%) | 4.5 (44%) |

* = JEDEC Mount conditions

*Figure 3-8:* **Impact of Mounted Board Characteristics on $\theta_{JA}$ of Flip-Chip FF1148**

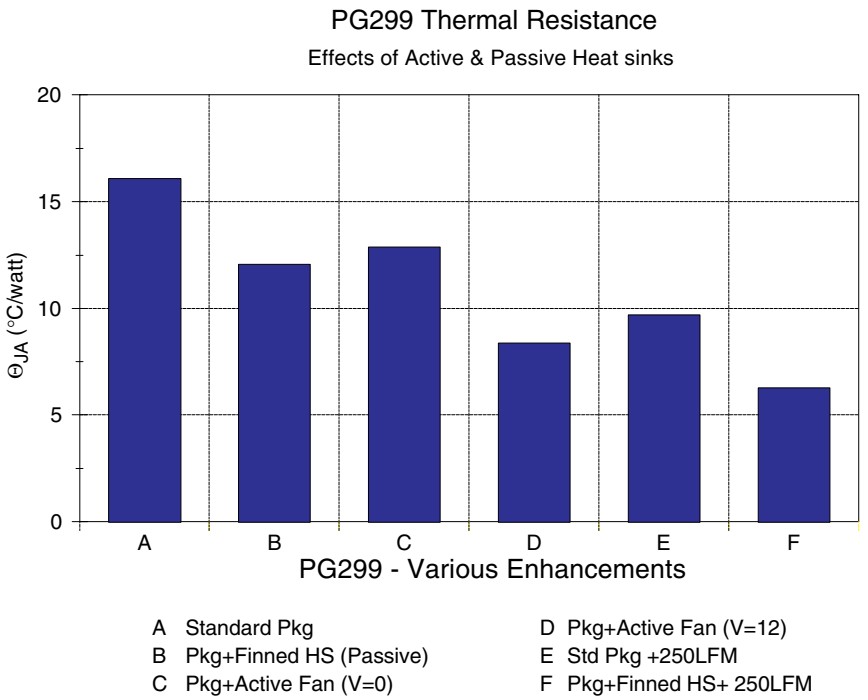



*Figure 3-9:* **PG299 Thermal Resistance**

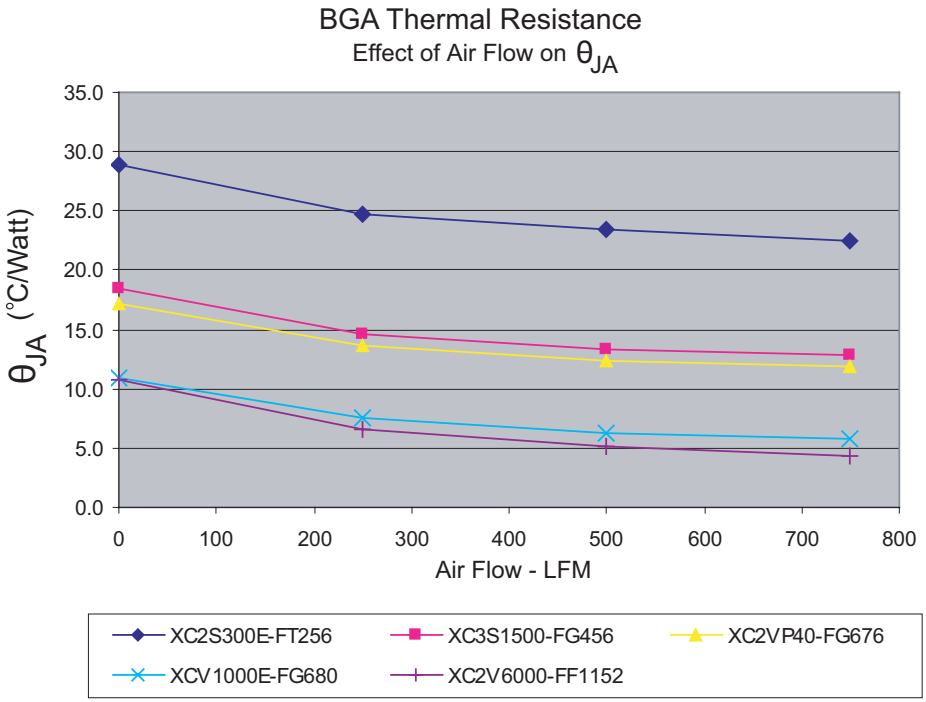



*Figure 3-10:* **BGA Thermal Resistance**

## Some Power Management Options

The variety of applications that the FPGA devices are used in makes it a challenge to anticipate the power requirements and thus the thermal management needs a particular user may have. While Xilinx programmable devices may not be the dominating power consumers in some systems, it is conceivable that high-gate-count FPGA devices will be exercised sufficiently to generate considerable heat.


*Figure 3-11:* **Enhanced BGA with Low Profile Retainer Type Passive Heatsinks**

In general, high-I/O and high-gate-count Virtex™ family devices have the potential of being clocked to produce high wattage. Being aware of this potential in power needs, the package offering for these devices includes medium- and high-power-capable package options. This allows a system designer to further enhance these high-end BGA packages to handle more power.

When the actual or estimated power dissipation appears to be more than the specification of the bare package, some thermal management options can be considered. The accompanying Thermal management chart illustrates the incremental nature of the recommendations — ranging from simple airflow to schemes that can include passive heatsinks and active heatsinks.

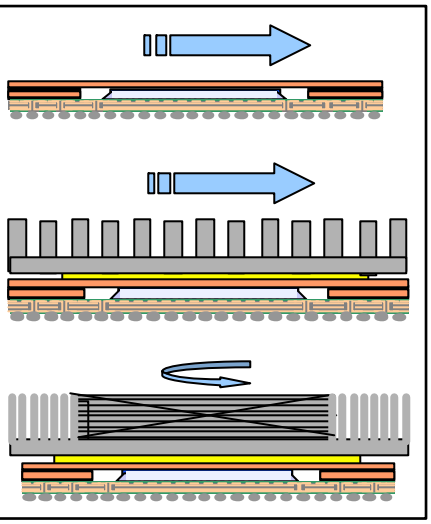
| | | | |
|---|---|---|---|
| Low End<br>1-6 Watts | Bare Package with Moderate Air<br>8-12˚C/Watt | Bare Package. Package may be used with moderate airflow within a system. |  |
| Mid Range<br>4-10 Watts | Passive H/S + Air<br>5-10˚C/Watt | Package used with various forms of Passive Heatsinks and Heat spreader techniques. | |
| High End<br>8-20 Watts | Active Heatsink<br>2-3˚C/Watt or better | Package used with Active Heatsinks TEC and Board level Heat spreader techniques. | |

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*Figure 3-12:* **Thermal Management — Incremental Options**

The use of heatpipes, and even liquid-cooled heat plates, may be considered in the extreme for some of these packages. Details on the engineering designs and analysis of some of these suggested considerations may require the help of thermal management consultants. The references listed at the end of this section can provide heatsink solutions for industry-standard packages.

Some of the options available in thermal management may include the following:

- Most high-gate-count Xilinx devices come in more than two package types. Explore thermally enhanced package options available for devices. The quad packages and some BGA packages have heat enhancement options. Typically, 25% to 40% improvement in thermal performance can be expected from these heatsink-embedded packages.
- In a system design, natural convection can be enhanced with venting in the system enclosure. This will effectively lower the Ta and increase available thermal budget for moderate power dissipation.
- The use of forced-air fans is the next step beyond natural convection, and it can be an effective way to improve thermal performance. As seen on the graphs and the calculations above, forced air (200-300 LFM) can reduce junction-to-ambient thermal resistance by up to 30%.

- For moderate power dissipation (2 to 5 Watts), the use of passive heatsinks and heat spreaders attached with thermally conductive double-sided tapes or retainers can offer quick solutions.
- The use of lightweight finned external passive heatsinks can be effective for dissipating up to 8 Watts on some packages. If implemented with forced air as well, the benefit can be a 40% to 50% reduction as illustrated in the XCV1000E-FG680 example. The more efficient external heatsinks tend to be tall and heavy. When using a bulky heatsink, it is advisable to use spring-loaded pins or clips to reduce heatsink-induced stress on the solder joints of the component as these pins or clips help transfer the mounting stress to the circuit board. The diagonals of some of these heatsinks may be designed with extensions to allow direct connection to the board (see Figure 3-13).


*Figure 3-13:* **Heatsink with Clips**

- Exposed metal heatsink packages: All thermally enhanced BGAs with dies facing down (including these package codes - BG352, BG432, BG560, FG680, FG860, and Flip-Chip BGAs) are offered with exposed metal heatsink at the top. These are considered high-end thermal packages and they lend themselves to the application of external heatsinks (passive or active) for further heat removal efficiency. Again, precautions should be taken to prevent component damage when a bulky heatsink is attached.
- Active heatsinks may include a simple heatsink incorporating a mini fan or even Peltier Thermoelectric Coolers (TECs) with a fan to carry away any heat generated. Any consideration of applying TEC in heat management should include consultation with experts in using the devices, as these devices can be reversed and this may damage components. Also, condensation can be an issue.
- Molded packages (FG456, FG676, FG1156, PQs, etc.) without exposed metal at the top also can use these heatsinks at the top for further heat reduction. These BGA packages are similar in construction to those used in graphic cards in PC applications, and heatsinks used for those applications can easily be used for these packages as well. In this case, the $\theta_{JC}$ resistance will be the limiting consideration.

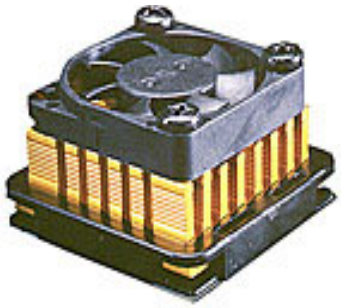


*Figure 3-14:* **Example of Active Heatsink for BGA (Malico)**

- Outside the package itself, the board on which the package sits can have a significant impact on thermal performance. Board designs can be implemented to take advantage of a board's ability to spread heat. Heat flows to the outside of a package and is sunk into the board to be conducted away – through heatpipes or by normal convection. The effect of the board will be dependent on the size and how it conducts heat. Board size, the level of copper traces on it, and the number of buried copper planes all lower the $\theta_{JA}$ thermal resistance for a package mounted on it. Some of the heatsink packages – like HQ, with the exposed heatsink on the board side – can be glued to the board with thermal compound to enhance heat removal into the board. BGA packages with full matrix of balls can be cooled with this scheme. Users need to be aware that a direct heat path to the board from a component also exposes the component to the effect of other heat sources, particularly if the board is not cooled effectively. An otherwise cooler component can be heated by other heat-contributing components on the board.
- A Xilinx lower voltage version of the equivalent circuit in the same or similar package. With the product and speed grade of choice, a power reduction of up to a 40% can be anticipated for a 5.0V to a 3.3V version. Not all products have equivalent lower voltage versions.

See "Web Sites for Heatsink Sources" in Appendix for lists of Web sites that offer more information on heat management and sources for interface material.

## System Simulation Support

For more accurate in-system $\mathbf{T_J}$ prediction, Xilinx can provide Compact Thermal Models (CTMs) to be used in system thermal simulations. The figure of merit thermal data Xilinx provides can be used to select packages and perform comparative thermal analysis and some preliminary $\mathbf{T_J}$ predictions. However, when the thermal margins are very tight, or the component is integrated with other heat sources in a system, a full system thermal analysis might be required. These CTMs are provided to reduce the computational complexity.

Our CTMs are based on the Delphi approach that JEDEC has proposed. Since the JEDEC neutral (XML) format proposal has not been adopted yet, the Delphi approach is used to generate these files and the data saved in the native and proprietary file formats of the targeted CFD tools, rather than follow a neutral file. We are closely following JC15-1 developments and hope to offer the neutral file format when it is ready and adopted by the CFD tool vendors.

In the meantime, these CTMs are based on the Delphi (dotcomp optimization) approach for specific tools. These tools occupied the first two places in our pre-introduction customer survey. The libraries are available in Flotherm (pdml) format; V5.1 and above and Icepack (ver. 4.2 and above) format.

Virtex-4, and newer products are supported. CTM Data can be downloaded from the Xilinx Support Download Center:
http://www.xilinx.com/xlnx/xil_sw_updates_home.jsp.

Models for older products can be requested from: ctm_team@xilinx.com.

The plan is to support models for other CFD tools through the neutral format approach. Before the neutral file format is adopted, there might be limited support of Xilinx formatted ASCII-based file defining nodes and listing the associated resistances between notes for manual entry into various other tools that support CTM usage; requests of this type should be directed to: ctm_team@xilinx.com.

Chapter 4

# Package Electrical Characteristics

## Introduction

As data rates increase and signal rise times become shorter, the effects of package parasitics are becoming increasingly significant as the hardware engineers model their circuits. Discontinuities that may have had minimal impact on circuit performance in past generations of components are now of paramount importance as designers strive to achieve higher performance in their systems.

The IC package forms an interconnect system just like traces on a printed circuit board (PCB) or conductors in connectors. When a designer simulates the signaling performance from a driver to a receiver, all the interconnect parasitics in the path, including the package, must be considered in order to achieve simulation results that represent the entire system's performance.

Current Xilinx packages are constructed with either wirebond or flip-chip interconnect technology. Some components use simpler leadframe-based packages, while others use laminate-based packages with multilayer construction. The choice of package matches the performance and marketing objectives sought for the device family. In multilayer packages, innovative pin-out selections and creative design techniques are used in a co-design effort to optimize package performance and to prevent the package from being a limiting factor for the device. For these high performance FPGA packages, Xilinx also provides package models that allow the user to take package parasites into account to accurately model the component's performance prior to committing to hardware.

This chapter focuses on defining certain critical concepts associated with electrical characterization of packages. It is also intended to provide relevant theoretical review of electrical issues and concepts as they relate to the characterization effort. The document provides descriptions of the methods utilized to generate the parasitic data and derive appropriate models for their use. Some data examples, ranging from simple tabulated RLC to s-parameter models, are given to illustrate the range of electrical data that are available for the packages.

## Terminology - Definitions and Reviews

There are a number of key concepts that should be understood in order to appreciate how packages affect the signals transiting through them, as well as how package parasitics are modeled or measured in the lab.

Any conductor system is characterized by some basic electrical parameters which are dependent of the physical design of the system, a package is no exception. The basic electrical parameters associated with packages are resistance, inductance, conductance, and capacitance. These are commonly referred to as RLGC parameters. The parameters will be defined in the following subsections. The section also explains several other metrics which are derived from RLGC parameter values. Finally, more advanced concepts such as s-parameters, crosstalk, and SSN will be covered.

## Resistance (R)

Resistance is one of the basic electrical parameters that commonly defines the series loss in a conductor. Electrically, Ohm's law defines resistance as the ratio of voltage to current in a conductor:

$$R = \frac{E}{I}$$ where $E$, is voltage and $I$ is current.

Physically, resistance is defined as:

$$R = \frac{\rho \cdot L}{A}$$ where $\rho$ is the resistivity of the conductor material,
$L$ is the length of the conductor, and
$A$ is the cross sectional area.

The physical equation above is valid at DC where the current flows through the whole cross sectional area of the conductor. At higher frequencies, where skin effect becomes important, the cross sectional area is decreased and consequently the resistance increases at higher frequencies. The amount that the cross sectional area is decreased is highly geometry-dependent and is also a function of the proximity of the conductor to other nearby current carrying conductors. Typically, the reported R component of the package resistances are given at DC for nets intended to operate below about 1 GHz. Higher frequency nets, such as those associated with transceivers (MGTs and GTPs), are characterized with frequency-dependent losses. These frequency-dependent losses are best determined with 2D or 3D extractor software.

The skin depth (which is the depth of electric and magnetic field penetration) of a conductor is given by:

$$\delta = 50\mu\sqrt{\frac{\rho}{f}}$$ where $\delta$ is the skin depth in microns.
$\rho$ is the conductor resistivity in $\mu\Omega$–$cm$ and
$f$ is the frequency in MHz.

As a point of reference, $\delta$ is about 20 microns at 10 MHz frequency if the conductor is copper. Note that $\delta$ decreases with the $\frac{1}{\sqrt{f}}$, so at a frequency of $4f$, the skin depth would be one half the value that it was at a frequency of $f$.

## Inductance (L)

Inductance is one of the fundamental properties of any electrical conductor. Any current carrying conductor is surrounded by lines of magnetic flux. These lines are circular loops which encircle the current carrying conductor. The number of loops in any instance is concentrated near the conductor with the density of the lines decreasing as the distance from the conductor increases. A basic relationship for inductance is:

$$L = \frac{N}{I}$$

where $L$ is the inductance (in Henrys)

$N$ is the number of magnetic lines encircling the conductor (in Webers)

$I$ is the current through the conductor in Amps.

Inductance is geometry-dependent. Whether a conductor has 1 Amp or 100 Amps flowing through it, the inductance is the same since the ratio remains constant. The presence of dielectric material near the conductor will not alter the inductance. The presence of ferro-magnetic material with permeability greater than 1 will affect the inductance.

When we discuss inductance, the terms *loop inductance, partial inductance, self inductance,* and *mutual inductance* are some of the items that come up. These are explained below:

- Loop inductance is the inductance of a complete current carrying loop. It is a unique value dependent on the loop geometry. The larger the area encompassed by the loop, the larger the loop inductance will be.
- A partial inductance is the inductance contributed by a portion of the loop. It is not a unique value.
- Self Inductance - When one refers to the inductance of a conductor the reference is usually meant to imply the self inductance. This is the ratio of lines of magnetic flux to current where the lines encircle their own conductor.
- The concept of mutual inductance comes into play when one considers lines of magnetic flux generated by a current carrying conductor that also encircle (or couple to) another conductor. These lines of flux will cause a voltage to be generated into the coupled conductor.

### Some Inductance Expressions

Closed form analytical equations to calculate inductance do exist for simple geometries. In a complex system like a package, such simplified closed form expressions are hard to come by; approximations abound with varying degrees of accuracy. To accurately determine the partial inductance of conductor geometry in a package, the use of a good 2D or 3D electromagnetic extractor program is recommended. Below are some closed-form formulas that are reasonably accurate for geometries commonly found in packages.

- Partial self inductance of a round wire (with ground at infinity):

$$Lwire = 5 \cdot d \cdot \left[ ln\left(\frac{2 \cdot d}{r}\right) - 3/4 \right]$$

where, $Lwire$ = inductance in nH

$d$ = wire length

$r$ = wire radius

(all dimensions in inches)

- Partial self inductance of a round wire over a metal plane:

$$Lwire = 5 \cdot d \cdot \left[ ln\left(\frac{2 \cdot h}{r}\right)\right]$$

where, *Lwire* = inductance in nH

*d* = wire length

*h* = height of wire above the plane

*r* = wire radius

(all dimensions in inches)

- Partial self inductance of a rectangular conductor (with ground at infinity):

$$L = 5 \cdot d \cdot \left[ ln\left(\frac{2 \cdot d}{(w + t)}\right) + \frac{1}{2}\right]$$

where, *L* = inductance in nH

*d* = conductor length

*h* = height of conductor above plane

*w* = width of conductor

*t* = thickness of conductor

(all dimensions in inches)

- Partial self inductance of a rectangular conductor - like a trace or perhaps a leadframe lead over a metal plane:

$$L = 5 \cdot d\left[ ln\left(\frac{8 \cdot h}{(w + t)}\right) + \frac{w + t}{4 \cdot h}\right]$$

where, *L* = inductance in nH

*d* = conductor length

*h* = height of conductor above plane

*w* = width of conductor

*t* = thickness of conductor

(all dimensions in inches)

These relationships have been compiled from publications by several authors[1,2,3] including Eric Bogatin, and Brian Young and Grover.

## Capacitance (C)

The capacitance of a conductor is dependent on the area of the conductor, the distance the conductor is placed from some reference conductor and the dielectric constant of the dielectric material. An expression for simple parallel plate capacitance is commonly expressed as:

$$C = \frac{\varepsilon_o \cdot A}{t}$$

where, $A$ = is the conductor area

$t$ = is the dielectric thickness and

$\varepsilon_o$ = is the permittivity of free space

If the dielectric material between the conductors is some material other than air or vacuum the equation is modified to include the relative dielectric constant $\varepsilon_r$ as follows:

$$C = \frac{\varepsilon_o \cdot \varepsilon_r \cdot A}{t}$$

$\varepsilon_o$ is equal to 0.0885 pF/cm or equivalently 0.225 pF/inch. It may be seen that the capacitance of a conductor will increase if the size of the conductor increases, the thickness of the dielectric decreases or the dielectric constant of the dielectric material is increased. While this expression is not directly applicable to the geometries of package transmission lines and planes, it does illustrate the basic relationships between capacitance and the dielectric constant, conductor area and dielectric thickness.

Other ways of expressing capacitance:

- Capacitance is also defined as the ratio of charge to voltage that can be stored between a pair of conductors

$$C = \frac{Q}{V}$$

where, $C$ is the capacitance in Farads

$Q$ is the charge in coulombs and

$V$ is the voltage in volts.

- Transmission lines commonly have their capacitance specified as a per-unit-length (PUL) value such that $C_{total} = C_{PUL}$ x Length.
- Self capacitance is the capacitance of a conductor to ground ($C_1$ would be the capacitance of conductor 1 to ground). Mutual capacitance is the capacitance between two conductors ($C_{12}$ would be the capacitance between conductor 1 and conductor 2).

Examples of closed form expressions for capacitance:

For complex structure a field solver is the preferred method of determining the capacitance of a conductor, however for a couple simple structures the following equations can provide answers accurate to within about 5%.

- Wire over a ground:

$$C = \frac{1 \cdot 4 \cdot \varepsilon_{eff}}{\ln\left(\frac{2h}{r}\right)}[(pF)/(inch)]$$

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \left(\frac{\varepsilon_r - 1}{2}\right)\frac{1}{\sqrt{\left(1 + \frac{10h}{r}\right)}}$$

where, $\varepsilon r$ is the relative dielectric constant of the dielectric

$h$ is the distance from the ground plane to the center of the wire

$r$ is the radius of the wire

$h$ and $r$ are in inches

- Capacitance between two parallel wires:

$$C = \frac{1 \cdot 4 \cdot \varepsilon_r}{\ln\left(\frac{s^2}{(ab)}\right)}[(pF)/(inch)]$$

where, $s$ is the distance between wire centers

$a$ and $b$ are the diameters of wires

## Conductance (G)

The conductance parameter (G) is related to the losses in the insulating substrate material. This is a frequency dependent parameter that scales directly with frequency. Most all substrate materials utilized in package construction have very low losses at low frequencies (less than 1 GHz). As a result, the conductance (a parallel loss) is very low and is usually ignored when modeling SelectIO™ lines. The dielectric loss does become significant at the higher frequencies where high speed nets are utilized. These lines are typically characterized by s-parameters as opposed to RLGC parameters.

## Impedance (Z)

The impedance of a transmission line may be calculated readily if you known the line's inductance and capacitance. The relevant equation is:

$$Z = \sqrt{\frac{L}{C}}$$

where, $Z$ is in Ohms,

$L$ is the line's per-unit-length inductance in Henrys and

$C$ is the per-unit-length capacitance in Farads.

When circuit elements interface with each other (for example, package trace and PCB trace, or PCB trace and termination), any mismatch in their impedances at their boundaries will result in reflections. The higher the mismatched magnitude, the greater the associated

reflection, hence distortion in the signal traversing the mismatched interface. For this reason, it makes sense to minimize the impedance mismatches in a system.

## Time Delay ($T_d$)

The time delay for transmission line (i.e., conductor) in a package is calculated by the equation $[T_d = \sqrt{L \cdot C}]$ where the delay is in seconds, the capacitance is in Farads and the inductance is in Henrys. Knowledge of a line's delay contribution is needed in determining timing closure. Time delay can also be determined if one knows the relative dielectric constant $\varepsilon_r$ of the substrate material associated with a transmission line. A transmission line with air as a dielectric propagates signals at the speed of light ($c = 3x10^{10}$ cm/sec.) or about 5.9 inches/psec. In a material with a relative dielectric of $\varepsilon_r$ the velocity of propagation is given by the expression:

$$v = \frac{c}{\sqrt{\varepsilon_r}};$$

where, $v$ is velocity in the material,

$c$ is speed of light, and

$r$ is the relative dielectric constant.

For example, typical FR4 material has a dielectric constant of about 4, so the velocity of propagation in a transmission line utilizing FR4 as the dielectric material will be c/2 (one half the speed of light) or 2.95 inches/psec. The time delay of a transmission line is simply the reciprocal of the velocity. In the case of FR4, the $T_d$ is about 169.5 inches/psec. Additionally, the time of flight ($T_{of}$) in a transmission line is simply the line's length times $T_d$. This $T_{of}$ number is what would be used in timing closure calculations.

For large size laminate and ceramic-based packages where $T_d$ is likely to be over 50 ps, the delay data is provided. This $T_d$ is derived from the LC data if the per-pin data is available. In some cases, $T_d$ is derived directly from the trace length data of the relevant package design.

## Crosstalk

Coupling (usually unwanted) from one conductor to another is termed “Crosstalk”. The line generating the signal is called the “aggressor” and the line into which the signal is coupled is termed the “victim.” Generally, this coupled signal is considered noise and is undesired. There are two mechanisms involved in this unwanted coupling between circuits; capacitive and inductive. Capacitive coupling occurs when the victim net is affected by the electric-field lines generated by the aggressor. Inductive coupling is caused by the magnetic-field lines generated by the aggressor inducing a voltage in the victim circuit. Physically, the two items that affect coupling are the distance between the two circuits and the length of the coupling regions. The most effective way to minimize crosstalk is to increase the spacing between the aggressor and victim nets.

Crosstalk is broadly divided into “near-end” and “far-end” crosstalk. Near-end crosstalk is always positive since the currents generated by the inductive and capacitive coupling components add and sum at the near end. Far-end crosstalk can be either negative or positive. If the magnitude of the inductively coupled component is larger than the capacitive coupled component then the difference of the currents at the far end is positive, however, if the capacitive component predominates then the far end effect will be a negative voltage. Also note, that the magnitude of the near-end crosstalk is insensitive to

the coupled length of the aggressor and victim nets. However, the far-end crosstalk will increase with increasing coupled length until a saturation point is reached.

The exact mathematical relationships for calculating crosstalk can be complex and vary in detail depending on whether the nets are terminated or open circuited and whether near-end or far-end crosstalk are considered.

The following expressions, taken from *High Speed Digital System Design*[4], illustrate a couple of cases where both the aggressor and victim nets are terminated at both the near and far-end (quite often the case): The above reference reviews other terminated cases as well.

- Far-end Crosstalk

$$\frac{\left(\frac{L_{ij}}{L_i}\right) - \left(\frac{C_{ij}}{C_i + C_{ij}}\right)}{4}$$

- Near-end Crosstalk

$$\frac{\left(\frac{L_{ij}}{L_i}\right) + \left(\frac{C_{ij}}{C_i + C_{ij}}\right)}{2}$$

$C_i$ and $L_i$ are the self capacitance and inductances of the victim lines respectively.

$C_{ij}$ and $L_{ij}$ are the mutual capacitances and inductances respectively between nets *i* and *j*.

## Ground Bounce

Ground bounce is the voltage difference between any two grounds (typically between an IC and circuit board ground) induced by simultaneously switching current through bond wire, lead, or other interconnect inductance. When IC outputs change state, large current spikes result from charging or discharging the load capacitance. The larger the load capacitance and faster the rise/fall times, the larger the current spikes are: $I = C * dv/dt$. Current spikes through the IC pin and bondwire induce a voltage drop across the leads and bondwires: $V = L * di/dt$. The result is a momentary voltage difference between the internal IC ground and system ground, which show up as voltage spikes and unswitched outputs.

Factors that affect ground bounce include:

- rise and fall times
- load capacitance
- package inductance
- number of output drivers sharing the same ground path
- device type

### Signal Integrity and Package Performance

Resistance, Capacitance and Inductance (defined in the "Terminology - Definitions and Reviews" section) are the three major electrical parameters used in one format or another to describe package electrical performance. These metrics are used to describe I/O, as well as power networks of the packages. The parameters, also known as interconnect parasitics, can be the source of many serious issues in digital systems. For example, a large resistance can cause RC and RL off-chip delays, power dissipation, and edge-rate degradation. Large capacitance in I/O nets can cause RC delays, crosstalk, edge-rate degradation, and signal distortion. Lead inductance, perhaps the most damaging parasitic in digital circuitry, can cause such problems as ground bounce (also known as simultaneous switching noise or delta-I noise), RL delays, crosstalk, edge-rate degradation, and signal distortion.

In the design of Xilinx packages, the challenge is to seek the appropriate balance for these parameters so that signal integrity issues are minimized. Package characterization is geared to assist the package designers in a co-design effort to make the appropriate choices backed by simulation and measurements in optimizing the package design and layout for performance. A further goal of the effort is to gather the parasitics data and seek the appropriate data representation of these parameters to help end-users deploy these packages. To this end, Xilinx offers raw tabulated package parasitic data, summaries of data, and various models as part of the deliverable. Representative samples will be shown at appropriate sections.

The measurement and 3D extraction capability, as well as the models support, will be described in the subsequent sections.

## Electrical Data Generation and Measurement Methods

With regards to experimental measurements, Xilinx uses both the Time-Domain Reflectometry (TDR) method for parasitic inductance and capacitance measurements, as well as frequency domain measurements performed with a 4-port Vector Network Analyzer (VNA). The practical measurement capability is augmented by a range of analytical calculators, 2D and 3D full wave FEM tools that are utilized through simulations to extract various signal integrity-based parameters about the packages.

### Review of Practical Measurements

The main components of a TDR setup includes a digitizing sampling oscilloscope, a fast rise-time step generator (<17 ps), a device-under-test (DUT) interface, and impedance-profile analysis software to extract parasitic models from the TDR reflection waveforms. In this method, a voltage step is propagated down the package under test, and the incident and reflected voltage waves are monitored by the oscilloscope at a particular point on the line. The resulting characteristic impedance of the package interconnect shows the nature (resistive, inductive, and capacitive) of each discontinuity.

The VNA measurement setup is composed of a 20 GHz 4-port VNA, a probing station, and microprobes. Using the VNA, s-parameter measurements of various package nets are made over wide bandwidths. The VNA injects a swept frequency signal into the DUT. The instrument then measures both reflected and transmitted voltages at various package nodes which are being probed.

## Package Sample and Fixture Preparation

Prior to performing package measurements utilizing either the TDR or VNA, the package and the DUT interface must be fixtured. Proper fixturing ensures accurate and repeatable measurements.

*Figure 4-1:* **Altair BGA Fixture used for TDR measurement**

Figure 4-1 depicts an Altair BGA test fixture that is used in some of the TDR measurements on BGA packages. For TDR measurements, the DUTs for all inductance (self and mutual) are specially assembled components with all leads shorted to the internal package ground. For packages without an internal ground (i.e., QFP, PLCC, etc.), the die-paddle is used instead (i.e., bonds are made to the paddle). Measurement includes the wire parasitics.

The DUT samples for capacitance (self and mutual) measurements are special assembled package units with all internal leads floating (un-bonded). In the actual testing, the lead/ball under test is isolated and all other package leads are connected to a common potential (ground) in the all conductor grounded (OCG) mode.

The DUT interface provides a physical connection between the oscilloscope and the DUT with minimum crosstalk and probe/DUT reflection. It also provides a small ground loop to minimize ground inductance of the fixture.

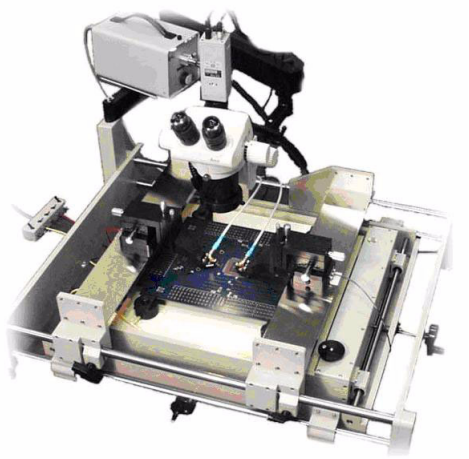


*Figure 4-2:* **GTL VNA Fixture**

For VNA measurements, either single-sided or two-sided measurements may be made. In most cases, the package to be measured is attached to a test fixture board that facilitates holding the sample package during the measurement procedure. Two-sided measurements allow characterization of the package from the bumps sites to the BGA balls. The package is held at right angles to the probing station table. Single-side measurements are sometimes made when it is difficult or impossible to achieve two-sided probing of the package. In this case, the package is held parallel to the probe station table.

In both TDR and VNA cases, measured waveforms are usually downloaded to an integrated PC running analysis software for package parasitic model extraction. The software for TDR uses a method called the Z-profile algorithm, or the impedance-profile algorithm, for parasitic analysis. This method translates the downloaded reflection waveforms into true impedance waveforms, from which package models for inductance and capacitance are extracted.

## Software-Based Simulations and Extractions

Xilinx data generation approach consists of a mix of electrical models based on 2-D and Full Wave 3-D package simulations/extraction that have been calibrated with time and frequency domain measurements. Once the simulation assumptions are optimized and calibrated with data, we deploy the extraction tools to generate per pin data and other full package models that may be impossible to deal with a TDR or VNA directly. The simulation tools are used to make determinations and provide design guidelines for pre-layout feasibility, pin assignment review, and layout design rule generation. In the post-layout/fabout stage, these software tools are deployed to, among other things, extract parasitics on the whole package. In addition to parasitic extraction, the tools also provide voltage drops and current densities of the power and ground nets. These same tools are used to generate data and models for internal as well as external use.

Some of the tools used in this effort are listed below.

### Modeling and Simulation Tools

- Ansoft Maxwell Q2D
- Ansoft HFSS (High Frequency Structure Simulator)
- Optimal Corp. PakSi-E High Speed 3D Field Solver
- Optimal Corp. O-wave/PowerGrid
- Cadence Advance Package Engineer (APE)/SpectraQuest
- Sigrity; Power SI
- TDA Systems I-Connect

## Package Electrical Data Delivery Formats

The tables below show some typical electrical data summaries. In general, generated electrical data is tabulated for the product and may be used in the appropriate IBIS models for the component. For specific products data, or for packages not listed, or additional information (such as mutual and power plane data), you may obtain them through a model at the download area or contact Xilinx Support with the specifics.

- **Summary data tables:** On most leadframe type packages (TQ, PQs, PC, etc.) and smaller laminate packages, Xilinx typically acquires electrical parasitic data on the longest and shortest lead/traces of the package based on design data. This provides the best and worst case for each package type (defined by package design, lead/ball count, pad size, etc.). Table 4-1 below shows some typical data for some laminate-based FPGA packages. Similar data is depicted in Table 4-2 for leadframe-based packages. For specific product-based data, you may review the [Package] section of the IBIS file or work through your field engineer.
- **The IBIS header file** - [Package]. Most electrical data generated for recent device families will be summarized in the [Package] section of the device IBIS file.The [Package] section data will be formatted in the Typical, Min and Max format of the file. In the completed IBIS file, all of the packages should be represented. You may need to uncomment the specific package of interest. The [Package] section of the Spartan™-3E file is shown in Figure 4-4 to illustrate this method of conveying package-specific electrical data for a device family. Note that in this example, the FG320 is uncommented for use. The device IBIS files can be downloaded from: http://www.xilinx.com/xlnx/xil_sw_updates_home.jsp?url=/support/download.htm
- **Per pin data tabulation:** Per pin electrical data is available for packages for most high end FPGA devices. Per pin data is not available for legacy products or leadframe devices. Xilinx keeps a database for this data type and will make them available to end-users in Excel format on request. The header for a typical Excel formatted per pin data tabulation can be found in Figure 4-5.
- **IBIS .pkg type file format:** See next section - models at Xilinx for description of IBIS format. This method conveys per pin RLC data in both coupled and uncoupled .pkg format. This is usually a long data file that may be parsed to get to the per pin data.

## Data Examples

Table 4-1 contains typical measured electrical data for some common laminate packages.

*Table 4-1:* **Electrical Data for Common Laminate Packages**

| Package Type | Xilinx PkgCode | Lself-Max (nH) | Lself-Min (nH) | C-Max (pF) | C-Min (pF) | R-Max (mW) | R-Min (mW) |
|---|---|---|---|---|---|---|---|
| 1.27 Pitch BGA | BG225 | 11.5 | 0.9 | 2.20 | 0.67 | 210 | 15 |
| | BG256 | 6.9 | 0.6 | 1.30 | 0.68 | 185 | 12 |
| | BG352 | 7.2 | 0.7 | 1.50 | 0.80 | 282 | 26 |
| | BG432 | 9.6 | 1.4 | 1.30 | 0.80 | 325 | 57 |
| | BG560 | 10.7 | 2.2 | 2.70 | 0.30 | 551 | 190 |
| | BG728 | 10.3 | 0.3 | 3.20 | 0.20 | 341 | 14 |
| | | | | | | | |
| Small Form Factor | CP132 | 3.8 | 1.2 | 0.30 | 0.10 | 158 | 135 |
| | CP56 | 2.2 | 0.3 | 0.40 | 0.14 | 313 | 48 |
| | CS144 | 3.0 | 1.5 | 0.30 | 0.20 | 143 | 76 |
| | CS280 | 8.9 | 2.7 | 0.80 | 0.20 | 371 | 148 |
| | CS48 | 2.4 | 1.8 | 0.30 | 0.20 | 126 | 26 |
| | | | | | | | |
| Fine Pitch 1.0 mm BGA | FT256 | 9.9 | 1.8 | 1.30 | 0.40 | 333 | 92 |
| | FG256 | 6.4 | 1.6 | 1.20 | 0.50 | 230 | 73 |
| | FG320 | 7.6 | 4.0 | 1.70 | 0.60 | 311 | 180 |
| | FG324 | 9.3 | 3.6 | 1.90 | 0.80 | 353 | 187 |
| | FG456 | 9.2 | 0.9 | 3.60 | 0.50 | 545 | 58 |
| | FG484 | 9.7 | 2.1 | 2.30 | 0.70 | 573 | 77 |
| | FG676 | 10.1 | 0.3 | 5.40 | 0.40 | 585 | 30 |
| | FG680 | 9.7 | 3.9 | 2.30 | 0.20 | 606 | 199 |
| | FG900 | 11.8 | 2.1 | 2.20 | 0.40 | 340 | 89 |
| | FG1156 | 12.3 | 1.8 | 2.20 | 0.50 | 330 | 82 |

**Notes:**

1. Wirebond parasitics were part of the consideration.
2. The data depicted in the table is a summary of measured data of typical laminate packages used for FPGAs. They are summarized without reference to the specific device families and for a larger range to cover all devices.
3. For more recent devices, specific device-based parasitic limits, as well as typical values, may be found in the [Package] section of the appropriate downloadable device IBIS file.
4. These ranges also apply to the lead-free equivalent packages. The lead-free version of packages has the letter “G” appended before the numeric portions of the package code (e.g., the lead-free version of FT256 will become FTG256). The same data applies to both packages.

Table 4-2 contains a summary of parasitics for some leadframe-based packages. The data includes the wirebond parasitics.

*Table 4-2:* **Parasitics for Leadframe-based Packages**

| Xilinx PkgCode* | Lself-Max (nH) | Lself-Min (nH) | C-Max (pF) | C-Min (pF) | R-Max (mW) | R-Min (mW) |
|---|---|---|---|---|---|---|
| PD8 | 6.4 | 3.0 | 1.0 | 0.6 | 52 | 32 |
| VO8 | 2.0 | 1.6 | 0.3 | 0.3 | 44 | 41 |
| SO20 | 3.0 | 1.7 | 0.4 | 0.2 | 60 | 40 |
| PC20 | 3.6 | 1.8 | 0.7 | 0.6 | 60 | 11 |
| PC44 | 4.3 | 2.1 | 1.0 | 0.7 | 69 | 14 |
| PC68 | 10.2 | 5.0 | 1.3 | 0.9 | 60 | 39 |
| PC84 | 13.0 | 6.8 | 1.8 | 1.6 | 58 | 43 |
| VQ44 | 2.4 | 1.2 | 0.4 | 0.2 | 60 | 16 |
| VQ64 | 1.7 | 1.3 | 0.4 | 0.4 | 30 | 23 |
| VQ100 | 6.7 | 1.5 | 0.8 | 0.3 | 124 | 18 |
| TQ44 | 1.6 | 1.1 | 0.4 | 0.3 | 20 | 15 |
| TQ100 | 5.9 | 1.1 | 0.7 | 0.3 | 108 | 17 |
| TQ144 | 9.7 | 6.4 | 1.4 | 0.7 | 144 | 105 |
| TQ176 | 10.1 | 3.5 | 1.3 | 0.7 | 58 | 44 |
| PQ100 | 8.2 | 2.3 | 1.3 | 0.4 | 99 | 29 |
| PQ160 | 15.2 | 5.2 | 1.9 | 1.0 | 127 | 62 |
| PQ208 | 15.9 | 5.3 | 2.0 | 0.5 | 138 | 81 |
| PQ240 | 15.2 | 6.9 | 2.0 | 1.3 | 126 | 71 |
| HQ208 | 12.7 | 5.3 | 2.0 | 1.0 | 139 | 73 |
| HQ240 | 12.1 | 4.9 | 2.5 | 1.2 | 119 | 57 |
| HQ304 | 12.2 | 7.3 | 2.7 | 1.9 | 144 | 94 |

**Notes:**

1. This is a compilation of measured data for leadframe packages without regard to any specific device family. Most product data will fall within these limits. These limits may be used for components listed in these products. Recent family of products will have specific limits in the [Package] section of the device IBIS file.
2. * - This same data applies to the lead-free versions of the packages. The lead-free version of these packages has the letter "G" appended before the numeric portions of the package code (e.g., the lead-free version of TQ144 will be TQG144). The same data applies to both packages.
3. This table will be updated periodically to reflect the addition of newer packages and updates to existing package data with newer limits, should those new devices expand the range.

Table 4-3 contains a summary of select I/O RLC parasitics for some flip-chip packages.

*Table 4-3:* **Select I/O RLC Parasitics for Flip-Chip Packages**

| Xilinx PkgCode | Lself-Max (nH) | Lself-Min (nH) | C-Max (pF) | C-Min (pF) | R-Max (mW) | R-Min (mW) |
|---|---|---|---|---|---|---|
| SF363 | 5.4 | 0.7 | 3.88 | 0.47 | 657 | 16 |
| FF668 | 6.2 | 0.8 | 3.34 | 0.84 | 1854 | 30 |
| FF672 | 7.9 | 0.5 | 3.11 | 0.40 | 1466 | 22 |
| FF676 | 6.0 | 1.2 | 3.93 | 1.00 | 1837 | 71 |
| FF896 | 8.2 | 0.8 | 7.50 | 0.90 | 680 | 21 |
| BF957 | 12.2 | 0.8 | 1.90 | 0.60 | 561 | 27 |
| FF1148 | 14.5 | 0.7 | 4.62 | 0.60 | 1962 | 38 |
| FF1152 | 11.8 | 0.5 | 5.30 | 0.77 | 2076 | 23 |
| FF1513 | 7.5 | 0.4 | 4.66 | 0.48 | 2450 | 32 |
| FF1517 | 9.0 | 0.8 | 9.70 | 0.75 | 1848 | 24 |
| FF1704 | 14.1 | 0.6 | 10.20 | 1.20 | 639 | 36 |
| FF1760 | 6.3 | 1.2 | 3.66 | 0.94 | 1884 | 75 |

**Notes:**

1. The I/O data reflects the full FC interconnect chain—bump, the vias, traces, and external balls as depicted in Figure 4-3.
2. The data presented in Table 4-3 is a compilation of all SelectIO-based data for all devices used in these flip-chip packages across a couple of generations of Virtex devices. The range encompasses all the known devices at the time of publication. This table will be updated periodically to include newer packages and updates to older packages with newer data, should those new devices expand the range.
3. Specific device family data may be obtained from the IBIS file (see example in Figure 4-4), or they can be requested through your field engineer.
4. These ranges also apply to the lead-free equivalent of the packages. The lead-free version of packages has the letter "G" appended before the numeric portions of the package code (e.g., the lead-free version of FF1148 will become FFG1148). The same data applies to both packages.

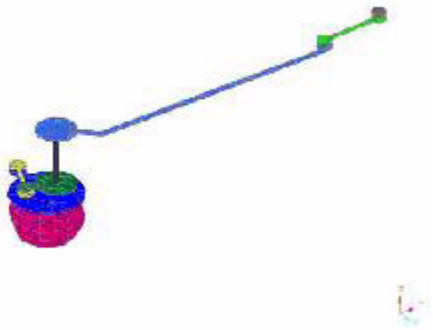


*Figure 4-3:* **Flip-Chip Interconnect Chain**

Figure 4-4 is a representation of electrical parasitics data embedded in a component family IBIS file.

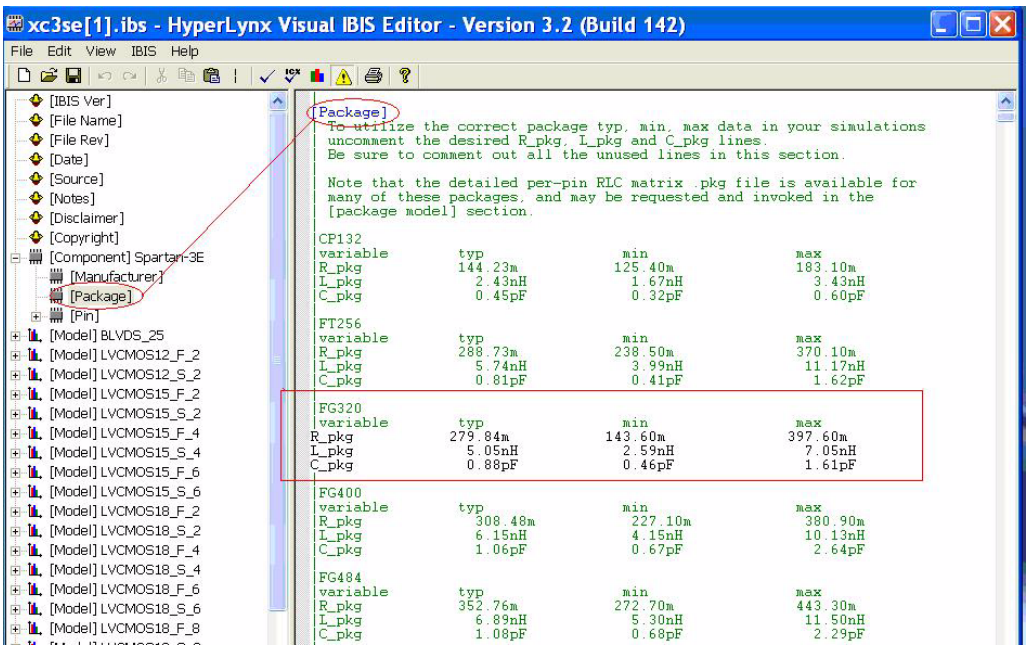



*Figure 4-4:* **Embedded Electrical Parasitics Data**

***Note:*** XC3SE IBIS file depicting the package electrical summary data in the [Package] section. In this case the FG320 package is uncommented as the default package. Data for other packages are clearly visible in this window.

Figure 4-5 illustrates Excel formatted tabulation of per pin data. The top 20 balls of the file for XC4VLX60 in FF1148 are shown.

Package: **FF1148**
Piecepart: **FGA0092**
Device: **XC4VLX60**
Freq: **500 MHz**
Rev: **1.0**

| | R (mΩ) | L (nH) | C (pF) |
|---|---|---|---|
| Max | 1931.00 | 6.13 | 4.11 |
| Mean | 1013.00 | 4.01 | 2.59 |
| Min | 68.87 | 1.37 | 1.17 |

| 0 | Ball | R (mOhm) | L (nH) | C (pF) | 0 | Ball | Function |
|---|---|---|---|---|---|---|---|
| 1 | A2 | VCCO_6 | VCCO_6 | VCCO_6 | 1 | A2 | VCCO_6 |
| 2 | A3 | 1765.00 | 5.93 | 3.55 | 2 | A3 | IO_L20N_VREF_6 |
| 3 | A4 | 1604.00 | 5.64 | 3.48 | 3 | A4 | IO_L20P_6 |
| 4 | A5 | 1483.00 | 5.44 | 3.48 | 4 | A5 | IO_L22P_6 |
| 5 | A6 | 1460.00 | 5.17 | 3.00 | 5 | A6 | IO_L12P_6 |
| 6 | A7 | GND | GND | GND | 6 | A7 | GND |
| 7 | A8 | 1446.00 | 5.06 | 2.93 | 7 | A8 | IO_L10P_6 |
| 8 | A9 | 1440.00 | 4.86 | 2.92 | 8 | A9 | IO_L15N_6 |
| 9 | A10 | 1288.00 | 4.59 | 2.70 | 9 | A10 | IO_L15P_6 |
| 10 | A11 | 1076.00 | 4.08 | 2.33 | 10 | A11 | IO_L3P_6 |
| 11 | A12 | VCCO_6 | VCCO_6 | VCCO_6 | 11 | A12 | VCCO_6 |
| 12 | A13 | 1397.00 | 4.68 | 2.75 | 12 | A13 | IO_L17N_6 |
| 13 | A14 | 1355.00 | 4.75 | 2.91 | 13 | A14 | IO_L17P_6 |
| 14 | A15 | 1753.00 | 5.68 | 3.60 | 14 | A15 | IO_L24P_LC_1 |
| 15 | A16 | NOPAD | NOPAD | NOPAD | 15 | A16 | NOPAD |
| 16 | A17 | NOPAD | NOPAD | NOPAD | 16 | A17 | NOPAD |
| 17 | A18 | NOPAD | NOPAD | NOPAD | 17 | A18 | NOPAD |
| 18 | A19 | GND | GND | GND | 18 | A19 | GND |
| 19 | A20 | 1634.00 | 5.33 | 3.39 | 19 | A20 | IO_L17N_CC_LC_1 |
| 20 | A21 | 1384.00 | 4.81 | 2.94 | 20 | A21 | IO_L21N_5 |

*Figure 4-5:* **Excel Formatted Tabulation of Per Pin Data**

## Models at Xilinx - Electrical Data Delivery via Models

Package models are a means to convey package electrical data, as stated in the previous section. These are provided to allow device users to accurately predict the performance of their designs. Xilinx recognizes that there may be several I/O model types available. For this reason, package electrical data is provided through the following I/O model formats as default:

- Base [Package] section data in IBIS device file. The base [Package] section data is provided for all newer devices in the base IBIS file. This data usually lists the packages used with Typical, Min, and Max parasitics, as illustrated in Figure 4-4.
- RLC matrix .pkg data format in either coupled RLC or uncoupled - depends on the device and size of package for SelectIO. These whole package RLC matrix data models are recommended for use below at about 1 Gbit/sec. data rates. The R, L and C element values are not frequency dependent. (The R value is typically characterized at DC). The IBIS .pkg format data is intended to be read by an IBIS simulator which will utilize the data to create an appropriate package model that will be connected to the IBIS buffer model being simulated. These models can be utilized in simulators such as HyperLynx, ICX, Hspice, and others. These models are extracted from the design database utilizing a 3D quasi-static FEM extracting tool. Figure 4-6 illustrates the topology of the extracted RLC parasitic data for both coupled and uncoupled conductors.

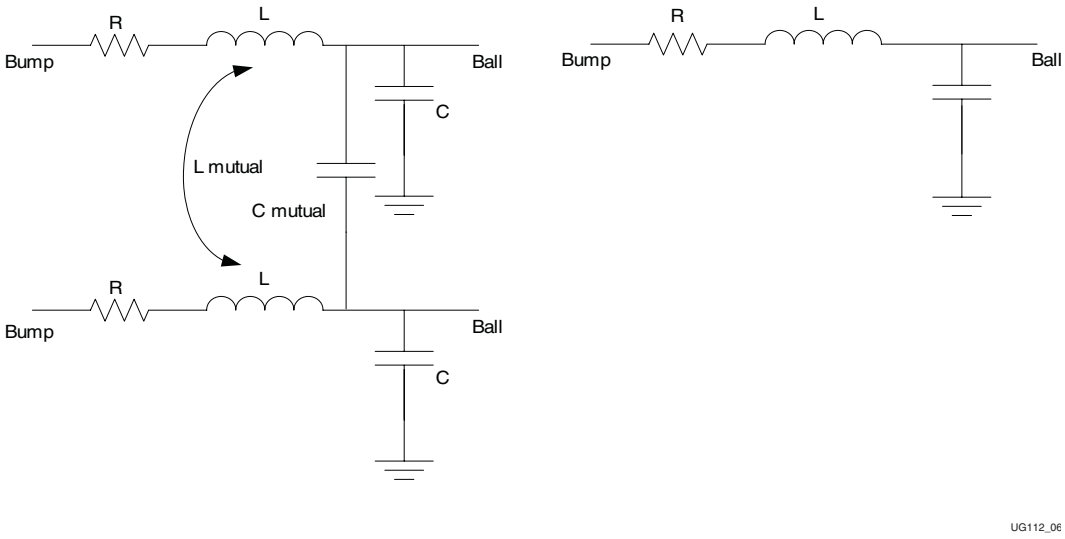
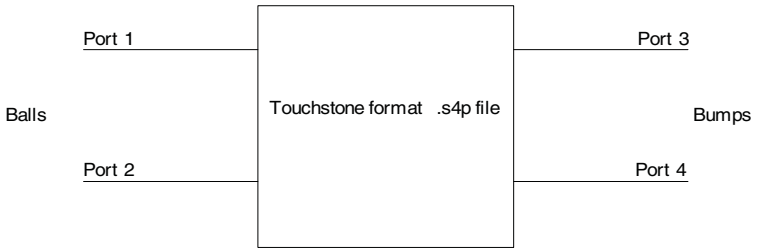



*Figure 4-6:* **Topology of Extracted RLC Parasitic**

- Touchstone s-parameter data files for high speed (e.g., MGT) nets. The s-parameter based models are provided to model the package nets associated with the MGT drivers and receivers at data rates above 1 Gbit/sec. The s-parameter data provided is extracted with 3D full-wave FEM extractor directly from the package design database. The tool setup and assumptions are optimized and calibrated with measured data. Typically, data is provided over the range of 1 GHz to 15 GHz, though wider bandwidth data may be available for some parts. S-parameters are measured and extracted with the assumption of a 50-ohm source and load impedance. At high frequencies, it is much easier to establish a good 50-ohm impedance than it is to establish a short or open, free from parasitic and fringing effects, as is often done in the characterization of low frequency components. S-parameter models are typically provided as Touchstone 4-port ".s4p" files to characterize differential MGT nets. The port assignment convention, as well as a sample 2-port formatted file, is illustrated in Figure 4-7.




```
ample 2-port Touchstone format file
Port1:bump:IPort2:ball :IO_L29N_SM4_7
100 MHz to 500 MHz

 Hz    S     RI       R     50
00000000     0.0061      0.0034     0.9920    -0.0497     0.9920    -0.0497     0.0058     0.003
50000000     0.0071      0.0043     0.9894    -0.0737     0.9894    -0.0737     0.0064     0.004
00000000     0.0082      0.0050     0.9862    -0.0975     0.9862    -0.0975     0.0070     0.005
50000000     0.0094      0.0055     0.9825    -0.1210     0.9825    -0.1210     0.0075     0.005
00000000     0.0105      0.0058     0.9783    -0.1443     0.9783    -0.1443     0.0079     0.006
50000000     0.0117      0.0059     0.9737    -0.1674     0.9737    -0.1674     0.0082     0.006
00000000     0.0129      0.0059     0.9685    -0.1903     0.9685    -0.1903     0.0083     0.007
50000000     0.0141      0.0058     0.9629    -0.2130     0.9629    -0.2130     0.0083     0.007
00000000     0.0153      0.0055     0.9568    -0.2355     0.9568    -0.2355     0.0082     0.007
```

*Figure 4-7:* **4-port Assignment Convention and Illustration of 2-port Touchstone Format**

- Other models—Upon request, it may be possible to provide other I/O models outside those outlined above. We are continuously reviewing formats and model delivery options, and will expand the above list as demand and practical needs of customers dictate. Following are some of the other models that may be supported on request.
  - SPICE sub-circuits - cover partial or all banks, distributed models, etc.
  - SSN models—models and simulations for simultaneous switching events depend on the I/O banks and number of nets considered. A full package model will be too complicated to generate and perhaps too unwieldy to use. The greater the number of ports, the more impractical it is to generate and verify such models. If there is a need for some reasonable n-port SSN model, please address this need through your FAE for review.
  - Power plane data and models—data for specific products will be supplied on request.
- For additional information about Xilinx electrical characterization methods and data, contact a local Xilinx field sales representative.

## Further Explanations on Model Data and Terminology

The coupled RLC matrix IBIS format data contains three matrix definitions within the .pkg file.

- The R matrix section defines the series resistive component of each modeled signal path.
- The L matrix section provides both the self and mutual inductance values for each modeled signal path and the four most closely coupled neighbor paths. On files without coupling, the representation is similar to the resistance section.

- The C matrix provides the self and mutual capacitive coupling values for each modeled signal path as well as the four most strongly coupled neighbor paths. Note that the mutual capacitance values are negative since they are elements of a Maxwellian matrix (see below for a review of matrix formulations) where the off diagonal terms are negative. The actual diagonal values and sign of the off-diagonal capacitances will be different from the corresponding nets in a spice deck. The following section explains the matrix formats.

## Capacitance Matrix formulations

When describing the RLC parasitics of a large package, it is convenient to utilize a matrix representation of the data. R and L data are quite straightforward to represent in a matrix. However, when it comes to capacitance, there is more than one option. Capacitance data is typically represented in the Maxwellian, Spice (or branch), and OCG (Other Conductors Grounded) matrix formats. Each of these formats has characteristics that make the format preferable for certain applications.

- **The Maxwellian format** is typically generated by field solvers. The main identifying feature of this format is that the off-diagonal terms are negative. This happens when the mutual capacitance terms are calculated in the solver by means of the relationship. When the matrix representation of the calculation is setup the off-diagonal C values are negative. These are the values presented in the Xilinx IBIS files.
- **The Spice matrix** formulation is particularly straightforward to utilize when describing a circuit topology in a nodal fashion as is done in spice. The mutual and self capacitance terms can be directly utilized as they appear in the matrix. Xilinx package Spice files already reflect the correct values.
- **The OCG format** arises from the way capacitance values are typically measured in the lab. All conductors in a package are grounded, except the ones that are being characterized. This causes the conductors under consideration to have somewhat greater capacitance to ground than they would otherwise.

In practical terms, users need not be concerned with using models, since the data elements are properly represented. However, awareness of the existence of these differences is important to avoid treating capacitance data for the same package in different models as potentially inconsistent. The guide below helps to understand the relationship among the formulations.

Figure 4-8 illustrates the relationship between Maxwellian and Spice formatted matrices for a 2x2 matrix. The corresponding OCG matrix (not shown) will be the same as the Maxwellian version with the data replaced with absolute value equivalents.

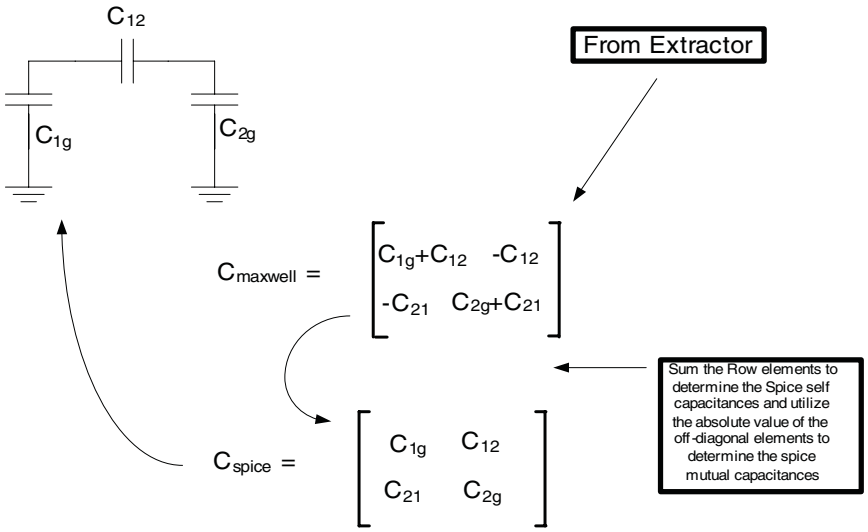



*Figure 4-8:* **Maxwellian and Spice Formatted Matrices (2x2 matrix)**

Figure 4-9 illustrates relationship numerically for a 2x2 matrix with mutual of 1, and $C_g = C_{2g} = 6$.

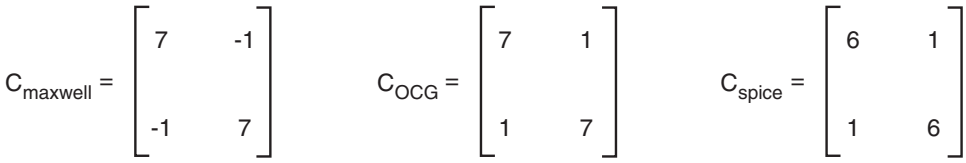



*Figure 4-9:* **2x2 Matrix**

# References


1. Eric Bogatin, *Signal Integrity - Simplified*, Prentice Hall 2004, ISBN 0-13-066946-6.
2. Brian Young, *Digital Signal Integrity*, Prentice Hall, ISBN 0140289043.
3. F. W. Grover, *Inductance Calculations: Working Formulas and Tables, Instrument Society of America*, 1945.
4. Stephen H. Hall, Garrett W. Hall & James A. McCall, *High-Speed Digital Systems Design: A handbook of interconnect theory and design practices*. John Wiley & Sons, 2000, ISBN 0-471-36090.

Chapter 5

# Recommended PCB Design Rules

## Recommended PCB Design Rules for QFP Packages

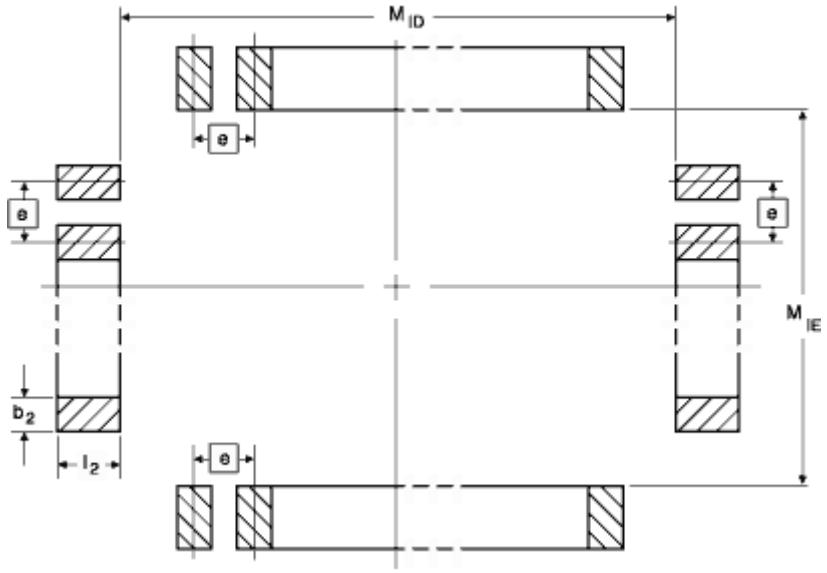



*Figure 5-1:* **EIA Standard Board Layout of Soldered Pads for QFP Packages**

*Table 5-1:* **PCB Land Pad Dimensions for Xilinx Quad Flat Packs(1)**

| Dim. | VQ44, VQG44 | VQ64, VQG64 | PQ100, PQG100 | HQ160, HQG160, PQ160, PQG160 | HQ208, HQG208, PQ208, PQG208 | VQ100, VQG100, TQ100, TQG100 | TQ144, TQG144 | TQ176, TQG176 | HQ240, HQG240, PQ240, PQG240 | HQ304, HQG304 |
|---|---|---|---|---|---|---|---|---|---|---|
| $M_{ID}$ | 9.80 | 9.80 | 20.40 | 28.40 | 28.20 | 13.80 | 19.80 | 23.80 | 32.20 | 40.20 |
| $M_{IE}$ | 9.80 | 9.80 | 14.40 | 28.40 | 28.20 | 13.80 | 19.80 | 23.80 | 32.20 | 40.20 |
| e | 0.80 | 0.50 | 0.65 | 0.65 | 0.50 | 0.50 | 0.50 | 0.50 | 0.50 | 0.50 |
| $b_2$ | 0.4-0.6 | 0.3-0.4 | 0.3-0.5 | 0.3-0.5 | 0.3-0.4 | 0.3-0.4 | 0.3-0.4 | 0.3-0.4 | 0.3-0.4 | 0.3-0.4 |
| $I_2$ | 1.60 | 1.60 | 1.80(2) | 1.80 | 1.60 | 1.60 | 1.60 | 1.60 | 1.60 | 1.60 |

**Notes:**

1. Dimensions in millimeters.
2. For 3.2 mm footprint per MS022, JEDEC Publication 95.

# Recommended PCB Design Rules for TSOP/TSSOP Packages

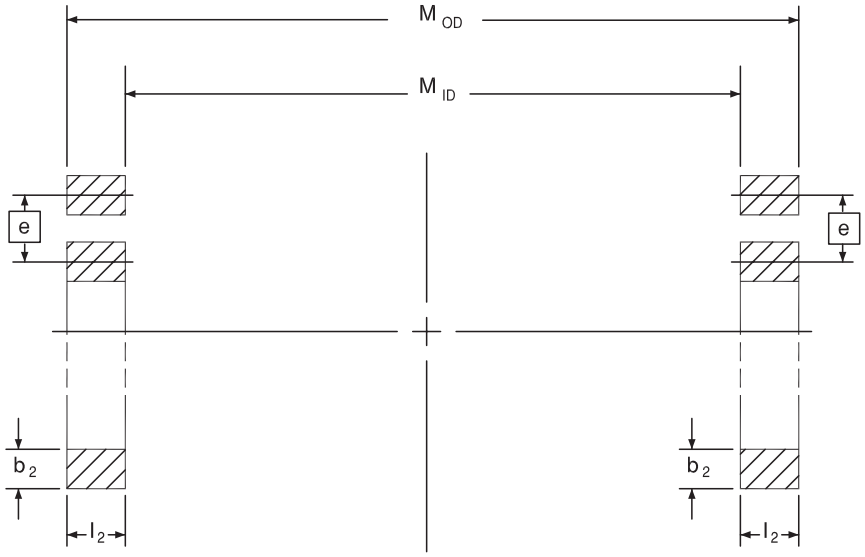



*Figure 5-2:* **IPC Standard Board Layout of Soldered Pads for TSOP/TSSOP Packages**

*Table 5-2:* **Dimensions for Xilinx TSOP/TSSOP Packages (mm)**

| Dimension | VO20, VOG20 | VO48, VOG48 |
|---|---|---|
| $M_{ID}$ | 4.20 - 4.40 | 17.80 - 18.00 |
| $M_{OD}$ | 7.20 - 7.40 | 20.80 - 21.00 |
| e | 0.65 | 0.50 |
| $b_2$ | 0.40 - 0.50 | 0.30 - 0.40 |
| $I_2$ | 1.50 | 1.50 |

# Recommended PCB Design Rules for BGA, CSP, and CCGA Packages

The diameter of a land pad on the component side is provided by Xilinx. This information is required prior to the start of your board layout so you can design the board pads to match the component-side land geometry. The typical values of these land pads are described in Figure 5-3 and summarized in Table 5-3. for Xilinx BGA packages, Non-Solder Mask Defined (NSMD) pads on the board are suggested. This allows a clearance between the land metal (diameter L) and the solder mask opening (diameter M) as shown in Figure 5-3. The space between the NSMD pad and the solder mask and the actual signal trace widths depends on the capability of the PCB vendor. The cost of the PCB is higher when the line width and spaces are smaller.

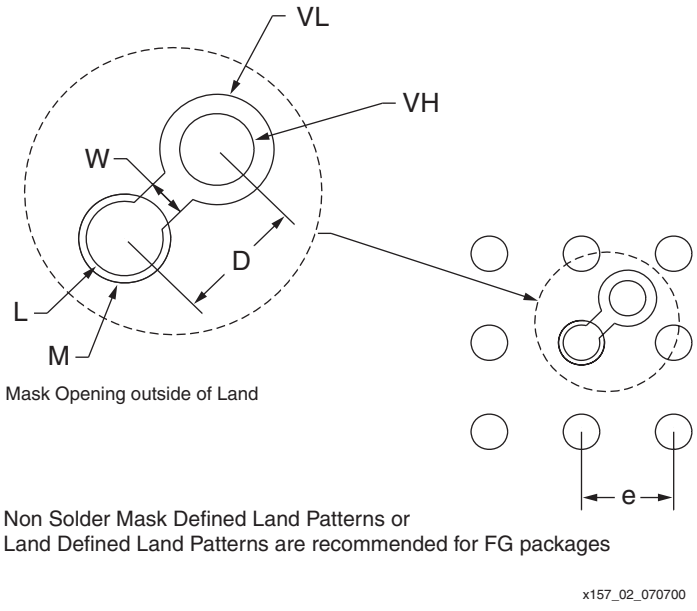



*Figure 5-3:* **Suggested Board Layout of Soldered Pads for BGA, CSP, and CCGA Packages***

*3x3 matrix for illustration only, one land pad shown with via connection.

*Table 5-3:* **Recommended PCB Design Rules (Dimensions in mm), Section 1**

| | FT256, FTG256 | FG256, FGG256, FG320, FGG320, FG324, FGG324 | FG400, FGG400, FG456, FGG456, FG676, FGG676, FG484 | FG680, FGG680 | FG860, FGG860 | FG900, FGG900 | FG1156, FGG1156 | FF668, FFG668, FF672, FFG672, FF896, FFG896 | FF1148, FFG1148, FF1152, FFG1152, FF1696, FFG1696 | FF1513, FFG1513, FF1517, FFG1517, FF1704, FFG1704 | SF363 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Component land Pad Diameter (SMD)(1) | 0.40 | 0.45 | 0.45 | 0.50 | 0.50 | 0.45 | 0.45 | 0.53 | 0.53 | 0.53 | 0.40 |
| Solder Land (L) Diameter | 0.40 | 0.40 | 0.40 | 0.40 | 0.40 | 0.40 | 0.40 | 0.45 | 0.45 | 0.45 | 0.33 |
| Opening in Solder Mask (M) Diameter | 0.50 | 0.50 | 0.50 | 0.50 | 0.50 | 0.50 | 0.50 | 0.55 | 0.55 | 0.55 | 0.50 |
| Solder (Ball) Land Pitch (e) | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | 0.80 |
| Line Width Between Via and Land (w) | 0.13 | 0.13 | 0.13 | 0.13 | 0.13 | 0.13 | 0.13 | 0.13 | 0.13 | 0.13 | 0.13 |
| Distance Between Via and Land (D) | 0.70 | 0.70 | 0.70 | 0.70 | 0.70 | 0.70 | 0.70 | 0.70 | 0.70 | 0.70 | 0.70 |
| Via Land (VL) Diameter | 0.61 | 0.61 | 0.61 | 0.61 | 0.61 | 0.61 | 0.61 | 0.61 | 0.61 | 0.61 | 0.50 |
| Through Hole (VH) Diameter | 0.300 | 0.300 | 0.300 | 0.300 | 0.300 | 0.300 | 0.300 | 0.300 | 0.300 | 0.300 | 0.300 |

**Notes:**

1. Component land pad diameter refers to the pad opening on the component side (solder mask defined).
2. FG456 package has solder balls in the center in addition to periphery rows of balls.

*Table 5-4:* **Recommended PCB Design Rules (mm), Section 2**

| | BG225 BGG225 | BG256 BGG256 | BG352 BGG352 | BG432 BGG432 | BG560 BGG560 | BG575 BGG575 | BG728 BGG728 | BF957 BFG957 | CS144, CSG144, CS280 CSG280 | FS48 FSG48 | CP56, CPG56 | CP132 CPG132 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Component land Pad Diameter(1) (SMD) | 0.63 | 0.63 | 0.63 | 0.63 | 0.63 | 0.61 | 0.61 | 0.61 | 0.35 | 0.40 | 0.30 | 0.30 |
| Solder Land (L) Diameter | 0.58 | 0.58 | 0.58 | 0.58 | 0.58 | 0.56 | 0.56 | 0.56 | 0.33 | 0.37 | 0.27 | 0.27 |
| Opening in Solder Mask (M) Diameter | 0.68 | 0.68 | 0.68 | 0.68 | 0.68 | 0.66 | 0.66 | 0.66 | 0.44 | 0.47 | 0.35 | 0.35 |
| Solder (Ball) Land Pitch (e) | 1.50 | 1.27 | 1.27 | 1.27 | 1.27 | 1.27 | 1.27 | 1.27 | 0.80 | 0.80 | 0.50 | 0.50 |
| Line Width Between Via and Land (w) | 0.300 | 0.203 | 0.203 | 0.203 | 0.203 | 0.203 | 0.203 | 0.203 | 0.13 | 0.13 | 0.13 | 0.13 |
| Distance Between Via and Land (D) | 1.06 | 0.90 | 0.90 | 0.90 | 0.90 | 0.90 | 0.90 | 0.90 | 0.56 | 0.56 | - | - |
| Via Land (VL) Diameter | 0.65 | 0.65 | 0.65 | 0.65 | 0.65 | 0.65 | 0.65 | 0.65 | 0.51 | 0.51 | 0.51 | 0.27 |
| Through Hole (VH) Diameter | 0.356 | 0.356 | 0.356 | 0.356 | 0.356 | 0.356 | 0.356 | 0.356 | 0.250 | 0.25 | 0.250 | 0.15 |

**Note:**

1. Component land pad diameter refers to the pad opening on the component side (solder mask defined).

*Table 5-5:* **Recommended PCB Design Rules (mm), Section 3**

| | CG560 | CG717 | CF1144 |
|---|---|---|---|
| Component land Pad Diameter(1) (SMD) | 0.86 | 0.86 | 0.80 |
| Solder Land (L) Diameter | 0.8 | 0.8 | 0.7 |
| Opening in Solder Mask (M) Diameter | 0.9 | 0.9 | 0.8 |
| Solder (Ball) Land Pitch (e) | 1.27 | 1.27 | 1.0 |
| Line Width Between Via and Land (w) | 0.300 | 0.300 | 0.200 |
| Distance Between Via and Land (D) | 0.9 | 0.9 | 0.7 |
| Via Land (VL) Diameter | 0.65 | 0.65 | 0.61 |
| Through Hole (VH) Diameter | 0.305 | 0.305 | 0.200 |

**Note:**

1. Component land pad diameter refers to the pad opening on the component side (solder mask defined).

# Board Routability Guidelines with Xilinx Fine-Pitch BGA Packages

Xilinx supplies full array fine-pitch BGA (Ball Grid Array) packages with 1.00 mm ball pitch. Successful and effective routing of these packages on PC boards is a significant challenge to designers. This application note provides board level routing guidelines for using Xilinx fine-pitch BGA packages. Specific examples are provided to choose appropriate routing schemes. These examples are based on package and board design rules for standard PCB technology and are not drawn to scale.

## Board Level Routing Challenges

### 1.0 mm Ball Pitch, Fine-Pitch BGA

Xilinx fine-pitch BGA packages have a full matrix of solder balls (Figure 5-4). These packages are made of multilayer BT substrates. Signal balls are in a perimeter format extending up to eight rows in FG676 packages and up to ten rows in FG1156 packages. Power and ground pins are grouped together appropriately.

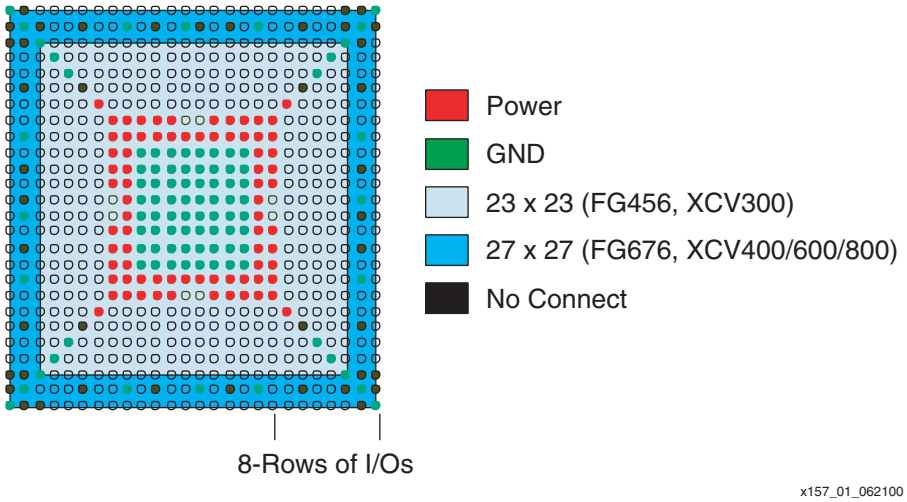



*Figure 5-4:* **Fine Pitch BGA Pin Assignments**

The number of layers required for effective routing of fine-pitch BGA packages is dictated by the layout of pins on each package. If several other technologies and components are already present on the board, the system cost is factored with every added board layer. The intent of a board designer is to optimize the number of layers required considering both cost and performance. This application note provides guidelines to minimize the required board layers for routing fine-pitch BGA products using standard PCB technologies (5/5 mils lines/space or 6/6 mils lines/space).

For high performance and other system needs, designers can use premium technologies with finer lines/spaces on the board. The pin assignment and pin grouping scheme on full array fine-pitch BGA packages enables an efficient way of routing the board with an optimum number of required board layers.

## Board Routing Strategy

### Minimum Requirements

The diameter of a land pad on the component side is provided by Xilinx. This information is required prior to the start of the board layout to design the board pads to match the component side land geometry. The typical values of these land pads are described in Figure 5-3.

For FG series packages, NSMD (Non Solder Mask Defined) pads on the board are suggested. This allows a clearance between the land metal (diameter L) and the solder mask opening (diameter M) as shown in Figure 5-3. The space between the NSMD pad and the solder mask, and the actual signal trace widths depends on the capability of the PCB vendor. The cost of the PCB is higher when the line width and spaces are smaller.

Selection of the pad types and pad sizes determines the available space between adjacent balls for signal escape. Based on PCB capability, the number of lines that can share the available space is described in Figure 5-5. Based on geometrical considerations, if one signal escapes between adjacent balls, then two signal rows can be routed on a single metal layer. This is illustrated in Figure 5-5 as routing with one line/channel, either at 6 mils lines and spaces or 5 mils lines and spaces. Using this suggested routing scheme. a minimum of eight PCB layers are required to route 10 signal rows in a package.

A slightly lower trace width can be used by the inner signal rows routed in internal layers than the top and bottom external or exposed traces. Depending on the signal being handled, the practice of "necking down" a trace in the critical space between the BGA balls is allowable. Changes in width over very short distances can cause small impedance changes. Validate these issues with the board vendor and signal integrity engineers responsible for design.

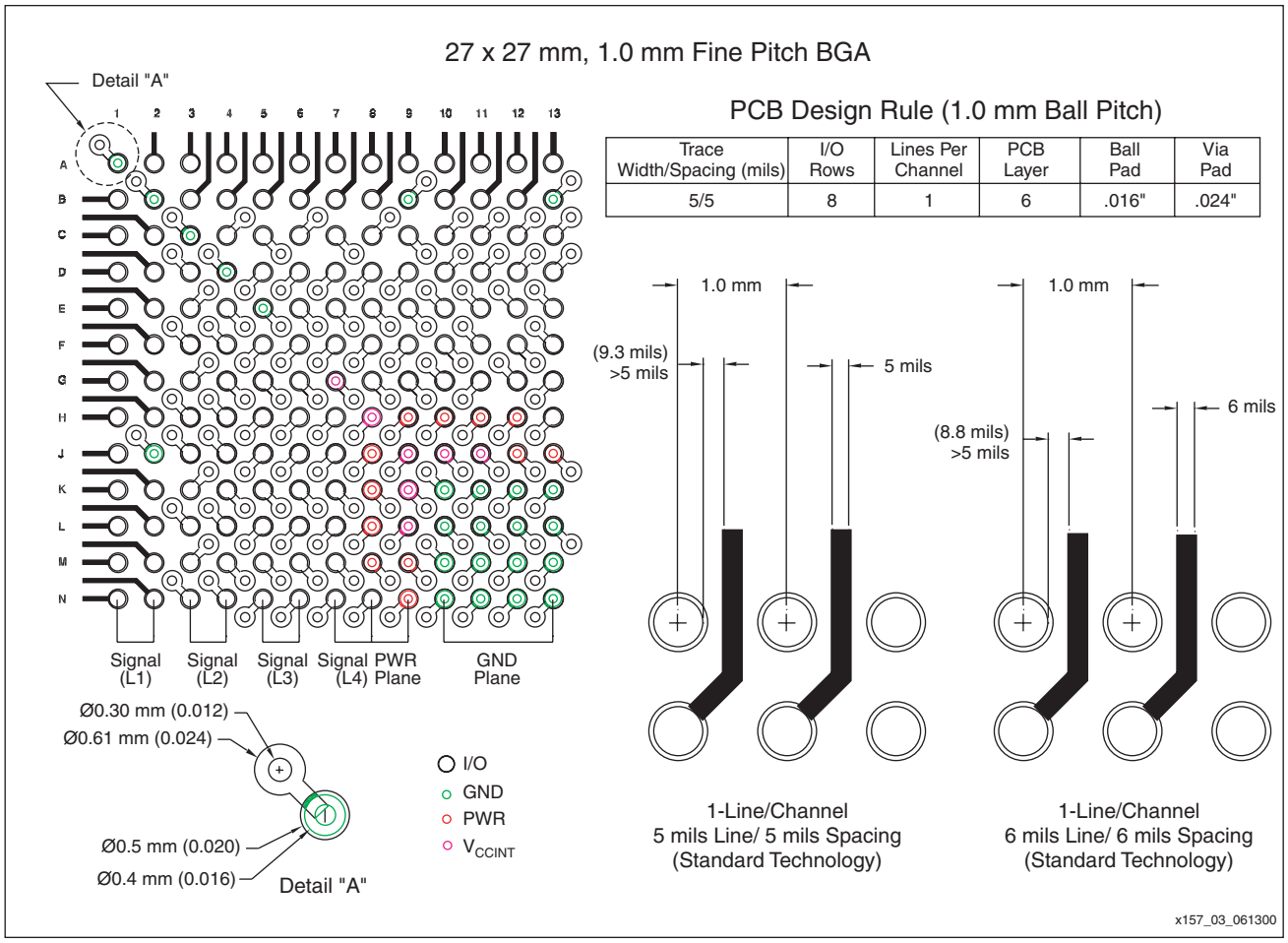



*Figure 5-5:* **FG676 PC Board Layout/Land Pattern**

Figure 5-5 describes a board-level layout strategy for a Xilinx 1.0 mm pitch FG676 package. Detail A in Figure 5-5 describes the opening geometry for the Land Pad and the Solder Mask. Routing with 5 mils lines/trace allows one signal per channel (between the balls). For successful routing, eight row deep signal traces require six PCB layers. Figure 5-6 shows the suggested schematic of layers for the six-layer routing scheme.

Using premium board technology such as Microvia Technology (allowing up to 4 mils lines and spaces) efficient routing is possible with a reduced number of board layers. A grouping scheme for power, ground, control and I/O pins, may also enable efficient routing.

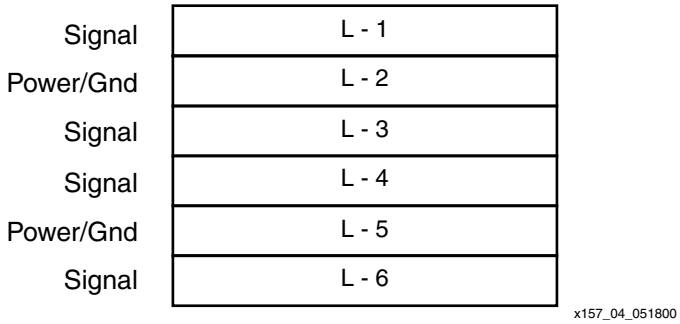



*Figure 5-6:* **Six-Layer Routing Scheme**

## Board Routing Examples

Figure 5-7 through Figure 5-11 offer examples of layer-by-layer board routing implementation using the rules outlined above for the Virtex™-E family of 1.0 mm BGA packages - FG256, FG456, FG676, FG900, and FG1156. The rule used assumes 5 mils lines and spaces. This is just an illustration of how the strategies outlined above can be used; it does not represent any specific implementation pin-out.

Similar board layout examples may be generated for other family (Virtex-II, Virtex-II Pro, etc.) pin-outs with the rules and strategies discussed in this section. It should be noted that the need to shield high-speed signals and meet Signal Integrity constraints might disrupt the plane sequence.

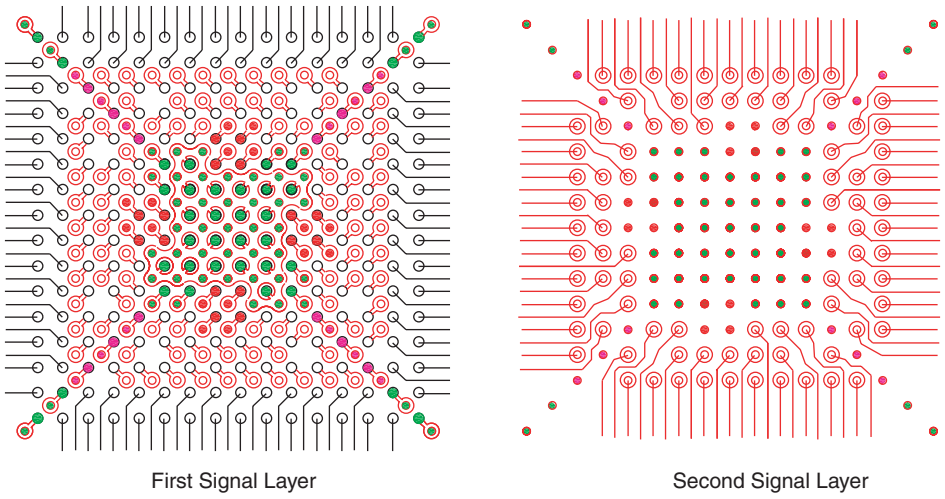
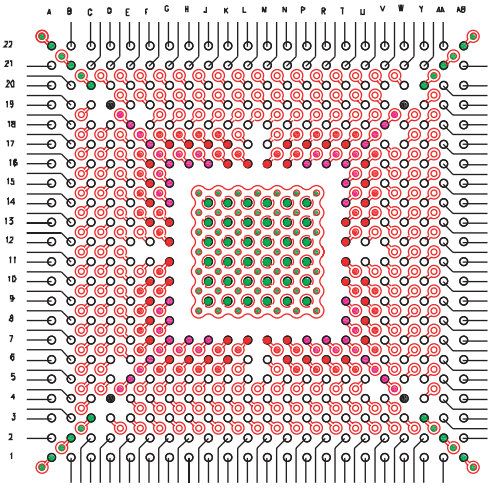
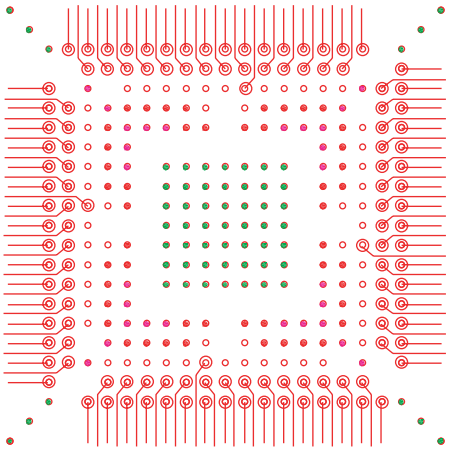


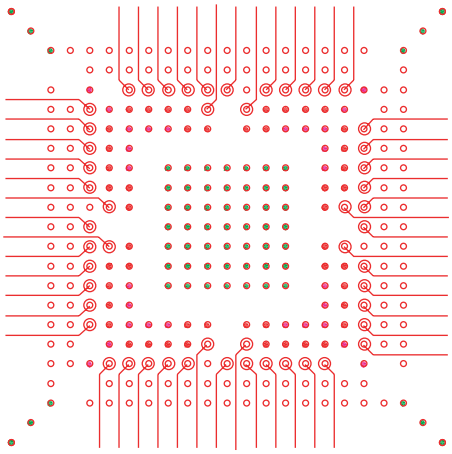

*Figure 5-7:* **XCV300E - FG256 NSMD Land Pad**



First Signal Layer



Second Signal Layer

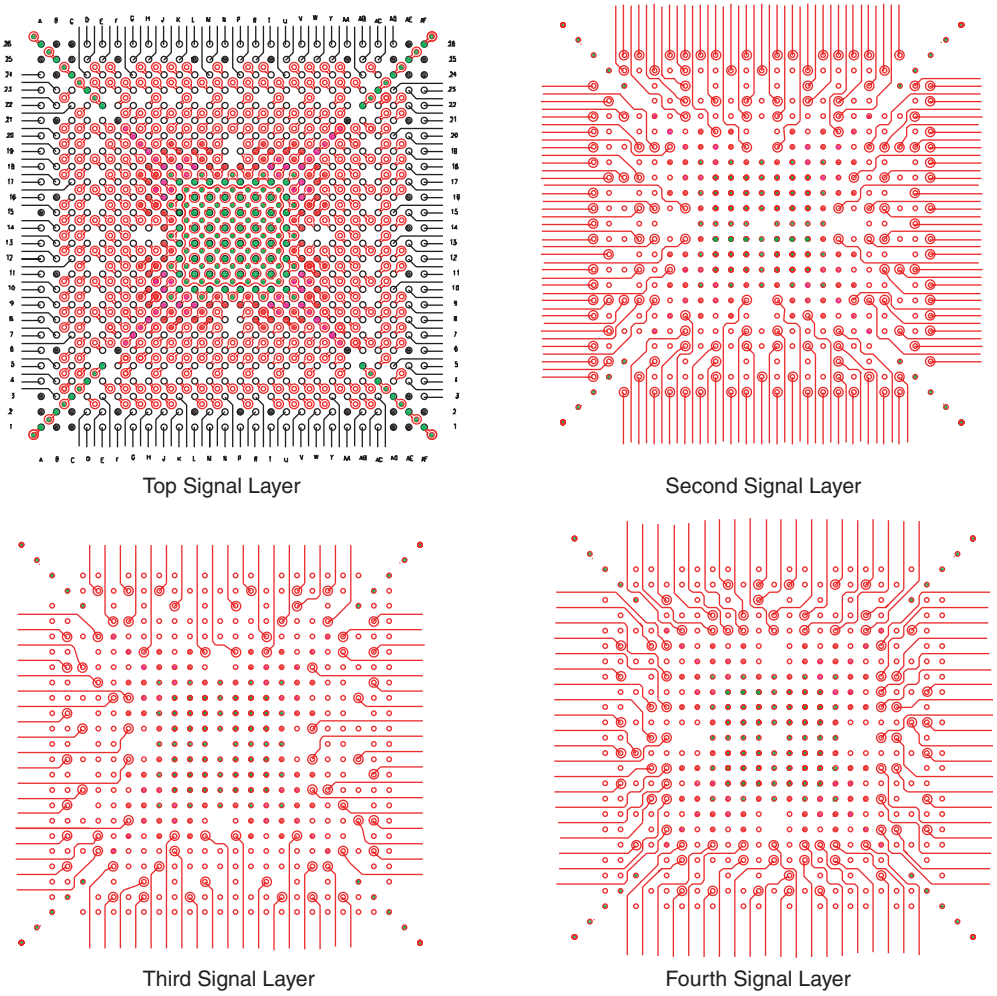


Third Signal Layer

Notes:
1) Solder land diameter 0.4 mm Nonsolder Mask Defined.
2) Solder Mask Opening 0.5 mm diameter.
3) Via diameter 0.3 mm on 0.61 mm diameter Via Land.
4) All Layers trace width 0.127 mm.

x157_06_072600

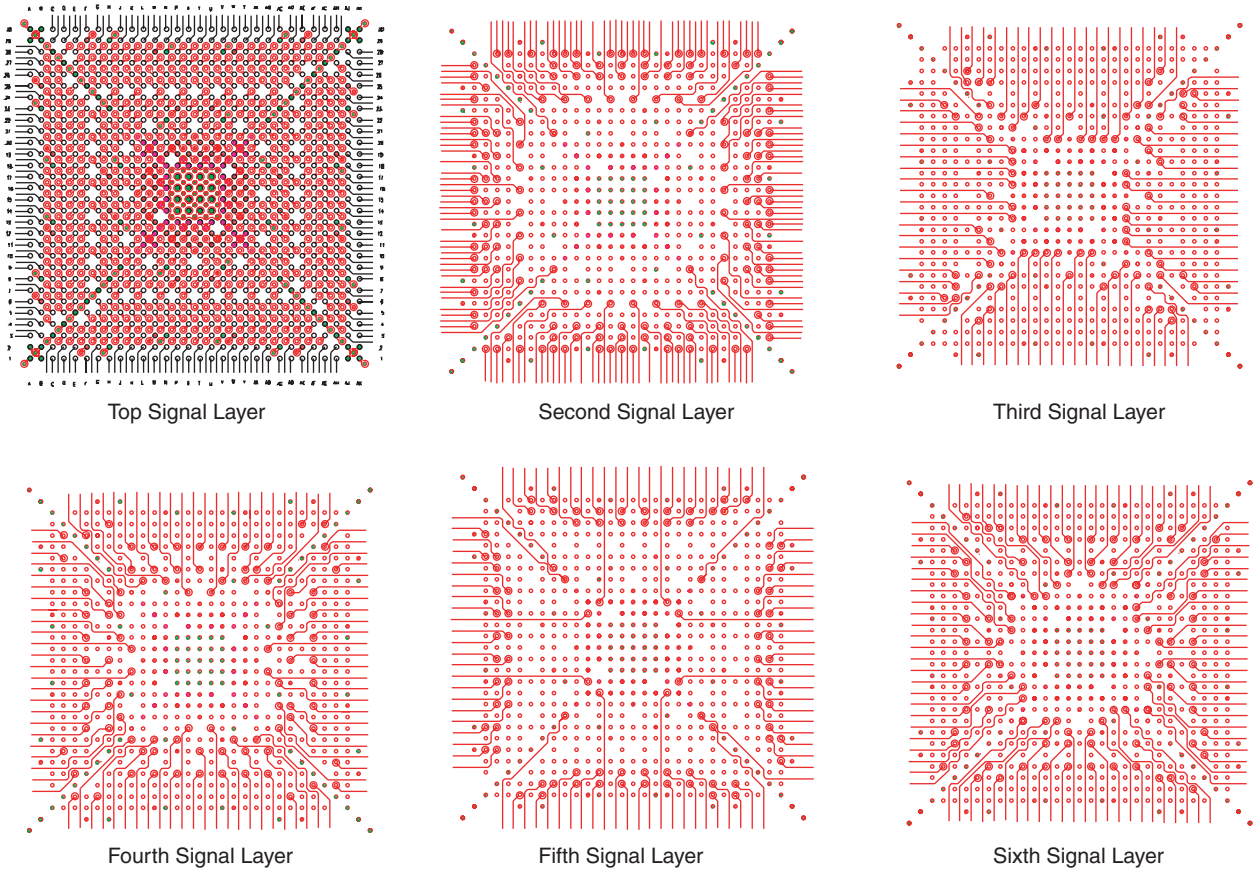
*Figure 5-8:* **XCV300E - FG456 NSMD Land Pad**




Notes:
1) Solder Land diameter 0.4 mm Nonsolder Mask Defined.
2) Solder Mask opening diameter 0.5 mm.
3) Via diameter 0.3 mm on 0.61 mm diameter Via Land.
4) Trace width 0.127 mm.

x157_07_072600

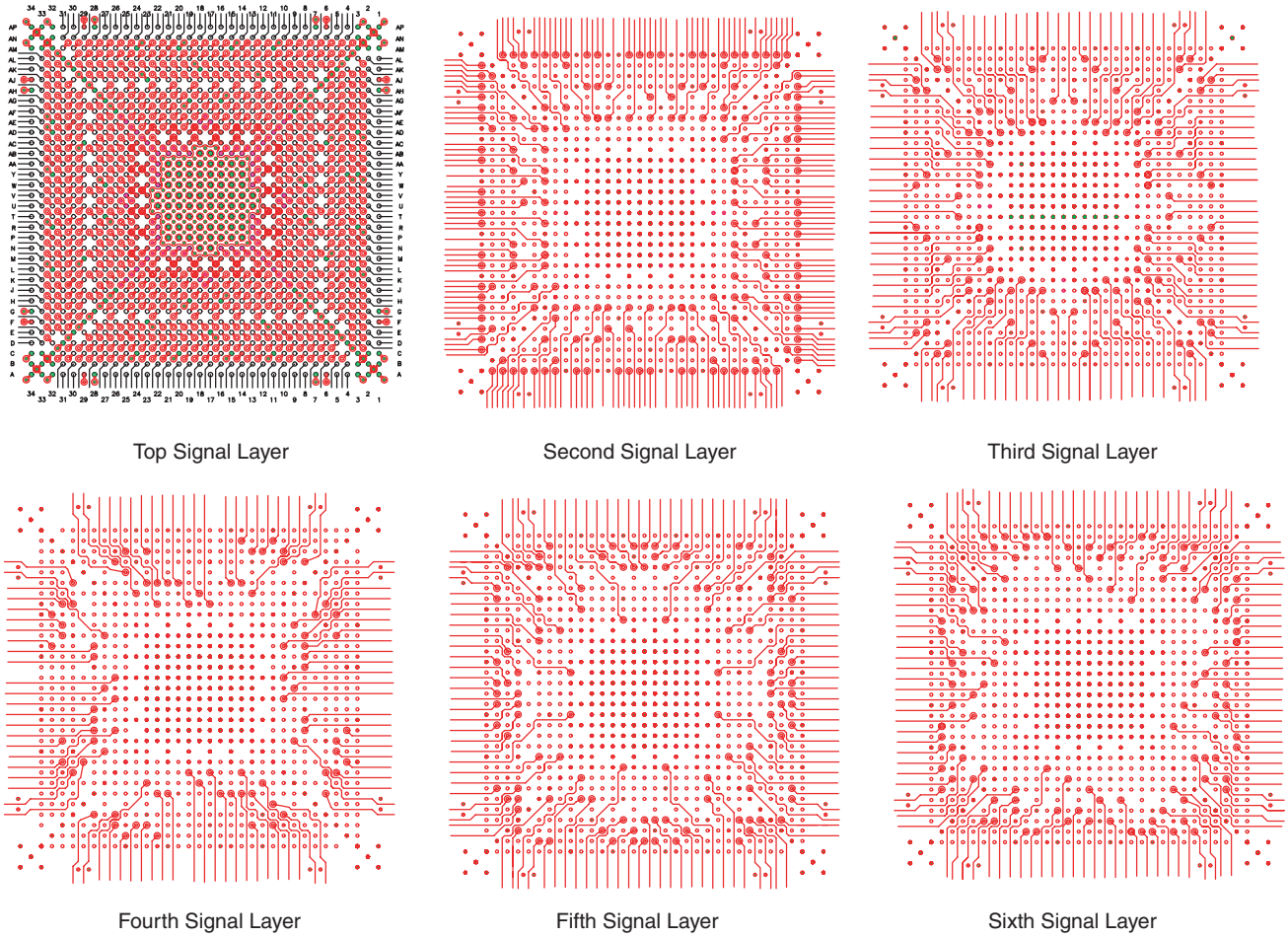
*Figure 5-9:* **XCV800 - FG676 NSMD Land Pad**




Notes:
1) Solder Land diameter 0.4 mm Nonsolder Mask Defined.
2) Solder Mask opening diameter 0.5 mm.
3) Via diameter 0.3 mm on 0.61 mm diameter Via Land.
4) Trace width 0.127 mm.

x157_08_072600

*Figure 5-10:* **XCV1600E - FG900 NSMD Solder Land Pad Layout**




Notes:
1) Solder Land diameter 0.4 mm Nonsolder Mask Defined.
2) Solder Mask Opening diameter 0.5 mm.
3) Via diameter 0.3 mm on 0.61 mm diameter Via Land.
4) All layers, trace width 0.127 mm.

x157_09_041002

*Figure 5-11:* **XCV2000E - FG1156 NSMD Solder Land Pad Layout**

# Recommended PCB Design Rules for QFN Packages

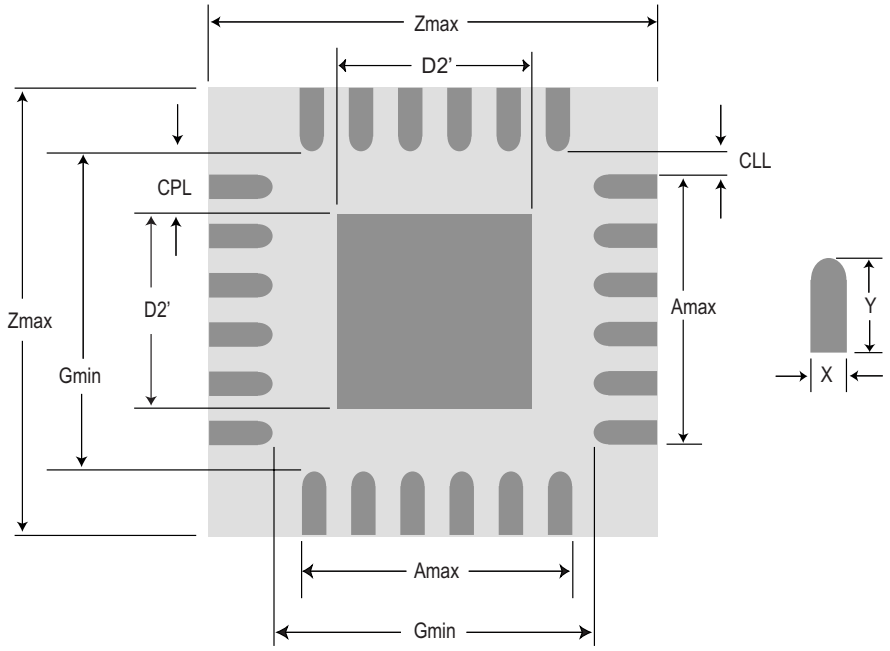



*Figure 5-12:* **IPC Standard Board Layout of Soldered Pads for QFN Packages**

*Table 5-6:* **Recommended PCB Land Pattern Dimensions (mm)**

| Package | | | PCB Land Pattern Dimensions | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Package** | **Body Size** | **Lead Pitch** | **Xmax** | **Yref** | **Amax** | **Gmin** | **Zmax** | **D2max** | **CLL(1)** | **CPL(2)** |
| QFG32 | 5 x 5 | 0.50 | 0.28 | 0.69 | 3.78 | 3.93 | 5.31 | 3.63 | 0.10 | 0.15 |
| QFG48 | 7 x 7 | 0.50 | 0.28 | 0.69 | 5.78 | 5.93 | 7.31 | 5.63 | 0.10 | 0.15 |

1. CLL defines the minimum distance between land to land for the corner joints on adjacent sides.
2. CPL defines the minimum distance between the inner tip of the peripheral lands and the outer edge of the thermal pad.

## PCB Pad Pattern Design and Surface-Mount Considerations for QFN Packages

Xilinx Quad Flat No-Lead (QFN) package is a robust and low profile leadframe-based plastic package that has several advantages over traditional leadframe packages.The exposed die attach paddle enables efficient thermal dissipation when directly soldered to the PCB. Additionally, this near chip scale package offers improved electrical performance, smaller package size, and an absence of external leads. Since the package has no external leads, coplanarity and bent leads are no longer a concern.

The exposed pads at the bottom of a QFN package may be used to enhance both electrical and thermal performance of the QFN component. To implement this, note that the exposed pad is a weak ground through its connection to the silicon. Under no circumstances should the pad be connected to a positive or negative voltage. The paddle should only be left floating or connected to corresponding ground pad on the board. Ground pads

incorporating thermal vias in them will significantly improve thermal performance, as shown in Figure 5-14.

The following factors have major effect on the quality and reliability of assembling QFN packages: PCB pad pattern design, amount of solder paste in thermal pad region, stencil design, type of solder paste, and reflow profile. This application note provides a good guideline on PCB pad pattern design and assembling of QFN packages for optimal reliability and quality. This is only a guideline and users are encouraged to perform actual studies to optimize the process.

## PCB Pad Patterns

Figure 5-13 shows the PCB pad pattern dimensions to be determined. The dimension X and Y indicate the width and length of the pad. CLL and CPL define the clearances needed to avoid solder bridging. CLL defines the minimum distance between land to land for the corner joints on adjacent sides and CPL defines the minimum distance between the inner tip of the peripheral lands and the outer edge of the thermal pad. CLL should be 0.1 mm and CPL should be 0.15mm.

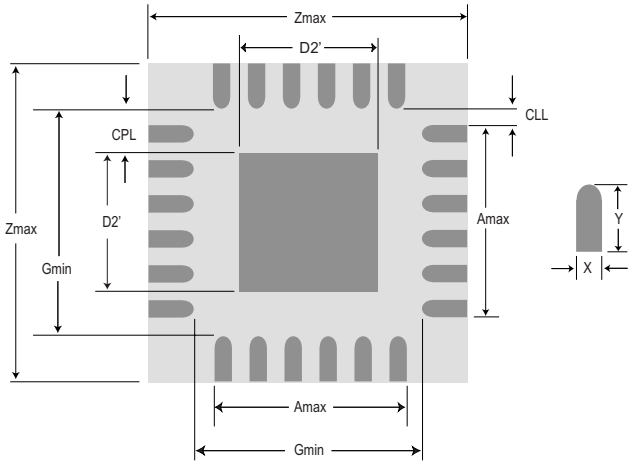



*Figure 5-13:* **PCB Land Pattern Dimensions**

Tolerance analysis should be performed on the package and the PCB dimensions in order to design a proper pad pattern. The recommended PCB land pattern dimensions are shown in Table 5-6.

*Table 5-7:* **Recommended PCB Land Pattern Dimensions (all dimensions in mm)**

| Package | | | PCB Land Pattern Dimensions | | | | | |
|---|---|---|---|---|---|---|---|---|
| Package | Body Size | Lead Pitch | Xmax | Yref | Amax | Gmin | Zmax | D2max |
| QFG32 | 5 x 5 | 0.50 | 0.28 | 0.69 | 3.78 | 3.93 | 5.31 | 3.63 |
| QFG48 | 7 x 7 | 0.50 | 0.28 | 0.69 | 5.78 | 5.93 | 7.31 | 5.63 |

## Thermal Pad and Via Design

Typical deployment of a QFN package has a thermal resistance (theta-JA) of 35 - 45° C/Watt (depending on package size). When needed, the base performance can be improved and a lower overall theta-JA is achieved by taking advantage of the exposed thermal pad feature. To take advantage of the exposed thermal pad under the package, the PCB should incorporate thermal pad and thermal vias. The thermal pad on the PCB acts as a solderable surface and the thermal vias provide a thermal path to the inner and/or bottom layers of the PCB to remove the heat. The number of thermal vias will depend on the following: application, power dissipation and electrical requirements. The thermal performance gets better as more thermal vias are added. However, there is a point of diminishing returns as shown in Figure 5-14 where the effect of number of vias on theta-JA is plotted for a 7mm, 48 lead package. A via diameter of 0.3 mm was used for this simulation.

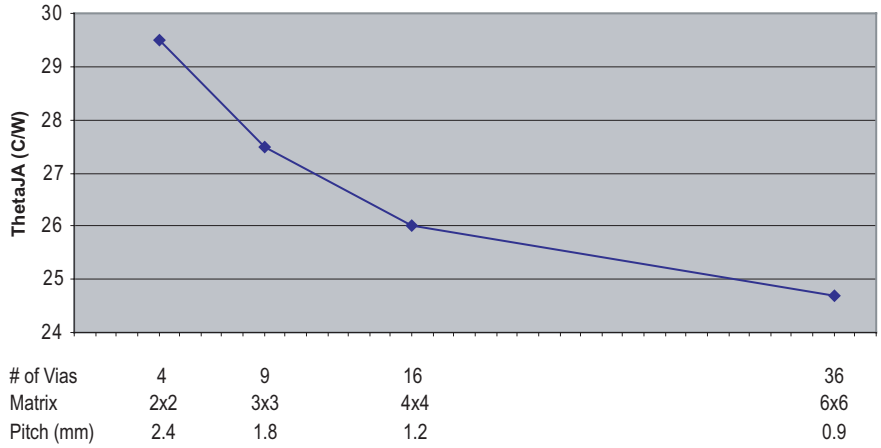



*Figure 5-14:* **Theta-JA vs. Number of Vias Graph**

Based on the above and similar thermal simulations, it is recommended to incorporate an array of thermal vias that have pitch of 1.0 to 1.2 mm with via diameter of 0.3 to 0.33 mm.

## Solder Masking Considerations

The PCB have pads that are either solder mask defined (SMD) or non solder mask defined (NSMD). NSMD pads are preferred over SMD pads since the copper etching process has tighter control than the solder masking process. Furthermore, NSMD pads with solder mask opening larger than the metal pad size improves the reliability of the solder joints as solder is allowed to wrap around the sides of metal pads.

The solder mask opening should be larger than the pad size by 120 to 150 microns. This results in a clearance of 60 – 75 microns between the copper pad and the solder mask.

The thermal pad area may be solder mask defined in order to avoid any solder bridging between the thermal pad and the perimeter pads. The mask opening should be 100 microns smaller than the thermal land size on all four sides.

## Stencil Design for Perimeter Pads

To achieve reliable solder joints, the solder joints on the perimeter pads should have about 50 to 75 microns standoff height and good side fillet on the outside. Good stand off can be achieved by having a stencil aperture opening that allows for maximum paste release. This is accomplished by having an area ratio that is greater than 0.66 and an aspect ratio that is greater than 1.5. Area Ratio and Aspect Ratio is defined below:

Area Ratio = LW/2T(L+W)

Aspect Ratio = W/T

Where L and W are the aperture length and width, and T is the stencil thickness. The stencil aperture should have a 1:1 ratio with the PCB pad sizes as both area and aspect ratio targets can easily be achieved by this aperture. Also, the stencil should be laser cut and electro-polished.

## Stencil Design for Thermal Pad

To enhance thermal and electrical performance, the die paddle should be soldered to the PCB thermal pad (see "PCB Pad Pattern Design and Surface-Mount Considerations for QFN Packages," page 96). Since outgassing occurs during reflow process and may cause defects such as splatter and solder balling, care must be taken to avoid large solder paste coverage. Thus, it is recommended to use smaller multiple openings in the stencil instead of one big opening for printing solder paste on the thermal pad area. By doing this, 50 to 80% solder paste coverage can be achieved. Figure 5-15 below shows one way to achieve these levels of solder paste coverage.

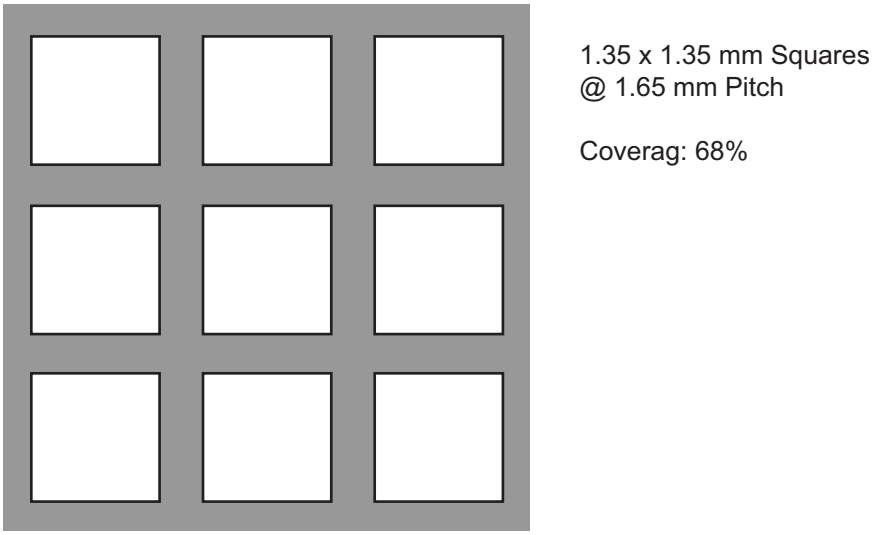



*Figure 5-15:* **Thermal Pad Stencil Design**

## Via Types and Solder Voiding

Voids in the thermal pad region are not expected to degrade thermal and electrical performance. However, large voids in the thermal pad area should be avoided. To control these voids, solder masking may be required for thermal vias to prevent solder wicking inside the via during reflow. Methods commonly used in the industry to control the voids include "via tenting" (top or bottom side) using dry film solder mask, "via plugging" with

liquid photo-imageable (LPI) solder mask from the bottom side, or "via encroaching". Figure 5-16 shows these options. For via tenting, the solder mask diameter should be 100 microns larger than the diameter of the via.

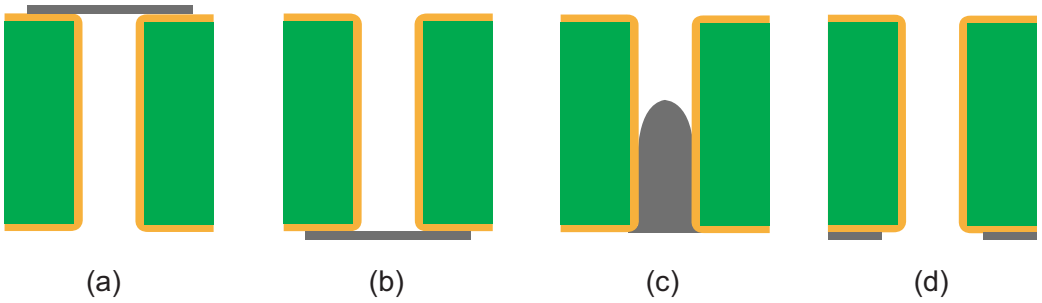



*Figure 5-16:* **Solder mask options for thermal vias: (a) via tenting from top, (b) via tenting from bottom, (c) via plugging from bottom, and (d) via encroached from bottom.**

There are advantages/disadvantages to each of these options. Via tenting from top side may result in smaller voids, but the presence of solder mask on the top side of the board may hinder proper paste printing. Via tenting from the bottom and via plugging from the bottom may result in larger voids because of outgassing. Finally, encroached vias allow the solder to wick inside the vias and reduce the size of the voids. This option, however, result in lower standoff of the package.

## Stencil Thickness and Solder Paste

For 0.5 mm pitch parts, a stencil thickness of 0.125 mm is recommended. Also, to improve the paste release, a stainless steel stencil with electro-polished trapezoidal walls is recommended.

For the paste, it is recommended to use "No Clean", Type 3 paste. Since the pads on the package are plated with 100% matte Sn, the package can be soldered using either Pb-free or SnPb solder paste.

## References

Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages, Dec. 2003.

Chapter 6

# Moisture Sensitivity of PSMCs

## Moisture-Induced Cracking During Solder Reflow

The surface mount reflow processing step subjects the Plastic Surface Mount Components (PSMC) to high thermal exposure and chemicals from solder fluxes and cleaning fluids during board mount assembly. The plastic mold compounds used for device encapsulation are, universally, hygroscopic and absorb moisture at a level determined by storage environment and other factors. Entrapped moisture can vaporize during rapid heating in the solder reflow process generating internal hydrostatic pressure. Additional stress is added due to thermal mismatch, and the Thermal Coefficient of Expansion (TCE) of plastic, metal lead frame, and silicon die. The resultant pressure may be sufficient to cause delamination within the package, or worse, an internal or external crack in the plastic package. Cracks in the plastic package can allow high moisture penetration, inducing transport of ionic contaminants to the die surface and increasing the potential for early device failure. Cracks in the plastic package can also result in broken/lifted bond wires.

How the effects of moisture in plastic packages and the critical moisture content result in package damage or failure is a complex function of several variables. Among them are package construction details—materials, design, geometry, die size, encapsulant thickness, encapsulant properties, TCE, and the amount of moisture absorbed. The PSMC moisture sensitivity has, in addition to package cracking, been identified as a contributor to delamination-related package failure artifacts. These package failure artifacts include bond lifting and breaking, wire neckdown, bond cratering, die attach separation, and die passivation/metal breakage.

Because of the importance of the PSMC moisture sensitivity, both device suppliers and device users have ownership and responsibility. The background for present conditions, moisture sensitivity standardized test and handling procedures have been published by two national organizations. Users and suppliers are urged to obtain copies of both documents (listed below) and use them rigorously. Xilinx adheres to both.

- IPC/JEDEC J-STD-020C

  "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices." Available on www.jedec.org website.

- IPC/JEDEC J-STD-033A

  "Standard for Handling, Packing, Shipping, and Use of Moisture/Reflow Sensitive Surface Mount Devices." Available on www.jedec.org website.

  None of the previously stated or following recommendations apply to parts in a socketed application. For board mounted parts careful handling by the supplier and the user is vital. Each of the above publications has addressed the sensitivity issue and has established eight levels of sensitivity (based on the variables identified). A replication of those listings, including the preconditioning and test requirements, and

the factory floor life conditions for each level are outlined in Table 6-1. Xilinx devices are characterized to their proper level as listed. This information is conveyed to the user via special labeling on the Moisture Barrier Bag (MBB).

The moisture sensitivity level number, found in Table 6-1, is printed on the MBB prior to shipment. This establishes the user's factory floor life conditions as listed in the time column. The soak requirement is the test limit used by Xilinx to determine the level number. This time includes manufacturer's exposure time or the time it will take for Xilinx to bag the product after baking.

*Table 6-1:* **Package Moisture Sensitivity Levels**

| Level | Floor Life | | Soak Requirements(1) | | | |
|---|---|---|---|---|---|---|
| | | | Standard | | Accelerated Equivalent(2) | |
| | Time | Conditions | Time (hours) | Conditions | Time (hrs) | Conditions |
| 1 | Unlimited | ≤30ºC/85% RH | 168 +5/-0 | 85ºC/85% RH | | |
| 2 | 1 year | ≤30ºC/60% RH | 168 +5/-0 | 85ºC/60% RH | | |
| 2a | 4 weeks | ≤30ºC/60% RH | 696(3) +5/-0 | 30ºC/60% RH | 120 +1/-0 | 60ºC/60% RH |
| 3 | 168 hours | ≤30ºC/60% RH | 192(3) +5/-0 | 30ºC/60% RH | 40 +1/-0 | 60ºC/60% RH |
| 4 | 72 hours | ≤30ºC/60% RH | 96(3) +2/-0 | 30ºC/60% RH | 20 +0.5/-0 | 60ºC/60% RH |
| 5 | 48 hours | ≤30ºC/60% RH | 72(3) +2/-0 | 30ºC/60% RH | 15 +0.5/-0 | 60ºC/60% RH |
| 5a | 24 hours | ≤30ºC/60% RH | 48(3) +2/-0 | 30ºC/60% RH | 10 +0.5/-0 | 60ºC/60% RH |
| 6 | Time on Label (TOL) | ≤30ºC/60% RH | TOL | 30ºC/60% RH | | |

**Notes:**

1. Suppliers may extend the soak time at their own risk.
2. **CAUTION** - The "accelerated equivalent" soak requirements shall not be used until correlation of damage response, including electrical, after soak and reflow is established with the "standard" soak requirements or if the known activation energy for diffusion is 0.4 - 0.48 eV. Accelerated soak times may vary depending on material properties; for example, mold compound, encapsulant, etc. JEDEC document JESD22-A120 provides a method for determining the diffusion coefficient.
3. The standard soak time includes a default value of 24 hours for the semiconductor manufacturer's exposure time (MET) between bake and bag and includes the maximum time allowed out of the bag at the distributor's facility.

   If the actual MET is less than 24 hours the soak time may be reduced. For soak conditions of 30ºC/60% RH, the soak time is reduced by one hour for each hour the MET is less than 24 hours. For soak conditions of 60ºC/60% RH, the soak time is reduced by one hour for each five hours the MET is less than 24 hours.

   If the actual MET is greater than 24 hours, the soak time must be increased. If soak conditions are 30ºC/60% RH, the soak time is increased one hour for each hour that the actual MET exceeds 24 hours. If soak conditions are 60ºC/60% RH, the soak time is increased one hour for each five hours that the actual MET exceeds 24 hours.

# Factory Floor Life

Factory floor life conditions for Xilinx devices are clearly stated on the MBB containing moisture sensitive PSMCs. These conditions have been ascertained by following test methods outlined in IPC/JEDEC J-STD-020C and are replicated in Table 6-1. If factory floor conditions are outside the stated environmental conditions (30°C/85% RH for Level 1, and 30°C/60% RH for Levels 2-6) or if time limits have been exceeded, then recovery can be achieved by baking the devices before the reflow step. Identified in the next section are two acceptable bake schedules. Either can be used for recovery to the required factory floor level.

# Dry Bake Recommendation and Dry Bag Policy

Xilinx recommends, as do the mentioned publications and other industry studies, that all moisture sensitive PSMCs be baked prior to use in surface mount applications, or comply strictly with requirements as specified on the MBB. Tape and Reeled parts are universally dry packed. Level 1 parts are shipped without the need for, or use of, an MBB. Note that to maintain level-1 status, the parts should be stored under conditions specified in Table 6-1 (≤30ºC/85% RH). Two bake schedules have been identified as acceptable and equivalent. The first is 24 hours in air at 125°C, in shipping media capable of handling that temperature. The second bake schedule is for 192 hours in a controlled atmosphere of 40°C, equal to or less than 5% RH.

Dry Devices are sealed in special military specification Moisture Barrier Bags (MBB). Enough desiccant pouches are enclosed in the MBB to maintain contents at less than 20% RH for up to 12 months from the date of seal. A reversible Humidity Indicator Card (HIC) is enclosed to monitor the internal humidity level. The loaded bag is then sealed shut under a partial vacuum with an impulse heat sealer.

Artwork on the bags provides storage, handling and use information. There are areas to mark the seal date, quantity, and moisture sensitivity level and other information. The following paragraphs contain additional information on handling PSMCs.

# Handling Parts in Sealed Bags

## Inspection

Note the seal date and all other printed or hand entered notations. Review the content information against what was ordered. Thoroughly inspect for holes, tears, or punctures that may expose contents. Xilinx strongly recommends that the MBB remain closed until it reaches the actual work station where the parts will be removed from the factory shipping form.

## Storage

The sealed MBB should be stored, unopened, in an environment of not more than 90% RH and 40ºC. The enclosed HIC is the only verification to show if the parts have been exposed to moisture. Nothing in the part's appearance can verify moisture levels.

## Expiration Date

The seal date is indicated on the MBB. The expiration date for dry packed SMD packages is 12 months from the seal date. If the expiration date has been exceeded or HIC shows exposure beyond 20% upon opening the bag bake the devices per the earlier stated bake schedules. The three following options apply after baking:

Use the devices within time limits stated on the MBB.

Reseal the parts completely under a partial vacuum with an impulse sealer (hot bar sealer) in an approved MBB within 12 hours, using fresh desiccant and HIC, and label accordingly. Partial closures using staples, plastic tape, or cloth tape are unacceptable.

Store the out-of-bag devices in a controlled atmosphere at less than 20% RH. A desiccator cabinet with controlled dry air or dry nitrogen is ideal.

### Other Conditions

Open the MBB when parts are to be used. Open the bag by cutting across the top as close to the seal as possible. This provides room for possible resealing and adhering to the reseal conditions outlined above. After opening, strictly adhere to factory floor life conditions to ensure that devices are maintained below critical moisture levels.

Bags opened for less than one hour (strongly dependent on environment) may be resealed with the original desiccant. If the bag is not resealed immediately, new desiccant or the old one that has been dried out may be used to reseal, if the factory floor life has not been exceeded. Note that factory floor life is cumulative. Any period of time when MBB is opened must be added to all other opened periods.

Both the desiccant pouches and the HIC are reversible. Restoration to dry condition is accomplished by baking at 125°C for 10-16 hours, depending on oven loading conditions.

## Assigned Package MSL

Table 6-2 depicts the typical MSL for various classes of Xilinx packages. Moisture level information will generally follow these MSL numbers for most products. Note that specific MSL information is always printed on the Moisture Barrier Bag (MBB) in which the components are shipped. The MSL printed on the MBB takes precedence over these typical values depicted in this table for a general overview.

*Table 6-2:* **Package MSL**

| Package Family | Description | Typical MSL |
|---|---|---|
| BF, FF, SF | Flip-Chip, FCBGA | 4 |
| BG | Ball Grid Array | 3 |
| CS, CP, QF, FS48 | Chipscale packages | 3 |
| FG, FT | Fine Ball Grid Array | 3 |
| HQ, HT, | Heat enhanced QFPs | 3 |
| PC | PLCC packages - product dependent | 3 |
| PD | Plastic Dual In Line | 1 |
| PQ, TQ, VQ | Plastic Quad Flat Packages | 3 |
| SO | SOIC packages | 1 |
| VO8/VO20/VO24 | TSSOP | 1 |
| CG1156 | Hi TEC ceramic | 3 |
| CB, CC, CD, CF, CG560, CG717, DD8, PG (all), WC | Ceramic Based packages - Not PSMC | Not sensitive - 1* |

**Notes:**

* Not PSMC component, not sensitive to moisture.

These Typical MSLs also apply to the lead-free components. The lead-free version of a package has the letter "G" appended after the 2-letter code (e.g., the lead-free package for FG will be FGG).

Chapter 7

# Reflow Soldering Process Guidelines

## Solder Reflow Process

The IR process is strongly dependent on equipment and loading differences. Components may overheat due to lack of thermal constraints. Unbalanced loading may lead to significant temperature variation on the board. This guideline is intended to assist users in avoiding damage to the components; the actual profile should be determined by those using these guidelines. For complete information on package moisture / reflow classification and package reflow conditions, refer to the Joint IPC/JEDEC Standard J-STD-020C.

To implement and control the production of surface-mount assemblies, the dynamics of the solder reflow process and how each element of the process is related to the end result must be thoroughly understood.

The primary phases of the reflow process are as follows:

1. Melting the particles in the solder paste
2. Wetting the surfaces to be joined
3. Solidifying the solder into a strong metallurgical bond

The sequence of five actions that occur during this process is shown in Figure 7-1. The profile below reflects the soldering sequences for Sn/Pb soldering system. For the Pb-free soldering system, the sequences are the same. However, for the Pb-free soldering system, higher reflow temperature is applied.

For reflow and rework guidelines on Pb-free packages, refer to XAPP427, http://www.xilinx.com/bvdocs/appnotes/xapp427.pdf.

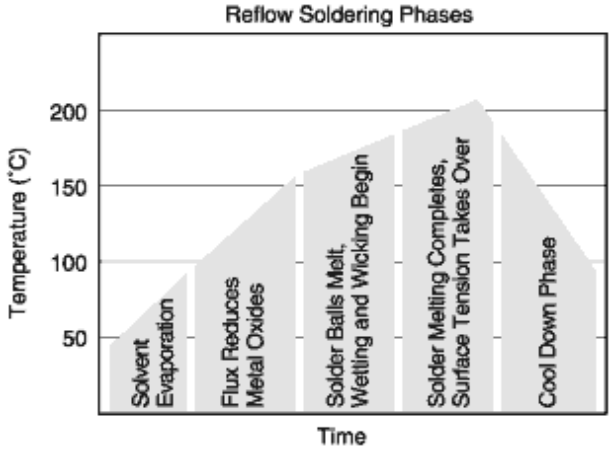



*Figure 7-1:* **Soldering Sequence**

### Package Peak Reflow Temperature

The peak reflow temperature of the PSMC body should not be more than 220°C (245°C for VQ44, VQ64, VQ100) for standard packages and 245-260°C for Pb-free package (package size dependent). For multiple BGAs in a single board, it is recommended to check all BGA sites for varying temperatures because of differences in surrounding components.

## Soldering Problems Summary

Each phase of a surface mount reflow profile has min/max limits that should be viewed as a process window. The process requires a careful selection and control of the materials, geometries of the mating surfaces (package footprint vs. PCB land pattern geometries) and the time/temperature of the profile. If all of the factors of the process are sufficiently optimized, there will be good solder wetting and fillet formation (between component leads and the land patterns on the substrate). If factors are not matched and optimized there can be potential problems as summarized in Figure 7-2.

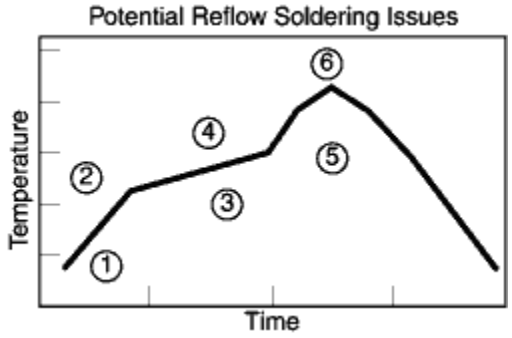



*Figure 7-2:* **Soldering Problems Summary**

**Soldering Problems Summary Notes:**

1. Insufficient Temperature to Evaporate Solvent
2. Component Shock and Solder Splatter
3. Insufficient Flux Activation
4. Excessive Flux Activity and Oxidation
5. Trapping of Solvent and Flux, Void Formation
6. Component and/or Board Damage

### Typical Conditions for IR Reflow Soldering

Figure 7-3 and Figure 7-4 show typical conditions for solder reflow processing of Sn/Pb soldering and Pb-free soldering using IR/Convection. Both IR and Convection furnaces are used for BGA assembly. The moisture sensitivity of Plastic Surface-Mount Components (PSMCs) must be verified prior to surface mount flow. See the preceding sections for a more complete discussion on PSMC moisture sensitivity.

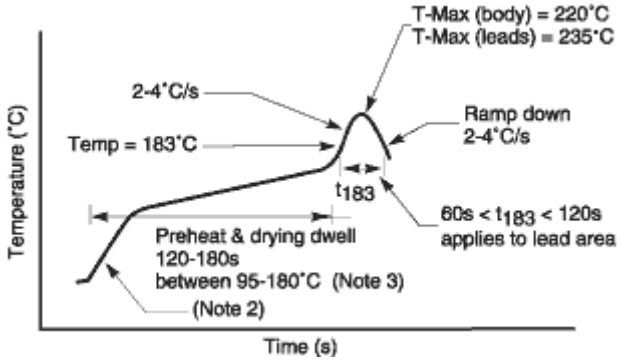



*Figure 7-3:* **Typical Conditions for IR Reflow Soldering of Sn/Pb Solder**

***Notes:***

1. Max temperature range = 220°C (body). Minimum temperature range before 205°C (leads/balls).
2. Preheat drying transition rate 2-4°C/s
3. Preheat dwell 95-180°C for 120-180 seconds
4. IR reflow shall be performed on dry packages
5. For MPM BGAs, do not reflow with lid on bottom

# Implementing and Optimizing Solder Reflow Process for BGA Packages

Xilinx flip chip BGA package is offered for Xilinx high-performance FPGA products. Unlike traditional packaging in which the die is attached to the substrate face up and the connection is made by using wire, the solder bumped die in flip chip BGA is flipped over and placed face down, with the conductive bumps connecting directly to the matching metal pads on the laminate substrate.

The primary purpose of solder reflow process is to wet the surfaces to be joined to form a strong metallurgical bond between the component and the PC board.

While the fundamentals of solder reflow process is the same for most applications, careful considerations must be taken for some of the larger and heavier BGA packages.

One of the most significant variables that can affect the package warpage is the solder reflow process. This application note discusses the details of the solder reflow process and provides guidelines on profiling to achieve successful reflow of BGA components.

## Reflow Ovens

Full convection ovens are preferred method for BGA assembly. Convection ovens provide more uniform heating and efficient heating across the board and the components. Convection ovens are especially recommended for applications that have a high mixture of components and densely populated boards.

## Reflow Process

During the reflow process, the components undergo reflow soldering phases, as shown in Figure 7-1.

As the components go through the five phases (Figure 7-1) in the oven, several actions take place to prepare a "clean" metal surface suitable for wetting and melting the solder, react with the interfaces, and solidify the solder onto the board. A typical profile with recommended settings for key parameters is shown in Table 7-1. A graphical representation of the typical profile can be found in Figure 7-5.

*Table 7-1:* **Process Window for Convection Oven**

| Process Steps | Process Description | Process Window |
|---|---|---|
| Preheat | Ramp Rate<br>Peak temperature in preheat | 1-3°C/sec<br>100°C-150°C |
| Preflow | Solder Paste Activation<br>Soak Time | 120°C-170°C<br>60-120 secs |
| Reflow | Time above 183°C<br>Peak Reflow Temperature<br>Component body temperature | 60-120 secs<br>200°C-210°C<br>220°C Max |
| Cool Down | Cooling Rate | 1-3°C/sec |

## Methods of Measuring Profiles

It is important to ensure that proper placement/attachment of thermocouples is carried out in order to accurately measure the desired temperatures. Thermocouples can be attached using either conductive epoxy or high temperature solders. Perhaps the easiest method to attach the thermocouple is by drilling through the pad of the PC board and attaching the thermocouple from the bottom of the PCB directly to the solder ball of the component.

Measurements should be taken at the following locations: center of the solder joint area of the component, the corner of the solder joint area of the component, the top surface of the component, and other components and locations on the PCB.

## Reflow Profiling

An optimized profile is paramount in achieving successful reflow result. A good starting point is to refer to the solder paste manufacturer's suggested reflow profile. However, solder paste manufacturers only supply the basic time/temperature duration information. To get an optimized reflow, components and board characteristics should dictate the maximum temperature and proper ramp rate.

Profiles should be established for all new board designs using thermocouples at multiple locations on the component (top, bottom, and corners-see Figure 7-4). In addition, if there are mixture of devices on the board, then the profile should be checked at different locations on the board to ensure that the minimum reflow temperature is reached to reflow the larger components and at the same time, the temperature does not exceed the threshold temperature that may damage the smaller, heat sensitive components. The minimum reflow temperature is the ideal thermal level at which the solder balls can be wetted to form the solder joints.

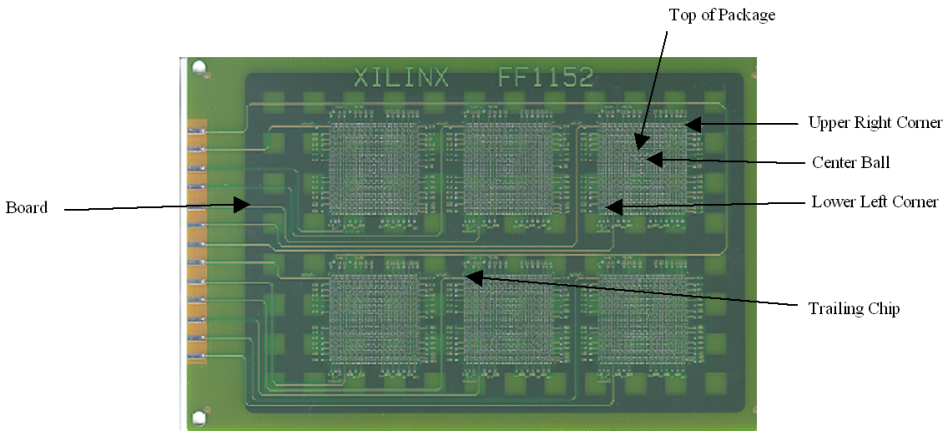



*Figure 7-4:* **Temperature Measurement Locations**

This information is usually provided by the solder paste manufacturers and it is typically 15-20°C above the solder's melting point. For eutectic (Sn63Pb37) solder, it is around 205-215°C.

It is critical to keep the temperature gradient across the board as minimal as possible (maintain less than 10°C) to prevent warpage of the components and the board. This is accomplished by using a slower rate in the warm-up and preheating stages. A heating rate of less than 1°C/sec during the initial stage, in combination with a heating rate of not more than 3°C/sec throughout the rest of the profile is recommended.

Aside from the board, it is also important to minimize the temperature gradient on the component, between top surface and bottom side, especially during the cool down phase. In fact, cooling is a crucial part of the reflow process and must be optimized accordingly. While a slow cooling rate may result in high assembly yields, it could lead to formation of thick intermetallic layers with large grain size; thereby, reducing the solder joint strength.

On the other hand, faster cooling rate leads to smaller solder joint grain size and hence resulting in higher solder joint fatigue resistance. However, overly aggressive cooling on stiff packages with large thermal mass such as flip chip BGAs may lead to cracking or package warpage, caused by the differential cooling effects between the top surface and bottom side of the component and between the component and the PCB materials.

The key is to have an optimized cooling with minimal temperature differential between the top surface of the package and the solder joint area. The temperature differential between the top surface of the component and the solder joint area should be as minimal as possible, preferably below 7°C during the critical region of the cool down phase of the reflow process. This critical region occurs at the phase in which the balls are not completely solidified to the board yet, usually between the 180°C and down to 160°C range. The best solution may be to divide the cooling section into multiple zones, with each zone operating at different temperatures to efficiently cool the parts. For a graphical representation of the typical reflow conditions for BGA, see Figure 7-5.

If second pass wave solder reflow is performed on the same board as BGAs, insure that the solder wafer profile is tightly controlled and consider shielding the BGA parts. The wave solder temperature profile can warp the board and break the solder joints on the topside of the BGA component

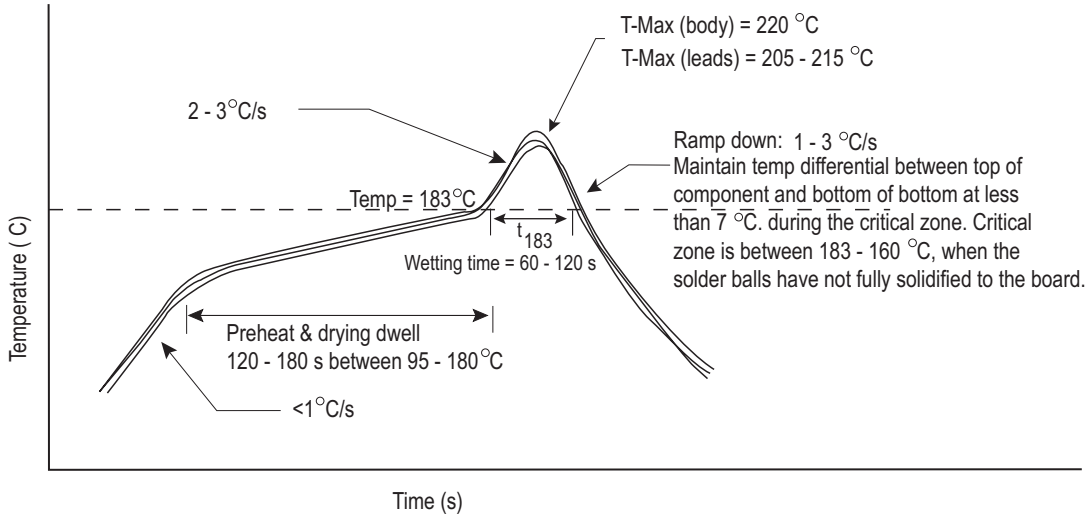



*Figure 7-5:* **Typical Solder Reflow Profile for BGA**

## Post Reflow Washing

Most major PCB assembly subcontractors today have successfully developed the no-clean process in which post assembly washing is not required. That would be an ideal process. If cleaning is required as part of the process, then it is recommended to use a water soluble paste and then wash with deionized water in a washer, such as a Westek Triton III at 140°F-145°F.

Cleaning solutions or solvents are not recommended as some cleaning solutions may contain chemicals that could attack the heatspreader adhesive, thermal compound, or the components inside the package.

## Reworking Flip Chip BGAs

Since the devices packaged in a flip chip BGA package are typically high performance and high priced devices, it is essential that proper procedures are followed to ensure successful rework of flip chip BGAs.

### Pre-Baking

As the printed circuit board and the BGA packages are quite moisture sensitive, one should always bake the PCBs and the BGA devices prior to any rework operations. The recommended temperature and duration is 125°C for at least four hours.

### BGA Removal

An accurate thermal profile needs to be established for the component removal process. This will determine the exposure duration and the maximum component/board temperatures.The profile should be adapted to each board and component to be removed. Although the typical profile should provide a peak temperature between 205 to 215°C (at the solder joint) for a maximum of 75 seconds, it is best, however, to consult with equipment manufacturer for the recommended profile.

Research has also indicated that a short delta T and a short dwell time above 183°C are preferred to minimize intermetallic growth and control board warpage. Also of importance is a need to assure that the component and the board are not overheated, and that all balls are reflowed on the specific component being removed. In general, preheat the entire board to a minimum of 85°C to avoid large temperature differentials and potential board warpage.

In terms of the equipment and tools available, automatic hot gas rework systems with vacuum suction are recommended. The nozzle should be designed such that most of the heat is applied at the solder joint area and not on the package. Excess heat can cause the lid attach epoxy to soften, which can cause the lid to come off. Apply heat from the topside using the rework profile developed (ramp the temperature for 45-60 secs with a maximum temperature between 205-215°C). When the solder balls are fully liquidus, remove the component using a vacuum tip. Do not attempt to remove partially reflowed component from a board by prying it off, as this would likely damage the component and can cause the lid to come off.

***Note:*** To avoid package delamination, the temperature at the top of the package must not exceed 225°C (245°C, 250°C, or 260°C for Pb-free Flip-Chip BGA packages, depending on package size).

## Site Preparation

The excess solder that remains on the board can be removed using a vacuum desoldering system or a soldering iron with a solder wick. Special care must be taken to avoid damaging the solder mask material and the solder pads. As a final step, alcohol may be used with a brush to clean the rework area. Allow the board to dry and inspect to ensure a clean solderable surface. The specific steps used here may be different from board to board and from company to company. As a minimum, the removal of the excess solder is an essential requirement.

## Solder Paste Application

There are several options available to apply the solder paste to the component site. The BGA package itself may be screened with paste prior to placement. In addition, the site may receive solder paste with a dispensing method. Finally the application of flux to a prepared pre-tinned site can produce acceptable results in most situations.

## BGA Placement and Reflow

The next step is to replace the component on the board. The replacement component should be baked prior to assembly if the component has been exposed to the environment for more than the allotted time. Place the component on the site, observing all the alignment precautions. Reflow the balls using hot air in a manner similar to the removal process. Again observe total board temperature to avoid any thermal gradients that can result in board warpage. It is recommended to heat the PCB from the underside to a given temperature (depending on the board size and properties), preferably in the 80°C-145°C range.

Heating the underside of the board can help to minimize the temperature gradient on the board.

Additionally, larger BGA components such as Flip Chip BGAs are quite sensitive to heat; therefore, extra precautions are necessary to ensure successful result. It is critical to minimize the temperature gradient on the part. High temperature gradient will create thermal shock that leads to package warpage. The temperature delta between the following locations should be 7°C or less: the solder balls on the corners, the solder balls at

the center of the package, and the top surface side of the package. To achieve minimal temperature gradient, a slower ramp up rate (0.5°C/sec) and a lower peak reflow temperature (200°C as measured at the solder balls) is recommended. Additionally, cooling should be optimized to minimize the temperature differential as described under the Reflow Profiling, page 4.

## BGA Reballing

Xilinx does not recommend reballing. Xilinx parts that are reballed will not be guaranteed by Xilinx. A maximum of three reflow cycles are allowed.

## Conformal Coating

Xilinx has no experience or reliability data on flip chip BGA packages on board after exposure to conformal coating. It is recommended that the end-user should characterize the board level reliability performance of Xilinx packages before production use.

## Post Assembly Handling

When assembling mechanical connectors or fixtures to the PB board, users should be careful not to create excessive bowing or flexing on the PB board as this might weaken or cause damage to the solder joints interface.

## Heat Sink Removal Procedure

The heatspreader on the package provides mechanical protection for the die and serves as the primary heat dissipation path. It is attached with an epoxy adhesive to provide the necessary adhesion strength to hold the package together. For an application in which an external heatsink subjects the lid adhesion joint to continuous tension or shear, extra support may be required.

In addition, if the removal of an attached external heat sink subjects the joint to tension, torque, or shear, care should be exercised to ensure that the lid itself does not come off. In such cases, it has been found useful to use a small metal blade or metal wire to break the lid to heatsink joint from the corners and carefully pry the heatsink off. The initial cut should reach far in enough so that the blade has leverage to exert upward pressure against the heat sink. Please contact the heat sink and heat sink adhesive manufacturer for more specific recommendations on heat sink removal.

## Package Pressure Handling Capacity

For mounted BGA packages, including Flip-Chips, a direct compressive (non varying) force applied normally to the lid or top of package with a tool head that coincides with the lid (or is slightly bigger) will not induce mechanical damage to the device including external balls, provided the force is not over 5.0 grams per external ball, and the device and board are supported to prevent any flexing or bowing.

These components are tested in sockets with loads in the 5 to 10 gm/ball range for short durations. Analysis using a 10g/ball (e.g., 10 kg for FF1148) showed little impact on short-term but some creep over time. 20 gm/ball and 45 gm/ball loads at 85°C over a six week period has shown the beginning of bridging of some outer balls; these were static load tests. The component may survive forces greater than the 5 gm limit while in short-term situations. However, sustained higher loads should be avoided (particularly if they are overlaid with thermal or power cycle loads). Within the recommended limits, circuit board

needs to be properly supported to prevent any flexing resulting from force application. Any flexing or bowing resulting from such a force can likely damage the package-to-board connections. Besides the damage that can occur from bending, the only major concern is long-term creep and bulging of the solder balls in compression to cause bridging. For the life of a part, staying below the recommended limit will ensure against that remote possibility.

### References


1. Adams, Jeff, “Xilinx FF1152 Assembly Report”, March 27, 2001, Samina Corporation.
2. Gilleo, Ken, “Area Array Packaging Handbook”, copyrighted 2002 by McGraw-Hill Co., pages 14.14-14.16.
3. Hall, James, “Concentrating on Reflow's Cooling Zones”, EP&P, 3/01/2001
4. Narrow, Phil, “Soldering”, SMT Magazine, Aug. 2000
5. O'Donnell, Dennis, “BGA Rework Practices”, Precision PCB Services Inc., 2001


## QFN Reflow Profile

Reflow profile for QFN packages is similar to reflow profile of other SMT packages. It is recommended to follow the paste manufacturer’s specification on peak reflow temperature, soak times, time above liquidus, and ramp rates. Typical profile for Sn/Pb solder paste has a peak temperature between 220-235°C with time above liquidus between 60-90 seconds.

Appendix

# Additional Information

## Table of Socket Manufacturers

Table 1 lists manufacturers known to offer sockets for Xilinx Package types. This summary does not imply an endorsement by Xilinx. Each user has the responsibility to evaluate and approve a particular socket manufacturer.

*Table-1:* **Socket Manufacturers Packages**

| Manufacturer | Packages | | | | | |
|---|---|---|---|---|---|---|
| | DIP, SO, VO | PC, WC | PQ, HQ, TQ, VQ | PG, PP | CB | BG, CG |
| Advanced Interconnect<br>5 Energy Way, P.O. Box 1019<br>W. Warwick, RI 02893<br>Toll Free: 1-800-424-9850<br>www.advintcorp.com | X | X | - | X | - | - |
| AMP Inc.<br>470 Friendship Road<br>Harrisburg, PA 17105-3608<br>(800) 522-6752<br>www.amp.com | X | X | - | X | - | - |
| Aries Electronics<br>P.O. Box 130<br>Frenchtown, NJ 08825<br>Phone: 908-996-6841<br>www.arieselec.com | X | X | - | X | - | X |
| Interconnect Systems, Inc.<br>708 Via Alondra<br>Camarillo, CA 93012<br>Phone: 805-482-2870 | | | | | | X |
| Ironwood Electronics Inc.<br>P.O. Box 21151<br>St. Paul, MN 55121<br>Phone: 651-452-8100<br>www.ironwoodelectronics.com | X | - | - | X | - | X |

*Table-1:* **Socket Manufacturers Packages *(Continued)***

| Manufacturer | Packages | | | | | |
|---|---|---|---|---|---|---|
| | DIP, SO, VO | PC, WC | PQ, HQ, TQ, VQ | PG, PP | CB | BG, CG |
| McKenzie Socket Division<br>910 Page Avenue<br>Fremont, CA 94538<br>(510) 651-2700 | X | X | - | X | - | - |
| Mill-Max MFG. Corporation<br>190 Pine Hollow Road<br>P.O. Box 300<br>Oyster Bay, NY 11771<br>Phone: 516-922-6000<br>www.mill-max.com | X | X | - | X | - | X |
| 3M Textool<br>6801 River Place Blvd.<br>Austin, TX 78726-9000<br>(800) 328-0411<br>www.3m.com | | | | X | X | X |
| Wells Electronics<br>1701 South Main Street<br>South Bend, IN 46613-2299<br>(219) 287-5941<br>www.wellscti.com | | | | X | | |
| Yamaichi Electronics Inc.<br>2235 Zanker Road<br>San Jose, CA 95131<br>(408) 456-0797<br>www.yeu.com | | X | X | X | X | |

## Web Sites for Heatsink Sources

Below is the list manufacturers' web pages offering heatsink solutions for Xilinx Package types. This summary does not imply an endorsement by Xilinx. Each user has the responsibility to evaluate and approve a particular heatsink solution provider.

Wakefield Thermal Solutions, Inc. — http://www.wakefield.com

AAVID Thermal Technologies — http://www.aavid.com

AAVID Thermalloy — http://www.thermalloy.com

Tyco Electronics — http://www.chipcoolers.com

Malico, Inc. — http://www.malico.com.tw

GlobalWin: http://www.globalwin.com.tw

Asia Vital Components Co., Ltd. — http://www.avc.com.tw

ALPHA — http://www.micforg.co.jp

Cofan USA — http://www.cofan-usa.com

## Web Sites for Interface Material Sources

Xilinx does not endorse these vendors nor their products. They are listed here for reference only. Any materials or services received from the vendors should be evaluated for compatibility with Xilinx components.

Power Devices — http://www.powerdevices.com

Chomerics — http://www.chomerics.com

Bergquist Company — http://www.bergquistcompany.com

AOS Thermal Compound — http://www.aosco.com

## Related Xilinx Web Sites and Links to Xilinx Packaging Application Notes

Package drawings,
http://www.xilinx.com/xlnx/xweb/xil_publications_index.jsp?category=Package+Drawings

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