Spartan-6 FPGA LX16 CES Errata

EN113 (v1.3) February 11, 2010 **Errata Notification**

Introduction

Thank you for participating in the Spartan®-6 FPGA Engineering Sample Program. As part of this program, we are pleased to provide to you engineering samples of the device listed in Table 1. Although Xilinx has made every effort to ensure the highest possible quality, this device is subject to the limitations described in the following errata.

Device

These errata apply to the Spartan-6 device shown in Table 1.

Table 1: **Device Affected by These Errata**

Device	JTAG ID (Revision Code)
XC6SLX16-2CSG324CES	1

Hardware Errata Details

This section provides a detailed description of each hardware issue known at the release time of this document.

Memory Controller Block (MCB)

MCB Calibration

In the device listed in Table 1, for designs using Calibrated Input Termination, use the following CSG324 pin locations for the RZQ reference resistor: MCB Bank 1 – pin M13, MCB Bank 3 – pin C2.

MCB and Suspend

In the device listed in Table 1, the MCB does not support the self-refresh mode of the external memory during FPGA Suspend.

MCB Address Bus Hold Time

In the device listed in Table 1, some bits of the MCB address bus (mcbx_dram_addr) can violate the input hold time (t_{IH}) specification of the memory device.

Work-around

See Answer Record 34089.

DCM Minimum Frequency

The Digital Clock Manager (DCM_SP or DCM_CLKGEN) minimum frequency does not meet the data sheet specifications in the device listed in Table 1. The following specifications deviate from the data sheet:

- CLKIN_FREQ_DLL Min: 50 MHz
- CLKOUT_FREQ_CLK0 Min: 50 MHz
- CLKOUT_FREQ_CLK90 Min: 50 MHz
- CLKOUT_FREQ_2X Min: 100 MHz
- CLKOUT_FREQ_DV Min: 3.125 MHz
- CLKIN_FREQ_FX Min: 1.6 MHz
- CLKOUT_FREQ_FX Min: 50 MHz
- CLKOUT_FREQ_FXDV: 1.6 MHz

BUFPLL LOCK Output

In the device listed in Table 1, the BUFPLL LOCK output might stay High when the PLL_BASE LOCKED signal is Low. As a result, the timing of the SERDESSTROBE signal might change after the PLL has been reset.

Work-around

Any application that performs a training, framing, or Bitslip function on the incoming data should be reinitialized following a PLL reset to ensure correct data reception.

Device DNA

Device DNA is not supported in the device listed in Table 1. Do not use this feature.

Block RAM Byte-Write Enable Hold Time

The block RAM byte-write enable input can have a positive hold time in the device listed in Table 1.

Work-around

Adding additional delay to the write enable input on the block RAM is recommended. Do not place the write-enable source in the CLB adjacent to the block RAM.

IOB DDR Mode

DDR mode is not supported in Banks 0 and 2 (top and bottom) in the device listed in Table 1.

Configuration Readback

Readback is not supported in the device listed in Table 1. Do not select the verify or readback options in the iMPACT tool or enable post-configuration CRC.

Operational Guidelines

Design Software Requirements

The device listed in Table 1, unless otherwise specified, requires the following Xilinx development software installation.

Speed specification v1.01 (or later), Xilinx® ISE® Design Suite 11.3, or later version of software.

Operating Conditions Required when Using I/O Delay Variable Mode

In the device listed in Table 1, when using I/O Delay Variable Mode, the operating conditions must be:

- V_{CCINT} = 1.20V to 1.26V
- Junction temperature (T_J) = 25°C to 85°C

The I/O delay variable mode (also known as I/O delay calibration and reset) is used when the IODELAY2 CAL or RST are used or when IODELAY2 IDELAY_TYPE attribute is set to VARIABLE_FROM_ZERO, VARIABLE_FROM_HALF_MAX, or DIFF_PHASE_DETECTOR.

Traceability

The XC6SLX16 listed in Table 1 is marked as shown in Figure 1.

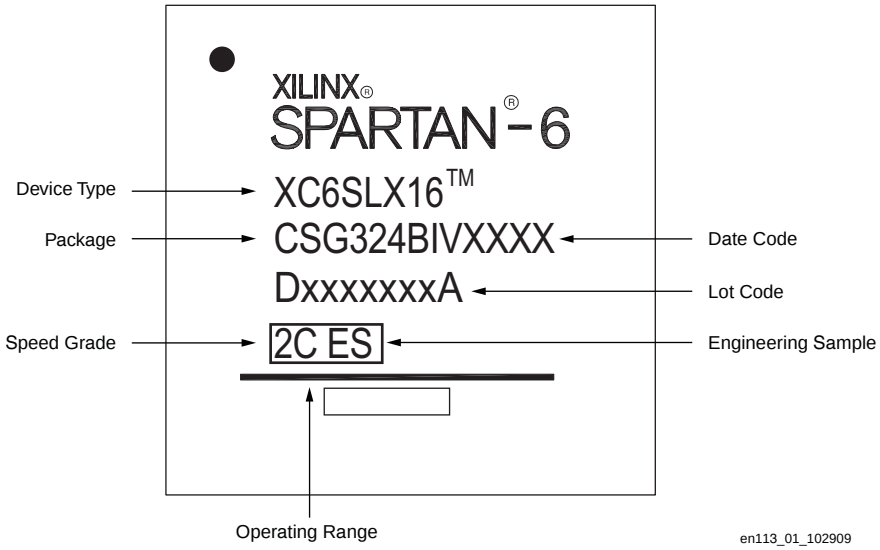

Figure 1: **XC6SLX16-2CSG324CES Marking**

Additional Questions or Clarifications

For additional questions regarding these errata, contact Xilinx Technical Support: http://www.xilinx.com/support/clearexpress/websupport.htm or your Xilinx Sales Representative: http://www.xilinx.com/company/contact.htm.

Revision History

Date	Version	Description
07/17/09	1.0	Initial Xilinx release.
09/10/09	1.1	Updated the Memory Controller Block (MCB) section and removed reference to software issues in Answer Record 33130. Removed MCB Auto-Precharge Instructions; this issue will be addressed in software.
10/29/09	1.2	Added MCB and Suspend. Updated Figure 1 marking.
02/11/10	1.3	Added MCB Address Bus Hold Time. Updated Design Software Requirements.

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