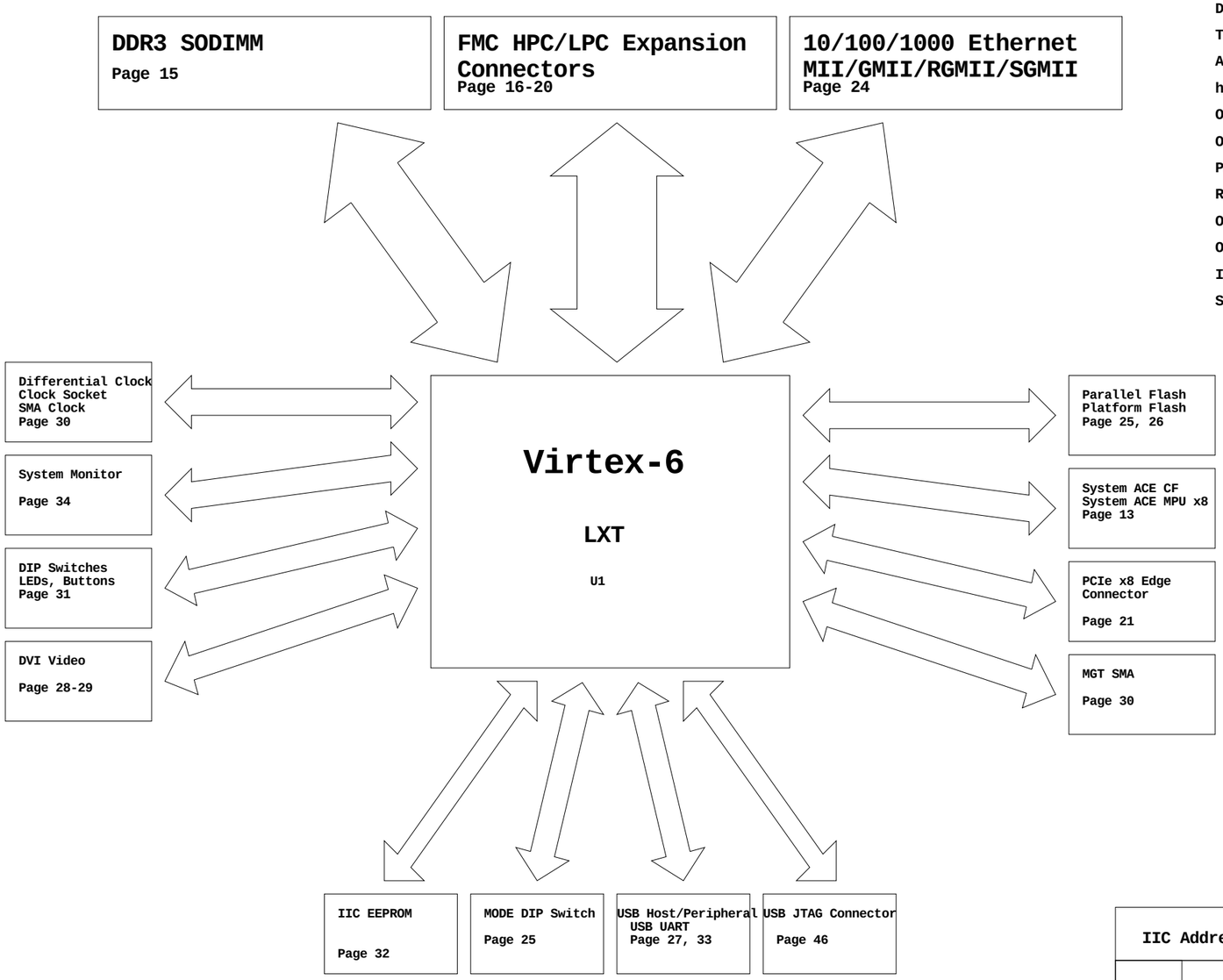
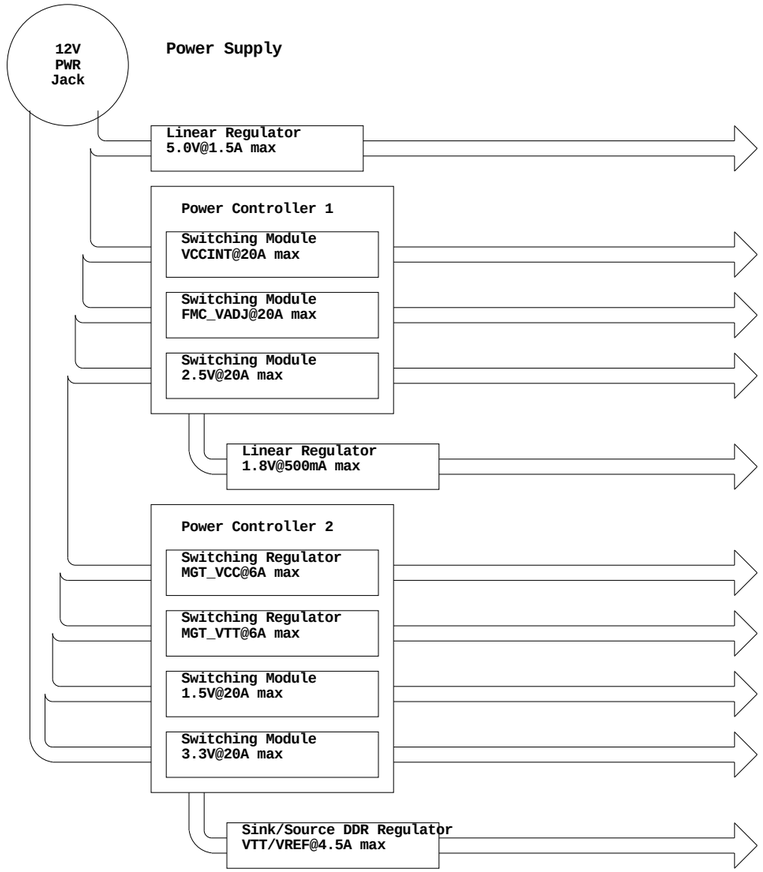
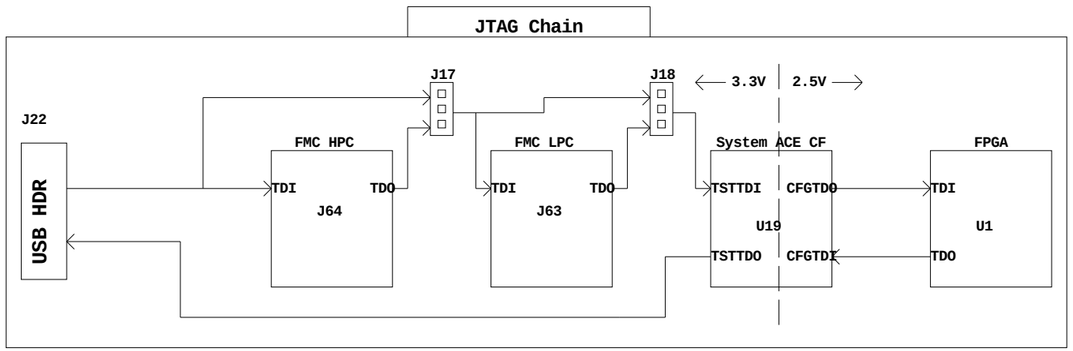


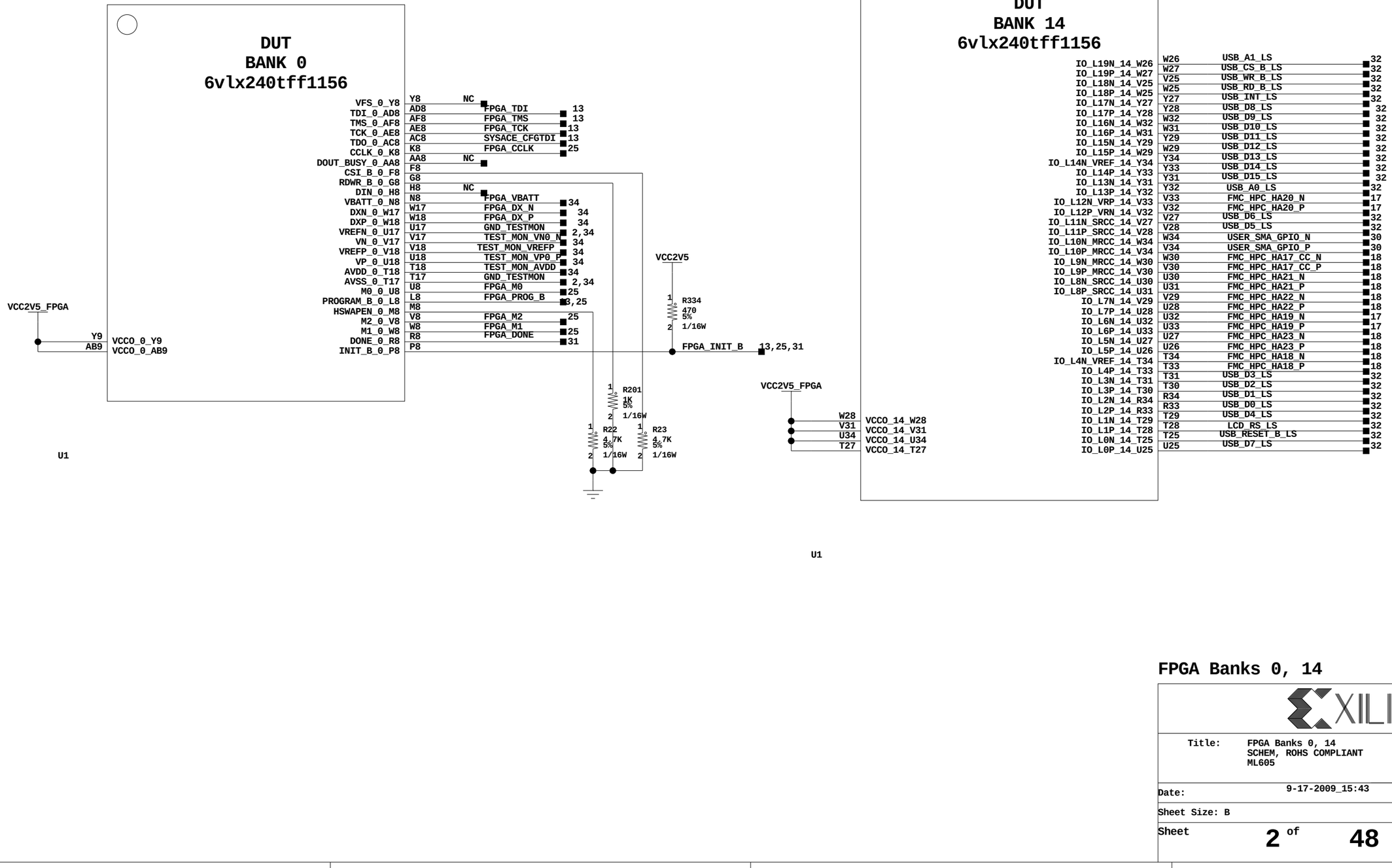




IIC Addressing	
U6	0b1010100
J63	0bXXXXX01
J64	0bXXXXX00
J1	0b0101011 0b0011011

XILINX

Title:	ML605 Block Diagram SCHEM, ROHS COMPLIANT ML605 EVALUATION PLATFORM	ASSY P/N: PCB P/N: SCH P/N:	0431540 1280479 0381311
Date:	9-17-2009_15:45	Ver:	D
Sheet Size: B		Rev:	04
Sheet	1 of 48	Drawn By	BF


DUT
BANK 0
6vlx240tff1156
VFS_0_Y8
TDI_0_AD8
TMS_0_AF8
TCK_0_AE8
TDO_0_AC8
CCLK_0_K8
DOUT_BUSY_0_AA8
CSI_B_0_F8
RDWR_B_0_G8
DIN_0_H8
VBATT_0_N8
DXN_0_W17
DXP_0_W18
VREFN_0_U17
VN_0_V17
VREFP_0_V18
VP_0_U18
AVDD_0_T18
AVSS_0_T17
M0_0_U8
PROGRAM_B_0_L8
HSWAPEN_0_M8
M2_0_V8
M1_0_W8
DONE_0_R8
INIT_B_0_P8
Y8 NC
AD8 FPGA_TDI 13
AF8 FPGA_TMS 13
AE8 FPGA_TCK 13
AC8 SYSACE_CFGTDI 13
K8 FPGA_CCLK 25
AA8 NC
F8
G8
H8 NC
N8 FPGA_VBATT
W17 FPGA_DX_N 34
W18 FPGA_DX_P 34
U17 GND_TESTMON 2,34
V17 TEST_MON_VN0_N 34
V18 TEST_MON_VREFP 34
U18 TEST_MON_VP0_P 34
T18 TEST_MON_AVDD 34
T17 GND_TESTMON 2,34
U8 FPGA_M0 25
L8 FPGA_PROG_B 3,25
M8
V8 FPGA_M2 25
W8 FPGA_M1 25
R8 FPGA_DONE 31
P8
VCC2V5_FPGA
Y9 VCCO_0_Y9
AB9 VCCO_0_AB9
VCC2V5
R334 470 5% 1/16W
FPGA_INIT_B 13,25,31
VCC2V5_FPGA
R201 1K 5% 1/16W
R22 4.7K 5% 1/16W
R23 4.7K 5% 1/16W
U1
DUT
BANK 14
6vlx240tff1156
IO_L19N_14_W26
IO_L19P_14_W27
IO_L18N_14_V25
IO_L18P_14_W25
IO_L17N_14_Y27
IO_L17P_14_Y28
IO_L16N_14_W32
IO_L16P_14_W31
IO_L15N_14_Y29
IO_L15P_14_W29
IO_L14N_VREF_14_Y34
IO_L14P_14_Y33
IO_L13N_14_Y31
IO_L13P_14_Y32
IO_L12N_VRP_14_V33
IO_L12P_VRN_14_V32
IO_L11N_SRCC_14_V27
IO_L11P_SRCC_14_V28
IO_L10N_MRCC_14_W34
IO_L10P_MRCC_14_V34
IO_L9N_MRCC_14_W30
IO_L9P_MRCC_14_V30
IO_L8N_SRCC_14_U30
IO_L8P_SRCC_14_U31
IO_L7N_14_V29
IO_L7P_14_U28
IO_L6N_14_U32
IO_L6P_14_U33
IO_L5N_14_U27
IO_L5P_14_U26
IO_L4N_VREF_14_T34
IO_L4P_14_T33
IO_L3N_14_T31
IO_L3P_14_T30
IO_L2N_14_R34
IO_L2P_14_R33
IO_L1N_14_T29
IO_L1P_14_T28
IO_L0N_14_T25
IO_L0P_14_U25
W26 USB_A1_LS 32
W27 USB_CS_B_LS 32
V25 USB_WR_B_LS 32
W25 USB_RD_B_LS 32
Y27 USB_INT_LS 32
Y28 USB_D8_LS 32
W32 USB_D9_LS 32
W31 USB_D10_LS 32
Y29 USB_D11_LS 32
W29 USB_D12_LS 32
Y34 USB_D13_LS 32
Y33 USB_D14_LS 32
Y31 USB_D15_LS 32
Y32 USB_A0_LS 32
V33 FMC_HPC_HA20_N 17
V32 FMC_HPC_HA20_P 17
V27 USB_D6_LS 32
V28 USB_D5_LS 32
W34 USER_SMA_GPIO_N 30
V34 USER_SMA_GPIO_P 30
W30 FMC_HPC_HA17_CC_N 18
V30 FMC_HPC_HA17_CC_P 18
U30 FMC_HPC_HA21_N 18
U31 FMC_HPC_HA21_P 18
V29 FMC_HPC_HA22_N 18
U28 FMC_HPC_HA22_P 18
U32 FMC_HPC_HA19_N 17
U33 FMC_HPC_HA19_P 17
U27 FMC_HPC_HA23_N 18
U26 FMC_HPC_HA23_P 18
T34 FMC_HPC_HA18_N 18
T33 FMC_HPC_HA18_P 18
T31 USB_D3_LS 32
T30 USB_D2_LS 32
R34 USB_D1_LS 32
R33 USB_D0_LS 32
T29 USB_D4_LS 32
T28 LCD_RS_LS 32
T25 USB_RESET_B_LS 32
U25 USB_D7_LS 32
VCC2V5_FPGA
W28 VCCO_14_W28
V31 VCCO_14_V31
U34 VCCO_14_U34
T27 VCCO_14_T27
U1
FPGA Banks 0, 14
XILINX
Title: FPGA Banks 0, 14
SCHEM, ROHS COMPLIANT
ML605
ASSY P/N: 0431540
PCB P/N: 1280479
SCH P/N: 0381311
Date: 9-17-2009_15:43
Ver: D
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DUT BANK 16 6vlx240tff1156

IO_L19N_16_J32	J32	FMC_LPC_LA03_N	20
IO_L19P_16_J31	J31	FMC_LPC_LA03_P	20
IO_L18N_16_L26	L26	FMC_LPC_LA09_N	20
IO_L18P_16_L25	L25	FMC_LPC_LA09_P	20
IO_L17N_16_H32	H32	FMC_LPC_LA07_N	20
IO_L17P_16_G32	G32	FMC_LPC_LA07_P	20
IO_L16N_16_J34	J34	FMC_LPC_LA06_N	20
IO_L16P_16_K33	K33	FMC_LPC_LA06_P	20
IO_L15N_16_D32	D32	FMC_LPC_LA11_N	20
IO_L15P_16_D31	D31	FMC_LPC_LA11_P	20
IO_L14N_VREF_16_H33	H33	FMC_LPC_LA05_N	20
IO_L14P_16_H34	H34	FMC_LPC_LA05_P	20
IO_L13N_16_K29	K29	FMC_LPC_LA08_N	20
IO_L13P_16_J30	J30	FMC_LPC_LA08_P	20
IO_L12N_VRP_16_F34	F34	VRP_16	3
IO_L12P_VRN_16_E34	E34	VRN_16	3
IO_L11N_SRCC_16_E31	E31	FMC_LPC_LA01_CC_N	20
IO_L11P_SRCC_16_F31	F31	FMC_LPC_LA01_CC_P	20
IO_L10N_MRCC_16_G33	G33	FMC_LPC_CLK1_M2C_N	20
IO_L10P_MRCC_16_F33	F33	FMC_LPC_CLK1_M2C_P	20
IO_L9N_MRCC_16_K27	K27	FMC_LPC_LA00_CC_N	20
IO_L9P_MRCC_16_K26	K26	FMC_LPC_LA00_CC_P	20
IO_L8N_SRCC_16_C34	C34	FMC_LPC_LA13_N	20
IO_L8P_SRCC_16_D34	D34	FMC_LPC_LA13_P	20
IO_L7N_16_J29	J29	FMC_LPC_LA04_N	20
IO_L7P_16_K28	K28	FMC_LPC_LA04_P	20
IO_L6N_16_B34	B34	FMC_LPC_LA14_N	20
IO_L6P_16_C33	C33	FMC_LPC_LA14_P	20
IO_L5N_16_H30	H30	FMC_LPC_LA02_N	20
IO_L5P_16_G31	G31	FMC_LPC_LA02_P	20
IO_L4N_VREF_16_B33	B33	FMC_LPC_LA16_N	20
IO_L4P_16_A33	A33	FMC_LPC_LA16_P	20
IO_L3N_16_G30	G30	FMC_LPC_LA10_N	20
IO_L3P_16_F30	F30	FMC_LPC_LA10_P	20
IO_L2N_16_E33	E33	FMC_LPC_LA12_N	20
IO_L2P_16_E32	E32	FMC_LPC_LA12_P	20
IO_L1N_16_J27	J27	FMC_HPC_PG_M2C_LS	32
IO_L1P_16_J26	J26	FLASH_WAIT	26
IO_L0N_16_B32	B32	FMC_LPC_LA15_N	20
IO_L0P_16_C32	C32	FMC_LPC_LA15_P	20

VCC2V5_FPGA

K25	VCCO_16_K25
J28	VCCO_16_J28
H31	VCCO_16_H31
G34	VCCO_16_G34
D33	VCCO_16_D33
A32	VCCO_16_A32

U1

VCC2V5

R351 49.9 1% 1/16W

3 VRN_16

3 VRP_16

R350 49.9 1% 1/16W

DUT BANK 15 6vlx240tff1156

IO_L19N_15_R29	R29	FMC_LPC_LA20_N	20
IO_L19P_15_P29	P29	FMC_LPC_LA20_P	20
IO_L18N_15_P34	P34	FMC_LPC_LA29_N	20
IO_L18P_15_N34	N34	FMC_LPC_LA29_P	20
IO_L17N_15_N30	N30	FMC_LPC_LA19_N	20
IO_L17P_15_M30	M30	FMC_LPC_LA19_P	20
IO_L16N_VRP_15_L34	L34	VRP_15	3
IO_L16P_VRN_15_K34	K34	VRN_15	3
IO_L15N_SM15N_15_T26	T26	FMC_LPC_LA21_N	20
IO_L15P_SM15P_15_R26	R26	FMC_LPC_LA21_P	20
IO_L14N_VREF_15_R32	R32	FMC_LPC_LA27_N	20
IO_L14P_15_R31	R31	FMC_LPC_LA27_P	20
IO_L13N_SM14N_15_R27	R27	FMC_LPC_LA23_N	20
IO_L13P_SM14P_15_R28	R28	FMC_LPC_LA23_P	20
IO_L12N_SM13N_15_P26	P26	VAUX_CURR_N	
IO_L12P_SM13P_15_P25	P25	VAUX_CURR_P	
IO_L11N_SRCC_15_L30	L30	FMC_LPC_LA18_CC_N	20
IO_L11P_SRCC_15_L29	L29	FMC_LPC_LA18_CC_P	20
IO_L10N_MRCC_15_M33	M33	FMC_LPC_LA28_N	20
IO_L10P_MRCC_15_N33	N33	FMC_LPC_LA28_P	20
IO_L9N_MRCC_15_N29	N29	FMC_LPC_LA17_CC_N	20
IO_L9P_MRCC_15_N28	N28	FMC_LPC_LA17_CC_P	20
IO_L8N_SRCC_15_P32	P32	FMC_LPC_LA24_N	20
IO_L8P_SRCC_15_N32	N32	FMC_LPC_LA24_P	20
IO_L7N_SM12N_15_M28	M28	VAUX_VOLT_N	
IO_L7P_SM12P_15_L28	L28	VAUX_VOLT_P	
IO_L6N_SM11N_15_M32	M32	FMC_LPC_LA26_N	20
IO_L6P_SM11P_15_L33	L33	FMC_LPC_LA26_P	20
IO_L5N_SM10N_15_P27	P27	FMC_LPC_LA22_N	20
IO_L5P_SM10P_15_N27	N27	FMC_LPC_LA22_P	20
IO_L4N_VREF_15_P30	P30	FMC_LPC_LA25_N	20
IO_L4P_15_P31	P31	FMC_LPC_LA25_P	20
IO_L3N_SM9N_15_M27	M27	FMC_LPC_LA30_N	20
IO_L3P_SM9P_15_M26	M26	FMC_LPC_LA30_P	20
IO_L2N_SM8N_15_K31	K31	FMC_LPC_LA33_N	20
IO_L2P_SM8P_15_K32	K32	FMC_LPC_LA33_P	20
IO_L1N_15_M25	M25	FMC_LPC_LA32_N	20
IO_L1P_15_N25	N25	FMC_LPC_LA32_P	20
IO_L0N_15_L31	L31	FMC_LPC_LA31_N	20
IO_L0P_15_M31	M31	FMC_LPC_LA31_P	20

VCC2V5_FPGA

R30	VCCO_15_R30
P33	VCCO_15_P33
N26	VCCO_15_N26
M29	VCCO_15_M29
L32	VCCO_15_L32

U1

VCC2V5

R348 49.9 1% 1/16W

3 VRN_15

3 VRP_15

R349 49.9 1% 1/16W

R373 1.00K 1% 1/16W — VAUX_COMMON_R 3,39

C384 0.01UF 16V X7R

R370 1.00K 1% 1/16W — VAUX_CURR_R 39

R371 1.00K 1% 1/16W — VAUX_VOLT_R 39

C385 0.01UF 16V X7R

R372 1.00K 1% 1/16W — VAUX_COMMON_R 3,39

Place above components near FPGA

FPGA Banks 15, 16

XILINX

Title:	FPGA Banks 15, 16 SCHEM, ROHS COMPLIANT ML605	ASSY P/N: PCB P/N: SCH P/N:	0431540 1280479 0381311
Date:	9-17-2009_15:43	Ver:	D
Sheet Size: B		Rev:	04
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DUT
BANK 34
6vlx240tff1156

IO_L19N_VRP_34_AP10	AP10	IIC_SDA_DVI	28,29
IO_L19P_VRN_34_AN10	AN10	IIC_SCL_DVI	28,29
IO_L18N_A16_34_AH8	AH8	FLASH_A16	25,26
IO_L18P_A17_34_AG8	AG8	FLASH_A17	25,26
IO_L17N_A18_34_AP9	AP9	FLASH_A18	25,26
IO_L17P_A19_34_AN9	AN9	FLASH_A19	25,26
IO_L16N_A20_34_AF10	AF10	FLASH_A20	25,26
IO_L16P_A21_34_AF9	AF9	FLASH_A21	25,26
IO_L15N_A22_34_AL9	AL9	FLASH_A22	25,26
IO_L15P_A23_34_AK9	AK9	IIC_SCL_MAIN_LS	32
IO_L14N_VREF_A24_34_AE9	AE9	IIC_SDA_MAIN_LS	32
IO_L14P_A25_34_AD9	AD9	FMC_LPC_PRSNT_M2C_L	20
IO_L13N_A00_D16_34_AL8	AL8	FLASH_A0	25,26
IO_L13P_A01_D17_34_AK8	AK8	FLASH_A1	25,26
IO_L12N_A02_D18_34_AC9	AC9	FLASH_A2	25,26
IO_L12P_A03_D19_34_AD10	AD10	FLASH_A3	25,26
IO_L11N_SRCC_34_AJ9	AJ9	PMBUS_CTRL_LS	32
IO_L11P_SRCC_34_AH9	AH9	PMBUS_ALERT_LS	32
IO_L10N_MRCC_34_AB10	AB10	PMBUS_DATA_LS	32
IO_L10P_MRCC_34_AC10	AC10	PMBUS_CLK_LS	32
IO_L9N_MRCC_34_M10	M10	SM_FAN_TACH	39
IO_L9P_MRCC_34_L10	L10	SM_FAN_PWM	39
IO_L8N_SRCC_34_K9	K9	DVI_GPIO1_FMC_C2M_PG_LS	32
IO_L8P_SRCC_34_L9	L9	SYSACE_MPIRQ	13
IO_L7N_A04_D20_34_C8	C8	FLASH_A4	25,26
IO_L7P_A05_D21_34_B8	B8	FLASH_A5	25,26
IO_L6N_A06_D22_34_E9	E9	FLASH_A6	25,26
IO_L6P_A07_D23_34_E8	E8	FLASH_A7	25,26
IO_L5N_A08_D24_34_A8	A8	FLASH_A8	25,26
IO_L5P_A09_D25_34_A9	A9	FLASH_A9	25,26
IO_L4N_VREF_A10_D26_34_D9	D9	FLASH_A10	25,26
IO_L4P_A11_D27_34_C9	C9	FLASH_A11	25,26
IO_L3N_A12_D28_34_D10	D10	FLASH_A12	25,26
IO_L3P_A13_D29_34_C10	C10	FLASH_A13	25,26
IO_L2N_A14_D30_34_F10	F10	FLASH_A14	25,26
IO_L2P_A15_D31_34_F9	F9	FLASH_A15	25,26
IO_L1N_GC_34_B10	B10	FMC_LPC_CLK0_M2C_N	20
IO_L1P_GC_34_A10	A10	FMC_LPC_CLK0_M2C_P	20
IO_L0N_GC_34_H9	H9	SYSCLK_N	30
IO_L0P_GC_34_J9	J9	SYSCLK_P	30

VCC2V5_FPGA

M9	VCCO_34_M9
E10	VCCO_34_E10
B9	VCCO_34_B9
AM9	VCCO_34_AM9
AJ8	VCCO_34_AJ8
AE10	VCCO_34_AE10

U1

DUT
BANK 24
6vlx240tff1156

IO_L19N_24_AD22	AD22	PCIE_WAKE_B_LS	32
IO_L19P_24_AC22	AC22	GPIO_LED_0	31
IO_L18N_24_AC24	AC24	GPIO_LED_1	31
IO_L18P_24_AC23	AC23	PLATFLASH_L_B	25
IO_L17N_VRP_24_AE22	AE22	GPIO_LED_2	31
IO_L17P_VRN_24_AE23	AE23	GPIO_LED_3	31
IO_L16N_CSO_B_24_AB23	AB23	GPIO_LED_4	31
IO_L16P_RS0_24_AA23	AA23	FLASH_A23	25,26
IO_L15N_RS1_24_AG23	AG23	GPIO_LED_5	31
IO_L15P_FWE_B_24_AF23	AF23	FPGA_FWE_B	25,26
IO_L14N_VREF_FOE_B_MOSI_24_AA24	AA24	FPGA_FOE_B	25,26
IO_L14P_FCS_B_24_Y24	Y24	FPGA_FCS_B	25
IO_L13N_D0_FS0_24_AF24	AF24	FLASH_D0	25,26
IO_L13P_D1_FS1_24_AF25	AF25	FLASH_D1	25,26
IO_L12N_D2_FS2_24_W24	W24	FLASH_D2	25,26
IO_L12P_D3_24_V24	V24	FLASH_D3	25,26
IO_L11N_SRCC_24_AE24	AE24	GPIO_LED_6	31
IO_L11P_SRCC_24_AD24	AD24	GPIO_LED_7	31
IO_L10N_MRCC_24_V23	V23	SFP_LOS	23
IO_L10P_MRCC_24_U23	U23	USER_CLOCK	30
IO_L9N_MRCC_24_J24	J24	USB_1_TX	33
IO_L9P_MRCC_24_J25	J25	USB_1_RX	33
IO_L8N_SRCC_24_T23	T23	USB_1_RTS	33
IO_L8P_SRCC_24_T24	T24	USB_1_CTS	33
IO_L7N_D4_24_H24	H24	FLASH_D4	25,26
IO_L7P_D5_24_H25	H25	FLASH_D5	25,26
IO_L6N_D6_24_P24	P24	FLASH_D6	25,26
IO_L6P_D7_24_R24	R24	FLASH_D7	25,26
IO_L5N_D8_24_G23	G23	FLASH_D8	25,26
IO_L5P_D9_24_H23	H23	FLASH_D9	25,26
IO_L4N_VREF_D10_24_N24	N24	FLASH_D10	25,26
IO_L4P_D11_24_N23	N23	FLASH_D11	25,26
IO_L3N_D12_24_F23	F23	FLASH_D12	25,26
IO_L3P_D13_24_F24	F24	FLASH_D13	25,26
IO_L2N_D14_24_L24	L24	FLASH_D14	25,26
IO_L2P_D15_24_M23	M23	FLASH_D15	25,26
IO_L1N_GC_24_K23	K23	FMC_HPC_CLK0_M2C_N	18
IO_L1P_GC_24_K24	K24	FMC_HPC_CLK0_M2C_P	18
IO_L0N_GC_24_M22	M22	USER_SMA_CLOCK_N	30
IO_L0P_GC_24_L23	L23	USER_SMA_CLOCK_P	30

VCC2V5_FPGA

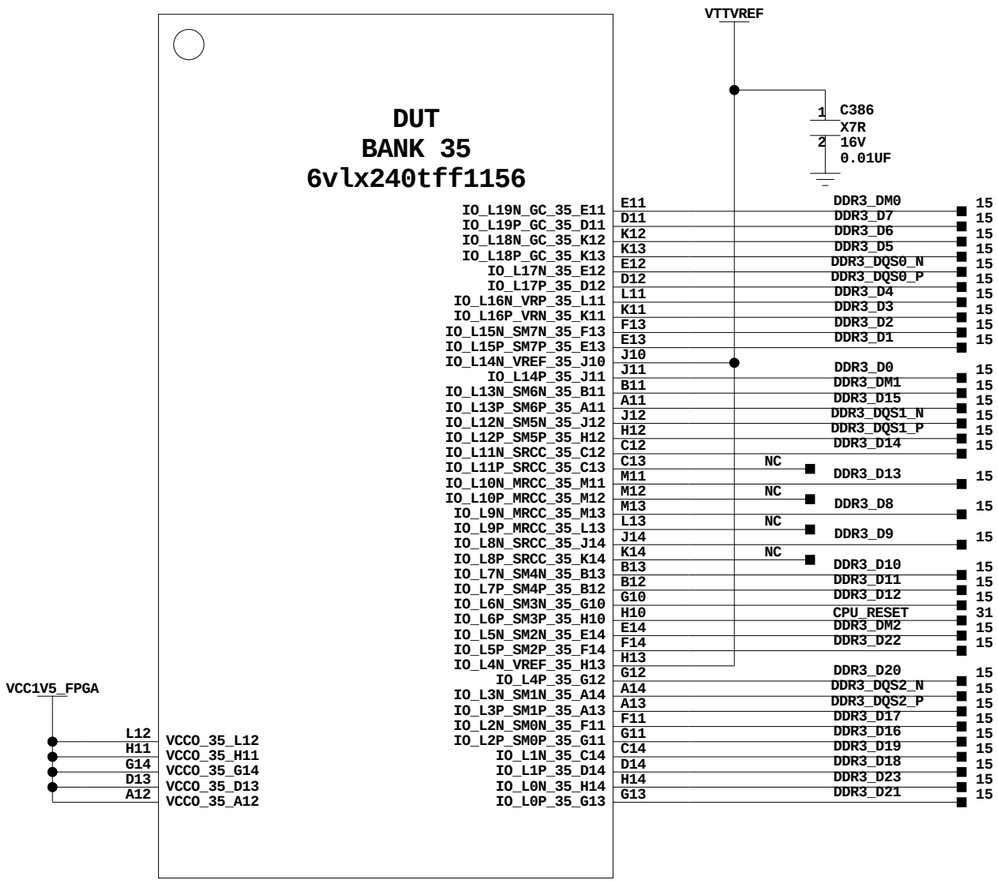
Y25	VCCO_24_Y25
U24	VCCO_24_U24
L22	VCCO_24_L22
G24	VCCO_24_G24
AG24	VCCO_24_AG24
AD23	VCCO_24_AD23

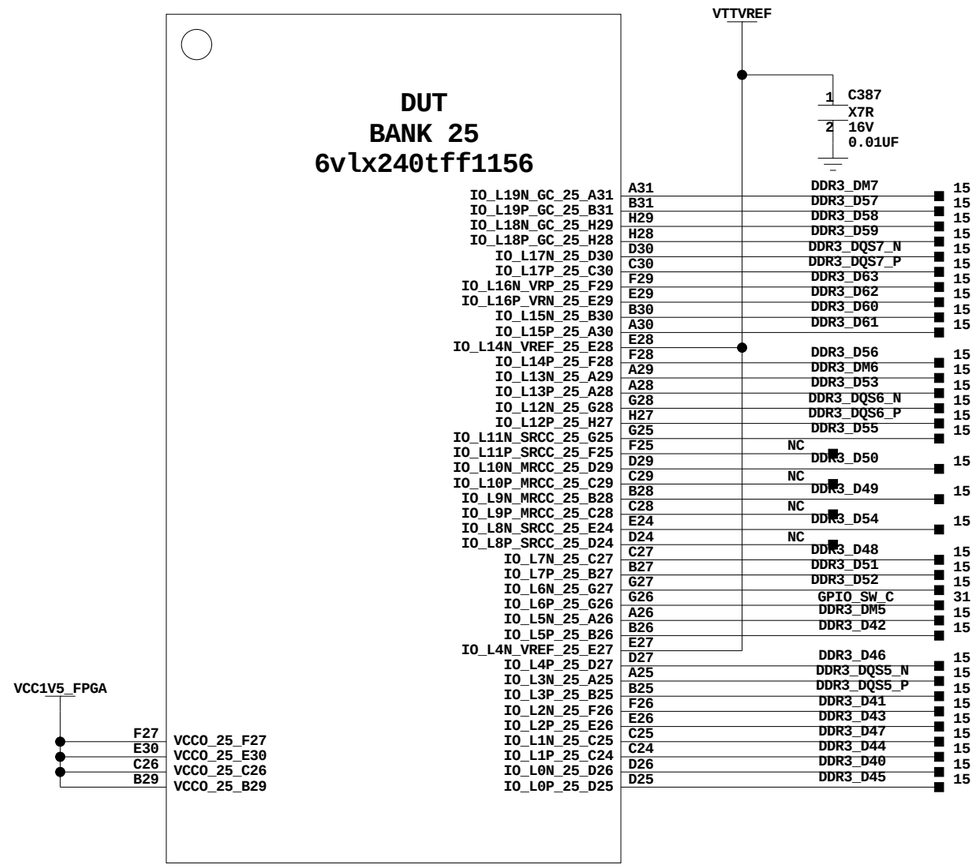
U1

FPGA Banks 24, 34

XILINX

Title:	FPGA Banks 24, 34 SCHEM, ROHS COMPLIANT ML605	ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311	
Date:	9-17-2009_15:43	Ver:	D
Sheet Size: B		Rev:	04
Sheet	4 of 48	Drawn By	BF

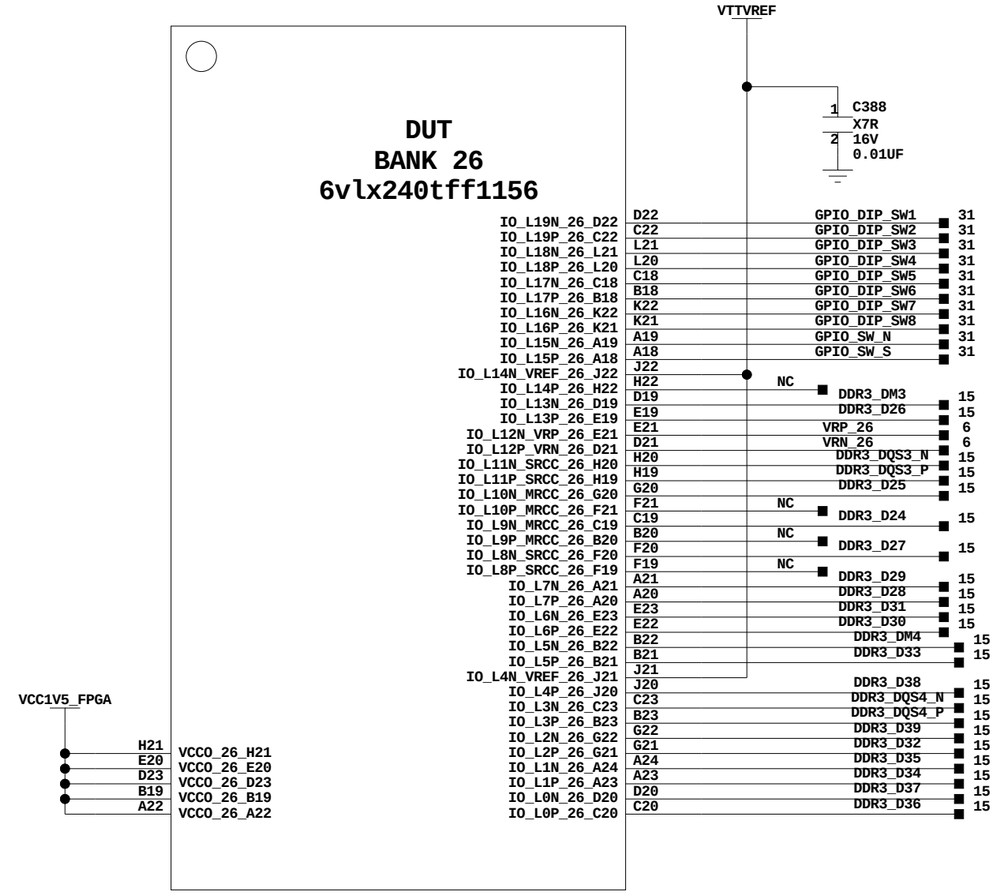


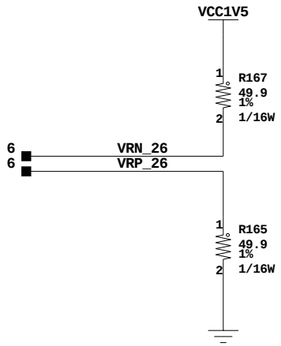


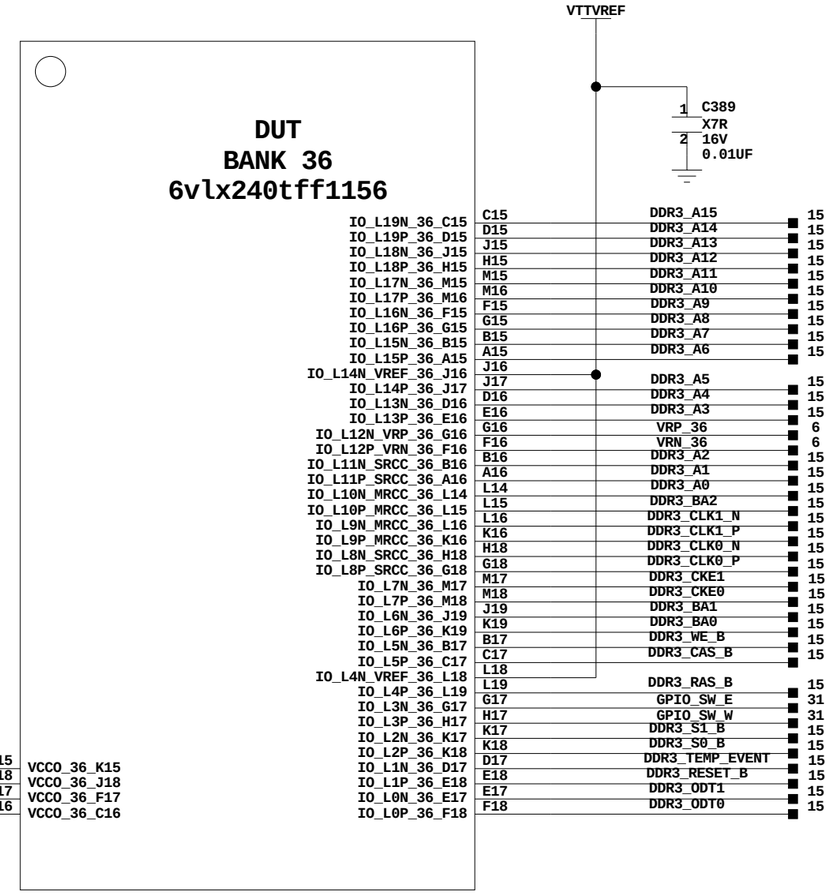
FPGA Banks 25, 35

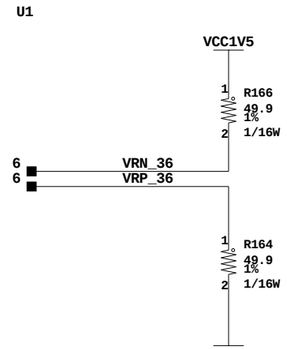
XILINX

Title:	FPGA Banks 25, 35 SCHEM, ROHS COMPLIANT ML605	ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311	
Date:	9-17-2009_15:43	Ver:	D
Sheet Size: B		Rev:	04
Sheet	5 of 48	Drawn By	BF









FPGA Banks 26, 36

XILINX

Title:	FPGA Banks 26, 36 SCHEM, ROHS COMPLIANT ML605	ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311	
Date:	9-17-2009_15:43	Ver:	D
Sheet Size: B		Rev:	04
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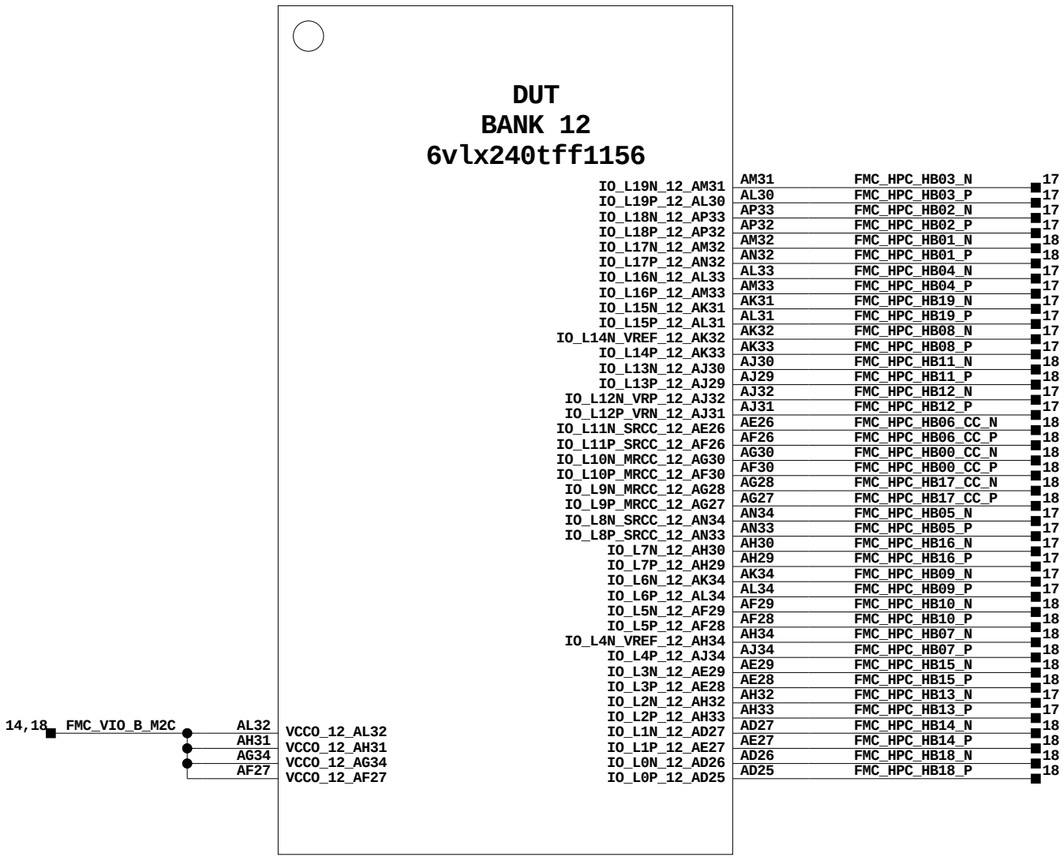
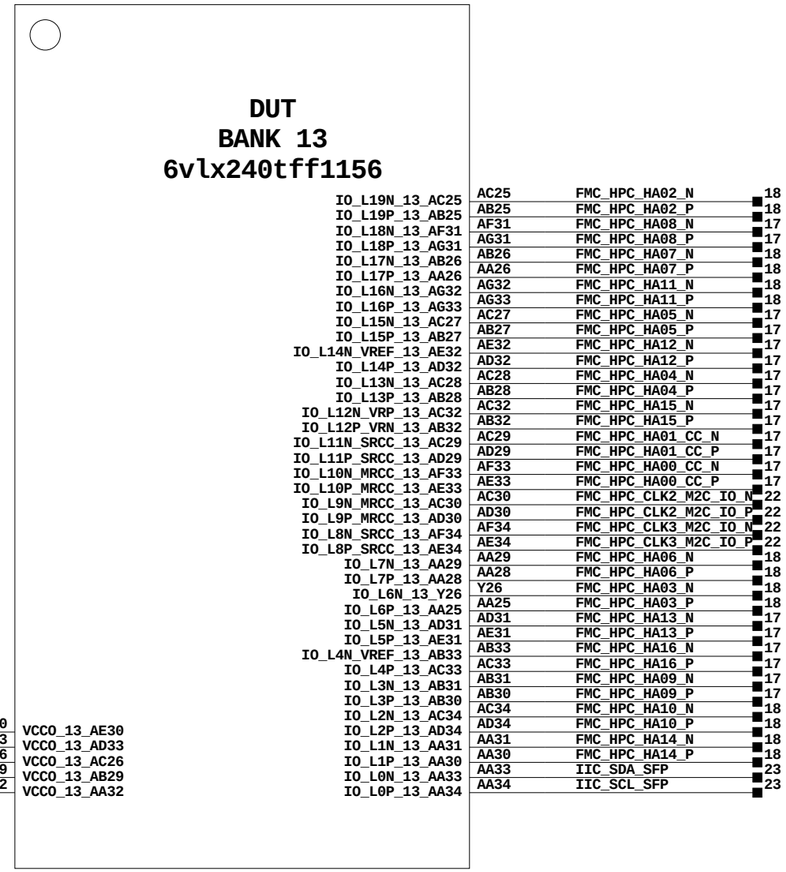
LX240T ONLY



LX240T ONLY



FPGA Banks 12, 13

XILINX

Title:	FPGA Banks 12, 13 SCHEM, ROHS COMPLIANT ML605	ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311	
Date:	9-17-2009_15:43	Ver:	D
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LX240T ONLY

DUT
BANK 22
6vlx240tff1156

IO_L19N_22_AN23	AN23	FMC_HPC_LA16_N	17
IO_L19P_22_AP22	AP22	FMC_HPC_LA16_P	17
IO_L18N_22_AG21	AG21	FMC_HPC_LA06_N	16
IO_L18P_22_AG20	AG20	FMC_HPC_LA06_P	16
IO_L17N_22_AN22	AN22	FMC_HPC_LA11_N	18
IO_L17P_22_AM22	AM22	FMC_HPC_LA11_P	18
IO_L16N_22_AJ21	AJ21	FMC_HPC_LA07_N	18
IO_L16P_22_AK21	AK21	FMC_HPC_LA07_P	18
IO_L15N_22_AL23	AL23	FMC_HPC_LA15_N	18
IO_L15P_22_AM23	AM23	FMC_HPC_LA15_P	18
IO_L14N_VREF_22_AD19	AD19	FMC_HPC_LA03_N	17
IO_L14P_22_AC19	AC19	FMC_HPC_LA03_P	17
IO_L13N_22_AL21	AL21	FMC_HPC_LA12_N	17
IO_L13P_22_AM21	AM21	FMC_HPC_LA12_P	17
IO_L12N_VRP_22_AH20	AH20	VRP_22	8
IO_L12P_VRN_22_AJ20	AJ20	VRN_22	8
IO_L11N_SRCC_22_AF21	AF21	FMC_HPC_LA00_CC_N	17
IO_L11P_SRCC_22_AF20	AF20	FMC_HPC_LA00_CC_P	17
IO_L10N_MRCC_22_AL19	AL19	FMC_HPC_LA01_CC_N	16
IO_L10P_MRCC_22_AK19	AK19	FMC_HPC_LA01_CC_P	16
IO_L9N_MRCC_22_AP21	AP21	FMC_HPC_CLK1_M2C_N	17
IO_L9P_MRCC_22_AP20	AP20	FMC_HPC_CLK1_M2C_P	17
IO_L8N_SRCC_22_AE19	AE19	FMC_HPC_LA04_N	18
IO_L8P_SRCC_22_AF19	AF19	FMC_HPC_LA04_P	18
IO_L7N_22_AL20	AL20	FMC_HPC_LA10_N	16
IO_L7P_22_AM20	AM20	FMC_HPC_LA10_P	16
IO_L6N_22_AD20	AD20	FMC_HPC_LA02_N	18
IO_L6P_22_AC20	AC20	FMC_HPC_LA02_P	18
IO_L5N_22_AN20	AN20	FMC_HPC_LA14_N	16
IO_L5P_22_AN19	AN19	FMC_HPC_LA14_P	16
IO_L4N_VREF_22_AJ22	AJ22	FMC_HPC_LA08_N	17
IO_L4P_22_AK22	AK22	FMC_HPC_LA08_P	17
IO_L3N_22_AN18	AN18	FMC_HPC_LA13_N	16
IO_L3P_22_AP19	AP19	FMC_HPC_LA13_P	16
IO_L2N_22_AH22	AH22	FMC_HPC_LA05_N	16
IO_L2P_22_AG22	AG22	FMC_HPC_LA05_P	16
IO_L1N_22_AL18	AL18	FMC_HPC_LA09_N	16
IO_L1P_22_AM18	AM18	FMC_HPC_LA09_P	16
IO_L0N_22_AD21	AD21	GPIO_LED_W	31
IO_L0P_22_AE21	AE21	GPIO_LED_E	31

VCC2V5_FPGA

AP23	VCCO_22_AP23
AM19	VCCO_22_AM19
AL22	VCCO_22_AL22
AH21	VCCO_22_AH21
AE20	VCCO_22_AE20

U1

VCC2V5

R356 49.9 1% 1/16W

8 VRN_22

8 VRP_22

R357 49.9 1% 1/16W

LX240T ONLY

DUT
BANK 23
6vlx240tff1156

IO_L19N_23_AP24	AP24	GPIO_LED_C	31
IO_L19P_23_AP25	AP25	FMC_HPC_PRSNT_M2C_L	18
IO_L18N_23_AL24	AL24	FMC_HPC_LA20_N	17
IO_L18P_23_AK23	AK23	FMC_HPC_LA20_P	17
IO_L17N_23_AN24	AN24	FMC_HPC_LA19_N	18
IO_L17P_23_AN25	AN25	FMC_HPC_LA19_P	18
IO_L16N_23_AL25	AL25	FMC_HPC_LA26_N	16
IO_L16P_23_AM25	AM25	FMC_HPC_LA26_P	16
IO_L15N_23_AP26	AP26	FMC_HPC_LA22_N	17
IO_L15P_23_AP27	AP27	FMC_HPC_LA22_P	17
IO_L14N_VREF_23_AK24	AK24	FMC_HPC_LA30_N	18
IO_L14P_23_AJ24	AJ24	FMC_HPC_LA30_P	18
IO_L13N_23_AM26	AM26	FMC_HPC_LA23_N	16
IO_L13P_23_AL26	AL26	FMC_HPC_LA23_P	16
IO_L12N_VRP_23_AJ26	AJ26	VRP_23	8
IO_L12P_VRN_23_AK26	AK26	VRN_23	8
IO_L11N_SRCC_23_AH24	AH24	FMC_HPC_LA33_N	17
IO_L11P_SRCC_23_AH23	AH23	FMC_HPC_LA33_P	17
IO_L10N_MRCC_23_AJ27	AJ27	FMC_HPC_LA28_N	18
IO_L10P_MRCC_23_AK27	AK27	FMC_HPC_LA28_P	18
IO_L9N_MRCC_23_AM27	AM27	FMC_HPC_LA17_CC_N	16
IO_L9P_MRCC_23_AN27	AN27	FMC_HPC_LA17_CC_P	16
IO_L8N_SRCC_23_AJ25	AJ25	FMC_HPC_LA18_CC_N	16
IO_L8P_SRCC_23_AH25	AH25	FMC_HPC_LA18_CC_P	16
IO_L7N_23_AM28	AM28	FMC_HPC_LA25_N	17
IO_L7P_23_AN28	AN28	FMC_HPC_LA25_P	17
IO_L6N_23_AK28	AK28	FMC_HPC_LA29_N	17
IO_L6P_23_AL28	AL28	FMC_HPC_LA29_P	17
IO_L5N_23_AP29	AP29	FMC_HPC_LA21_N	18
IO_L5P_23_AN29	AN29	FMC_HPC_LA21_P	18
IO_L4N_VREF_23_AK29	AK29	FMC_HPC_LA31_N	17
IO_L4P_23_AL29	AL29	FMC_HPC_LA31_P	17
IO_L3N_23_AP31	AP31	FMC_HPC_LA27_N	16
IO_L3P_23_AP30	AP30	FMC_HPC_LA27_P	16
IO_L2N_23_AG26	AG26	FMC_HPC_LA32_N	18
IO_L2P_23_AG25	AG25	FMC_HPC_LA32_P	18
IO_L1N_23_AM30	AM30	FMC_HPC_LA24_N	18
IO_L1P_23_AN30	AN30	FMC_HPC_LA24_P	18
IO_L0N_23_AH28	AH28	GPIO_LED_S	31
IO_L0P_23_AH27	AH27	GPIO_LED_N	31

VCC2V5_FPGA

AN26	VCCO_23_AN26
AM29	VCCO_23_AM29
AK25	VCCO_23_AK25
AJ28	VCCO_23_AJ28

U1

VCC2V5

R354 49.9 1% 1/16W

8 VRN_23

8 VRP_23

R355 49.9 1% 1/16W

FPGA Banks 22, 23

XILINX

Title:	FPGA Banks 22, 23 SCHEM, ROHS COMPLIANT ML605	ASSY P/N: PCB P/N: SCH P/N:	0431540 1280479 0381311
Date:	9-17-2009_15:43	Ver:	D
Sheet Size: B		Rev:	04
Sheet	8 of 48	Drawn By	BF

LX240T ONLY

DUT
BANK 32
6vlx240tff1156

IO_L19N_32_AK16	AK16	DVI_D11	29
IO_L19P_32_AL16	AL16	DVI_D10	29
IO_L18N_32_AF18	AF18	DVI_D9	29
IO_L18P_32_AE18	AE18	DVI_D8	29
IO_L17N_32_AK17	AK17	DVI_D7	29
IO_L17P_32_AK18	AK18	DVI_D6	29
IO_L16N_32_AE17	AE17	DVI_D5	29
IO_L16P_32_AD17	AD17	DVI_D4	29
IO_L15N_32_AM16	AM16	DVI_D3	29
IO_L15P_32_AM17	AM17	DVI_D2	29
IO_L14N_VREF_32_AH19	AH19	DVI_D1	29
IO_L14P_32_AJ19	AJ19	DVI_D0	29
IO_L13N_32_AP17	AP17	DVI_RESET_B_LS	32
IO_L13P_32_AN17	AN17	DVI_H	29
IO_L12N_VRP_32_AG18	AG18	VRP_32	9
IO_L12P_VRN_32_AH18	AH18	VRN_32	9
IO_L11N_SRCC_32_AC17	AC17	DVI_XCLK_N	29
IO_L11P_SRCC_32_AC18	AC18	DVI_XCLK_P	29
IO_L10N_MRCC_32_AD16	AD16	DVI_DE	29
IO_L10P_MRCC_32_AE16	AE16	CLK_33MHZ_SYSACE	13
IO_L9N_MRCC_32_AD15	AD15	DVI_V	29
IO_L9P_MRCC_32_AC15	AC15	SYSACE_MPA00	13
IO_L8N_SRCC_32_AG17	AG17	SYSACE_MPA02	13
IO_L8P_SRCC_32_AH17	AH17	SYSACE_MPA03	13
IO_L7N_32_AP15	AP15	SYSACE_MPA01	13
IO_L7P_32_AP16	AP16	SYSACE_D3	13
IO_L6N_32_AJ16	AJ16	SYSACE_D2	13
IO_L6P_32_AJ17	AJ17	SYSACE_D1	13
IO_L5N_32_AM15	AM15	SYSACE_D0	13
IO_L5P_32_AN15	AN15	SYSACE_D7	13
IO_L4N_VREF_32_AF16	AF16	SYSACE_D6	13
IO_L4P_32_AG16	AG16	SYSACE_D4	13
IO_L3N_32_AL14	AL14	SYSACE_MPWE	13
IO_L3P_32_AL15	AL15	SYSACE_MPOE	13
IO_L2N_32_AH15	AH15	SYSACE_D5	13
IO_L2P_32_AJ15	AJ15	SYSACE_MPBRDY	13
IO_L1N_32_AJ14	AJ14	SYSACE_MPCE	13
IO_L1P_32_AK14	AK14	SYSACE_MPA06	13
IO_L0N_32_AF15	AF15	SYSACE_MPA05	13
IO_L0P_32_AG15	AG15	SYSACE_MPA04	13

VCC2V5_FPGA

AN16	VCCO_32_AN16
AK15	VCCO_32_AK15
AJ18	VCCO_32_AJ18
AF17	VCCO_32_AF17
AC16	VCCO_32_AC16

U1

VCC2V5

R169 1 2 49.9 1% 1/16W

R168 1 2 49.9 1% 1/16W

9	VRN_32
9	VRP_32

LX240T ONLY

DUT
BANK 33
6vlx240tff1156

IO_L19N_33_AN14	AN14	PHY_MDIO	24
IO_L19P_33_AP14	AP14	PHY_MDC	24
IO_L18N_33_AH14	AH14	PHY_INT	24
IO_L18P_33_AH13	AH13	PHY_RESET	24
IO_L17N_33_AL13	AL13	PHY_CRS	24
IO_L17P_33_AK13	AK13	PHY_COL	24
IO_L16N_33_AH12	AH12	PHY_TXC_GTXCLK	24
IO_L16P_33_AG12	AG12	PHY_RXER	24
IO_L15N_33_AM13	AM13	PHY_RXCTL_RXDV	24
IO_L15P_33_AN13	AN13	PHY_RXD0	24
IO_L14N_VREF_33_AF14	AF14	PHY_RXD1	24
IO_L14P_33_AE14	AE14	PHY_RXD2	24
IO_L13N_33_AN12	AN12	PHY_RXD3	24
IO_L13P_33_AM12	AM12	PHY_RXD4	24
IO_L12N_VRP_33_AG13	AG13	FMC_LPC_IIC_SDA_LS	32
IO_L12P_VRN_33_AF13	AF13	FMC_LPC_IIC_SCL_LS	32
IO_L11N_SRCC_33_AP12	AP12	SFP_TX_DISABLE_FPGA	23
IO_L11P_SRCC_33_AP11	AP11	PHY_RXCLK	24
IO_L10N_MRCC_33_AD11	AD11	PHY_RXD5	24
IO_L10P_MRCC_33_AD12	AD12	PHY_TXCLK	24
IO_L9N_MRCC_33_AC12	AC12	PHY_RXD6	24
IO_L9P_MRCC_33_AC13	AC13	PHY_RXD7	24
IO_L8N_SRCC_33_AH10	AH10	PHY_TXER	24
IO_L8P_SRCC_33_AJ10	AJ10	PHY_TXCTL_TXEN	24
IO_L7N_33_AM11	AM11	PHY_TXD0	24
IO_L7P_33_AL11	AL11	PHY_TXD1	24
IO_L6N_33_AG10	AG10	PHY_TXD2	24
IO_L6P_33_AG11	AG11	PHY_TXD3	24
IO_L5N_33_AL10	AL10	PHY_TXD4	24
IO_L5P_33_AM10	AM10	PHY_TXD5	24
IO_L4N_VREF_33_AE11	AE11	PHY_TXD6	24
IO_L4P_33_AF11	AF11	PHY_TXD7	24
IO_L3N_33_AJ12	AJ12	P30_CS_SEL	25
IO_L3P_33_AK12	AK12	LCD_E_LS	32
IO_L2N_33_AC14	AC14	LCD_RW_LS	32
IO_L2P_33_AD14	AD14	LCD_DB4_LS	32
IO_L1N_33_AK11	AK11	LCD_DB5_LS	32
IO_L1P_33_AJ11	AJ11	LCD_DB6_LS	32
IO_L0N_33_AE12	AE12	LCD_DB7_LS	32
IO_L0P_33_AE13	AE13	PCIE_PERST_B_LS	32

VCC2V5_FPGA

AP13	VCCO_33_AP13
AL12	VCCO_33_AL12
AH11	VCCO_33_AH11
AG14	VCCO_33_AG14
AD13	VCCO_33_AD13

U1

FPGA Banks 32, 33

XILINX

Title:	FPGA Banks 32, 33 SCHEM, ROHS COMPLIANT ML605	ASSY P/N: PCB P/N: SCH P/N:	0431540 1280479 0381311
Date:	9-17-2009_15:42	Ver:	D
Sheet Size: B		Rev:	04
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LX240T ONLY

DUT
BANK 112
6vlx240tff1156

MGTTXP0_112_AP1	AP1	FMC_HPC_DP7_C2M_P	16
MGTTXN0_112_AP2	AP2	FMC_HPC_DP7_C2M_N	16
MGTRXP0_112_AP5	AP5	FMC_HPC_DP7_M2C_P	16
MGTRXN0_112_AP6	AP6	FMC_HPC_DP7_M2C_N	16
MGTTXP1_112_AN3	AN3	FMC_HPC_DP6_C2M_P	16
MGTTXN1_112_AN4	AN4	FMC_HPC_DP6_C2M_N	16
MGTRXP1_112_AM5	AM5	FMC_HPC_DP6_M2C_P	16
MGTRXN1_112_AM6	AM6	FMC_HPC_DP6_M2C_N	16
MGTTXP2_112_AM1	AM1	FMC_HPC_DP5_C2M_P	16
MGTTXN2_112_AM2	AM2	FMC_HPC_DP5_C2M_N	16
MGTRXP2_112_AL3	AL3	FMC_HPC_DP5_M2C_P	16
MGTRXN2_112_AL4	AL4	FMC_HPC_DP5_M2C_N	16
MGTTXP3_112_AK1	AK1	FMC_HPC_DP4_C2M_P	16
MGTTXN3_112_AK2	AK2	FMC_HPC_DP4_C2M_N	16
MGTRXP3_112_AJ3	AJ3	FMC_HPC_DP4_M2C_P	16
MGTRXN3_112_AJ4	AJ4	FMC_HPC_DP4_M2C_N	16
MGTREFCLK0P_112_AK6	AK6	FMC_HPC_GBTCLK1_M2C_C_P	10
MGTREFCLK0N_112_AK5	AK5	FMC_HPC_GBTCLK1_M2C_C_N	10
MGTREFCLK1P_112_AH6	AH6	FMC_HPC_CLK3_M2C_MGT_P	10
MGTREFCLK1N_112_AH5	AH5	FMC_HPC_CLK3_M2C_MGT_N	10

DUT
BANK 114
6vlx240tff1156

MGTTXP0_114_Y1	Y1	PCIE_TX7_P	21
MGTTXN0_114_Y2	Y2	PCIE_TX7_N	21
MGTRXP0_114_AA3	AA3	PCIE_RX7_P	21
MGTRXN0_114_AA4	AA4	PCIE_RX7_N	21
MGTTXP1_114_V1	V1	PCIE_TX6_P	21
MGTTXN1_114_V2	V2	PCIE_TX6_N	21
MGTRXP1_114_W3	W3	PCIE_RX6_P	21
MGTRXN1_114_W4	W4	PCIE_RX6_N	21
MGTTXP2_114_T1	T1	PCIE_TX5_P	21
MGTTXN2_114_T2	T2	PCIE_TX5_N	21
MGTRXP2_114_U3	U3	PCIE_RX5_P	21
MGTRXN2_114_U4	U4	PCIE_RX5_N	21
MGTTXP3_114_P1	P1	PCIE_TX4_P	21
MGTTXN3_114_P2	P2	PCIE_TX4_N	21
MGTRXP3_114_R3	R3	PCIE_RX4_P	21
MGTRXN3_114_R4	R4	PCIE_RX4_N	21
MGTREFCLK0P_114_V6	V6	PCIE_250M_MGT1_P	22
MGTREFCLK0N_114_V5	V5	PCIE_250M_MGT1_N	22
MGTREFCLK1P_114_T6	T6	NC	
MGTREFCLK1N_114_T5	T5	NC	

DUT
BANK 116
6vlx240tff1156

MGTTXP0_116_D1	D1	FMC_LPC_DP0_C2M_P	20
MGTTXN0_116_D2	D2	FMC_LPC_DP0_C2M_N	20
MGTRXP0_116_G3	G3	FMC_LPC_DP0_M2C_P	20
MGTRXN0_116_G4	G4	FMC_LPC_DP0_M2C_N	20
MGTTXP1_116_C3	C3	SFP_TX_P	23
MGTTXN1_116_C4	C4	SFP_TX_N	23
MGTRXP1_116_E3	E3	SFP_RX_P	23
MGTRXN1_116_E4	E4	SFP_RX_N	23
MGTTXP2_116_B1	B1	SMA_TX_P	30
MGTTXN2_116_B2	B2	SMA_TX_N	30
MGTRXP2_116_D5	D5	SMA_RX_P	30
MGTRXN2_116_D6	D6	SMA_RX_N	30
MGTTXP3_116_A3	A3	SGMII_TX_P	24
MGTTXN3_116_A4	A4	SGMII_TX_N	24
MGTRXP3_116_B5	B5	SGMII_RX_P	24
MGTRXN3_116_B6	B6	SGMII_RX_N	24
MGTREFCLK0P_116_H6	H6	SGMIICLK_QO_P	30
MGTREFCLK0N_116_H5	H5	SGMIICLK_QO_N	30
MGTREFCLK1P_116_F6	F6	SMA_REFCLK_P	30
MGTREFCLK1N_116_F5	F5	SMA_REFCLK_N	30

U1

22 FMC_HPC_CLK3_M2C_MGT_R C396 1 0.1UF 10V X5R 2 FMC_HPC_CLK3_M2C_MGT_C_P 10

22 FMC_HPC_CLK3_M2C_MGT_N C397 1 0.1UF 10V X5R 2 FMC_HPC_CLK3_M2C_MGT_C_N 10

U1

16 FMC_HPC_GBTCLK1_M2C_P C426 1 0.1UF 10V X5R 2 FMC_HPC_GBTCLK1_M2C_C_P 10

16 FMC_HPC_GBTCLK1_M2C_N C427 1 0.1UF 10V X5R 2 FMC_HPC_GBTCLK1_M2C_C_N 10

U1

LX240T ONLY

DUT
BANK 113
6vlx240tff1156

MGTTXP0_113_AH1	AH1	FMC_HPC_DP3_C2M_P	16
MGTTXN0_113_AH2	AH2	FMC_HPC_DP3_C2M_N	16
MGTRXP0_113_AG3	AG3	FMC_HPC_DP3_M2C_P	16
MGTRXN0_113_AG4	AG4	FMC_HPC_DP3_M2C_N	16
MGTTXP1_113_AF1	AF1	FMC_HPC_DP2_C2M_P	16
MGTTXN1_113_AF2	AF2	FMC_HPC_DP2_C2M_N	16
MGTRXP1_113_AF5	AF5	FMC_HPC_DP2_M2C_P	16
MGTRXN1_113_AF6	AF6	FMC_HPC_DP2_M2C_N	16
MGTTXP2_113_AD1	AD1	FMC_HPC_DP1_C2M_P	16
MGTTXN2_113_AD2	AD2	FMC_HPC_DP1_C2M_N	16
MGTRXP2_113_AE3	AE3	FMC_HPC_DP1_M2C_P	16
MGTRXN2_113_AE4	AE4	FMC_HPC_DP1_M2C_N	16
MGTTXP3_113_AB1	AB1	FMC_HPC_DP0_C2M_P	16
MGTTXN3_113_AB2	AB2	FMC_HPC_DP0_C2M_N	16
MGTRXP3_113_AC3	AC3	FMC_HPC_DP0_M2C_P	16
MGTRXN3_113_AC4	AC4	FMC_HPC_DP0_M2C_N	16
MGTREFCLK0P_113_AD6	AD6	FMC_HPC_GBTCLK0_M2C_C_P	10
MGTREFCLK0N_113_AD5	AD5	FMC_HPC_GBTCLK0_M2C_C_N	10
MGTREFCLK1P_113_AB6	AB6	FMC_HPC_CLK2_M2C_MGT_P	10
MGTREFCLK1N_113_AB5	AB5	FMC_HPC_CLK2_M2C_MGT_N	10

DUT
BANK 115
6vlx240tff1156

MGTTXP0_115_M1	M1	PCIE_TX3_P	21
MGTTXN0_115_M2	M2	PCIE_TX3_N	21
MGTRXP0_115_N3	N3	PCIE_RX3_P	21
MGTRXN0_115_N4	N4	PCIE_RX3_N	21
MGTTXP1_115_K1	K1	PCIE_TX2_P	21
MGTTXN1_115_K2	K2	PCIE_TX2_N	21
MGTRXP1_115_L3	L3	PCIE_RX2_P	21
MGTRXN1_115_L4	L4	PCIE_RX2_N	21
MGTTXP2_115_H1	H1	PCIE_TX1_P	21
MGTTXN2_115_H2	H2	PCIE_TX1_N	21
MGTRXP2_115_K5	K5	PCIE_RX1_P	21
MGTRXN2_115_K6	K6	PCIE_RX1_N	21
MGTTXP3_115_F1	F1	PCIE_TX0_P	21
MGTTXN3_115_F2	F2	PCIE_TX0_N	21
MGTRXP3_115_J3	J3	PCIE_RX0_P	21
MGTRXN3_115_J4	J4	PCIE_RX0_N	21
MGTREFCLK0P_115_P6	P6	PCIE_100M_MGT0_P	22
MGTREFCLK0N_115_P5	P5	PCIE_100M_MGT0_N	22
MGTREFCLK1P_115_M6	M6	FMC_LPC_GBTCLK0_M2C_C_P	10
MGTREFCLK1N_115_M5	M5	FMC_LPC_GBTCLK0_M2C_C_N	10
MGTAVTTRCAL_115_AP7	AP7		
MGTRREF_115_AN7	AN7		

MGT_AVTT

1 R213 100 1% 2 1/16W

U1

22 FMC_HPC_CLK2_M2C_MGT_R C398 1 0.1UF 10V X5R 2 FMC_HPC_CLK2_M2C_MGT_C_P 10

22 FMC_HPC_CLK2_M2C_MGT_N C399 1 0.1UF 10V X5R 2 FMC_HPC_CLK2_M2C_MGT_C_N 10

U1

16 FMC_HPC_GBTCLK0_M2C_P C425 1 0.1UF 10V X5R 2 FMC_HPC_GBTCLK0_M2C_C_P 10

16 FMC_HPC_GBTCLK0_M2C_N C424 1 0.1UF 10V X5R 2 FMC_HPC_GBTCLK0_M2C_C_N 10

20 FMC_LPC_GBTCLK0_M2C_P C422 1 0.1UF 10V X5R 2 FMC_LPC_GBTCLK0_M2C_C_P 10

20 FMC_LPC_GBTCLK0_M2C_N C423 1 0.1UF 10V X5R 2 FMC_LPC_GBTCLK0_M2C_C_N 10

FPGA MGT Banks

XILINX

Title:	FPGA MGT Banks SCHEM, ROHS COMPLIANT ML605	ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311	
Date:	9-17-2009_15:42	Ver:	D
Sheet Size: B		Rev:	04
Sheet	10 of 48	Drawn By	BF

DUT
BANK VCCINT
6vlx240tff1156

VCCINT_FPGA

VCCINT_Y21	Y21
VCCINT_Y19	Y19
VCCINT_Y17	Y17
VCCINT_Y15	Y15
VCCINT_Y13	Y13
VCCINT_Y11	Y11
VCCINT_W20	W20
VCCINT_W16	W16
VCCINT_W14	W14
VCCINT_W12	W12
VCCINT_V21	V21
VCCINT_V19	V19
VCCINT_V15	V15
VCCINT_V13	V13
VCCINT_V11	V11
VCCINT_U20	U20
VCCINT_U16	U16
VCCINT_U14	U14
VCCINT_U12	U12
VCCINT_U10	U10
VCCINT_T21	T21
VCCINT_T19	T19
VCCINT_T15	T15
VCCINT_T13	T13
VCCINT_T11	T11
VCCINT_R20	R20
VCCINT_R18	R18
VCCINT_R16	R16
VCCINT_R14	R14
VCCINT_R12	R12
VCCINT_R10	R10
VCCINT_P21	P21
VCCINT_P19	P19
VCCINT_P17	P17
VCCINT_P15	P15
VCCINT_P13	P13
VCCINT_P11	P11
VCCINT_N20	N20
VCCINT_N18	N18
VCCINT_N16	N16
VCCINT_N14	N14
VCCINT_N12	N12
VCCINT_M21	M21
VCCINT_M19	M19
VCCINT_AB21	AB21
VCCINT_AB19	AB19
VCCINT_AB17	AB17
VCCINT_AB15	AB15
VCCINT_AB13	AB13
VCCINT_AB11	AB11
VCCINT_AA20	AA20
VCCINT_AA18	AA18
VCCINT_AA16	AA16
VCCINT_AA14	AA14
VCCINT_AA12	AA12

U1

DUT
BANK VCCAUX
6vlx240tff1156

VCCAUX

VCCAUX_Y23	Y23
VCCAUX_W22	W22
VCCAUX_W10	W10
VCCAUX_V9	V9
VCCAUX_U22	U22
VCCAUX_T9	T9
VCCAUX_R22	R22
VCCAUX_P23	P23
VCCAUX_P9	P9
VCCAUX_N22	N22
VCCAUX_N10	N10
VCCAUX_AA22	AA22
VCCAUX_AA10	AA10

U1

DUT
BANK MGTAVCC_N
6vlx240tff1156

MGT_AVCC

MGTAVCC_N_N6	N6
MGTAVCC_N_L6	L6
MGTAVCC_N_J6	J6
MGTAVCC_N_G6	G6
MGTAVCC_N_E6	E6
MGTAVCC_N_C6	C6

U1

DUT
BANK MGTAVCC_S
6vlx240tff1156

MGT_AVCC

MGTAVCC_S_W6	W6
MGTAVCC_S_U6	U6
MGTAVCC_S_R6	R6
MGTAVCC_S_AN6	AN6
MGTAVCC_S_AL6	AL6
MGTAVCC_S_AJ6	AJ6
MGTAVCC_S_AG6	AG6
MGTAVCC_S_AE6	AE6
MGTAVCC_S_AC6	AC6
MGTAVCC_S_AA6	AA6

U1

DUT
BANK MGTAVTT_N
6vlx240tff1156

MGT_AVTT

MGTAVTT_N_M3	M3
MGTAVTT_N_L2	L2
MGTAVTT_N_H3	H3
MGTAVTT_N_G2	G2
MGTAVTT_N_D3	D3
MGTAVTT_N_C2	C2

U1

DUT
BANK MGTAVTT_S
6vlx240tff1156

MGT_AVTT

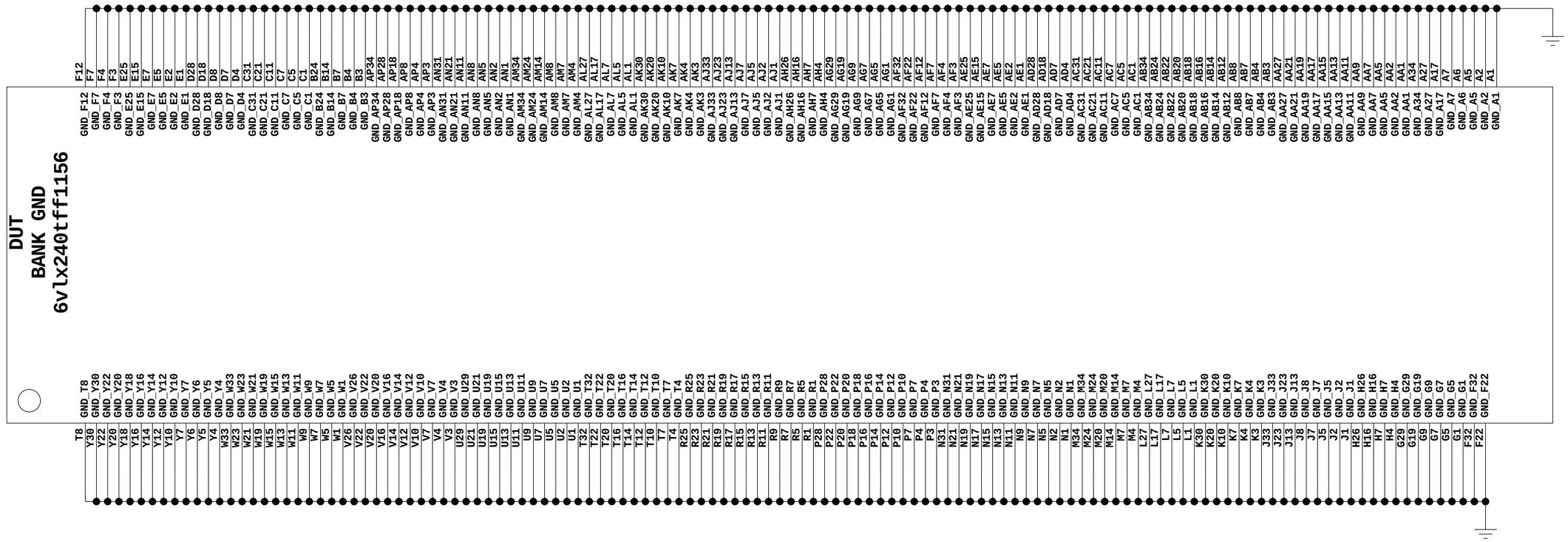
MGTAVTT_S_Y3	Y3
MGTAVTT_S_W2	W2
MGTAVTT_S_T3	T3
MGTAVTT_S_R2	R2
MGTAVTT_S_AM3	AM3
MGTAVTT_S_AL2	AL2
MGTAVTT_S_AH3	AH3
MGTAVTT_S_AG2	AG2
MGTAVTT_S_AD3	AD3
MGTAVTT_S_AC2	AC2

U1

FPGA Power

XILINX

Title:	FPGA Power SCHEM, ROHS COMPLIANT ML605	ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311
Date:	9-17-2009_15:42	Ver: D
Sheet Size: B		Rev: 04
Sheet	11 of 48	Drawn By BF



FPGA GND

XILINX

Title:	FPGA GND SCHEM, ROHS COMPLIANT ML605	ASSY P/N: PCB P/N: SCH P/N:	0431540 1280479 0381311
Date:	9-17-2009_15:42	Ver:	D
Sheet Size: B		Rev:	04
Sheet	12 of 48	Drawn By	BF

SYSTEMACE TQFP144 (DIE DOWN)

PARTS=1
LEVEL=STD
XCCACE-TQ144I

U19

Silkscreen: PROG

Silkscreen: "SYSACE RESET"

SysACE Failsafe Mode Jumpers

OR = Failsafe Mode Enabled

Combined FPGA & CPU PC4 Connector

U73

N7E50-7516PG-20

Silkscreen "System ACE" "Status LED"

Silkscreen "System ACE" "Error LED"

Disable Sysace Error LED

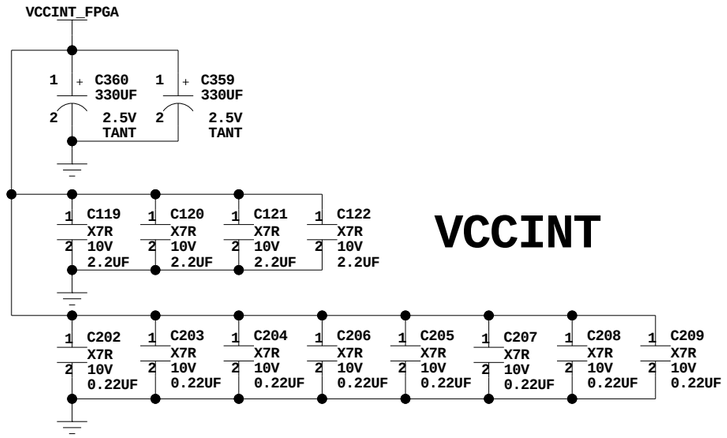
System ACE CF

XILINX

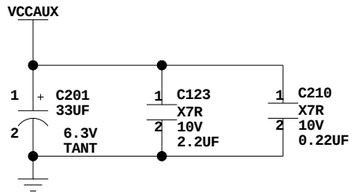
Title: SCHEM, ROHS COMPLIANT, SYSTEM ACE CF		ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311	
Date:	3-17-2010_8:25	Ver:	D
Sheet Size: B		Rev:	04
Sheet	13 of 48	Drawn By	BF

V-6 FF1156 DECOUPLING

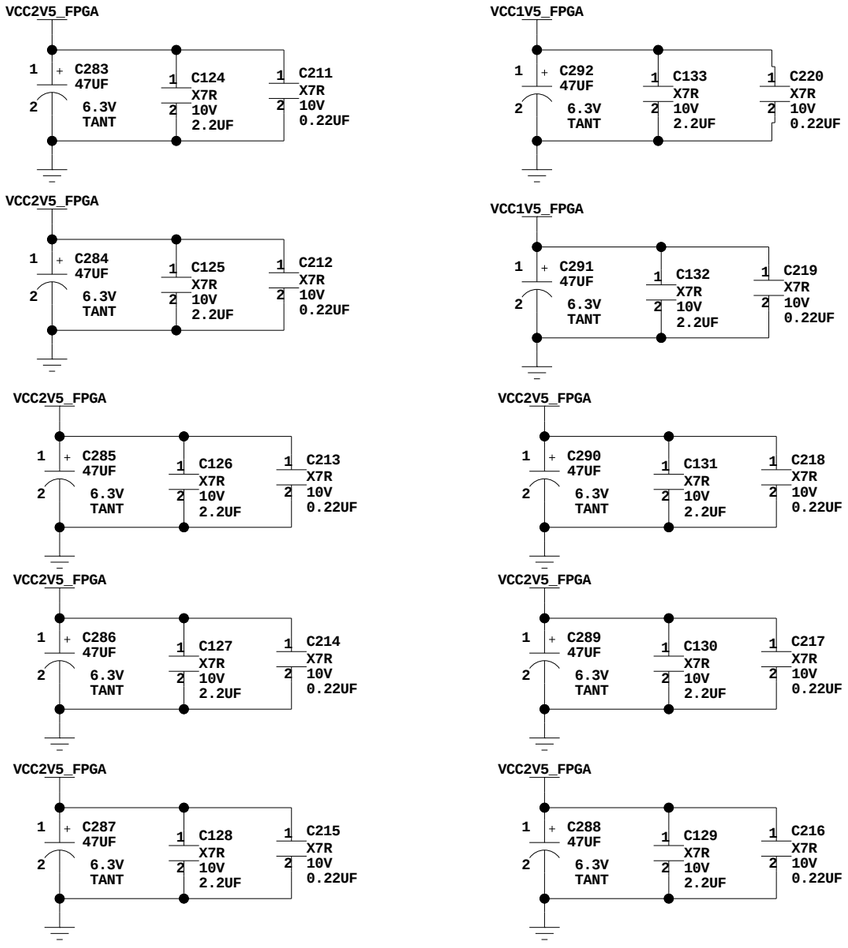
VCCINT

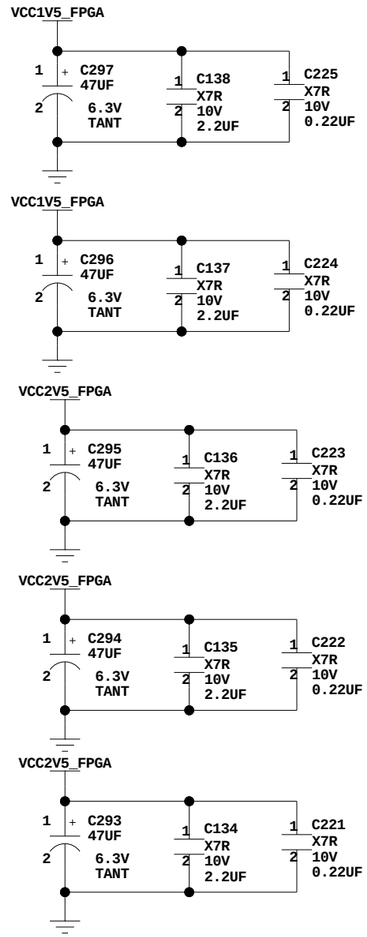


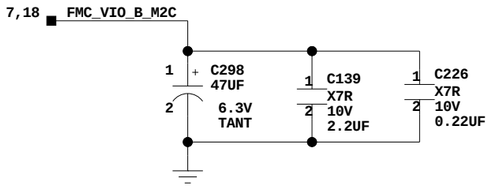
VCCAUX



VCCO







PLACEMENT RULES

330uF, 100uF, 47uF, 33uF: Anywhere on board, but as close as possible to FPGA.

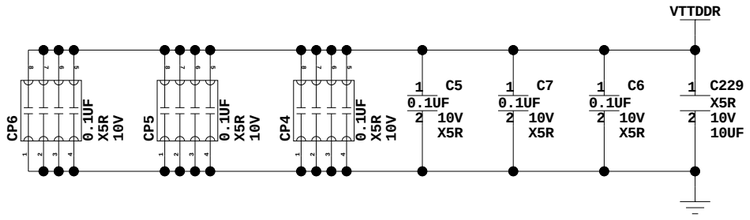
2.2uF: No more than 3" from periphery of FPGA, but as close as possible.

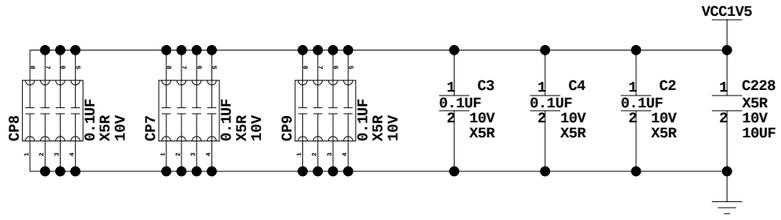
0.22uF: No more than 1" from periphery of FPGA, but as close as possible.

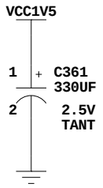
FPGA Decoupling

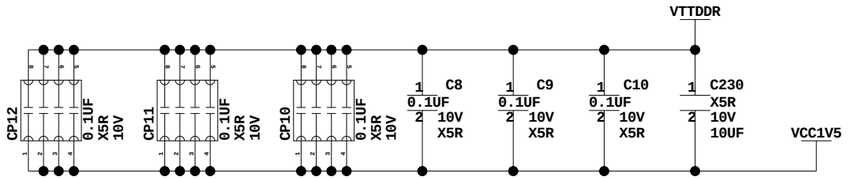
XILINX

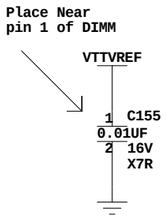
Title:	FPGA Decoupling SCHEM, ROHS COMPLIANT ML605	ASSY P/N: PCB P/N: SCH P/N:	0431540 1280479 0381311
Date:	9-17-2009_15:42	Ver:	D
Sheet Size: B		Rev:	04
Sheet	14 of 48	Drawn By	BF

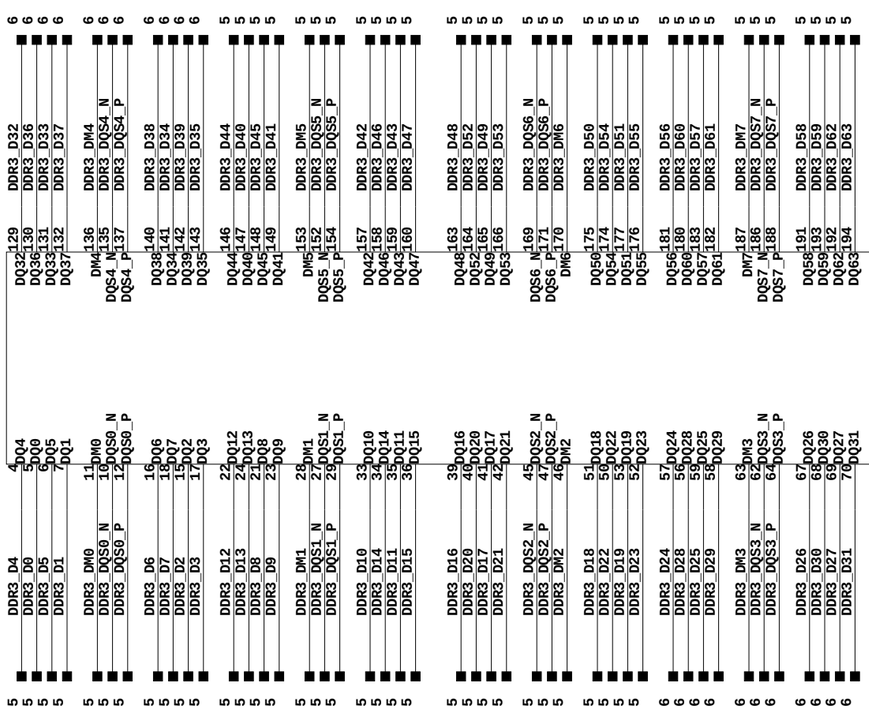


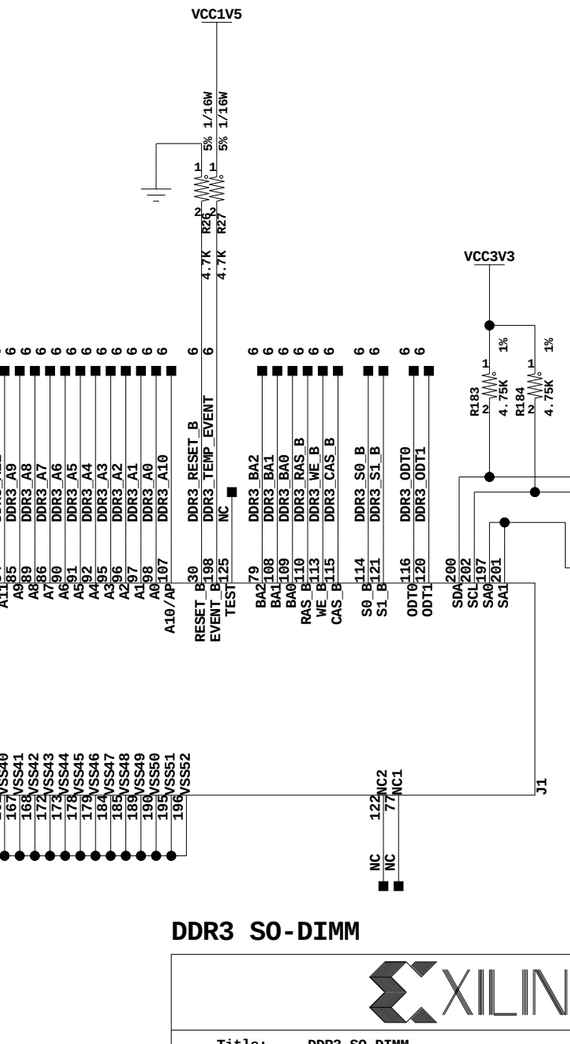










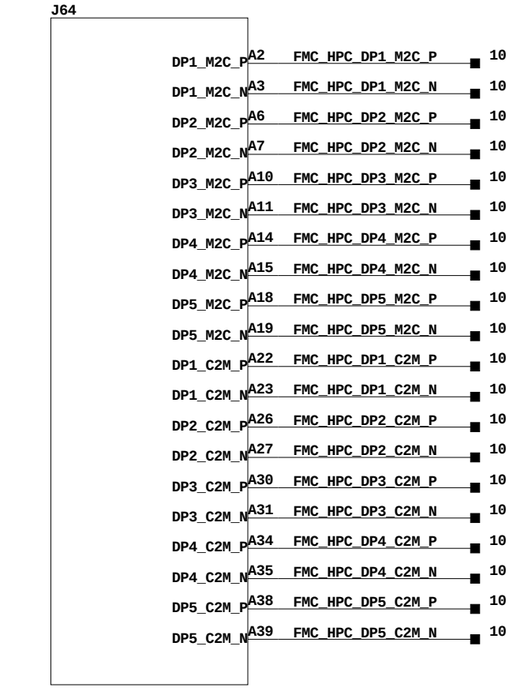


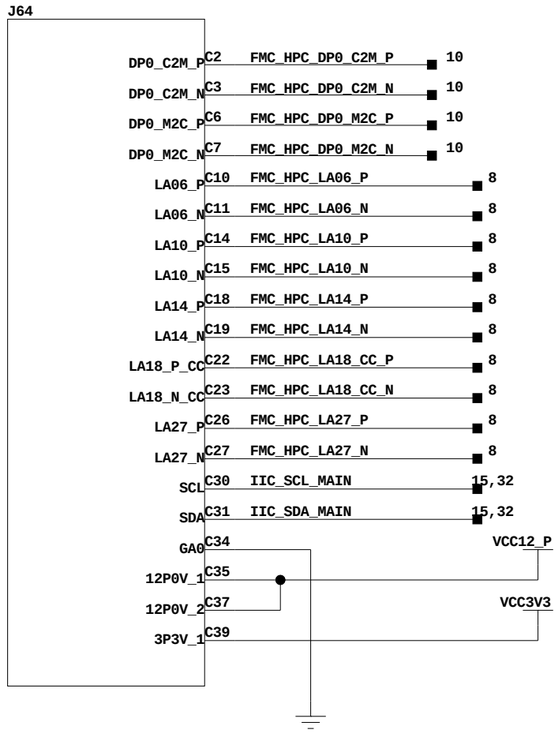
Silkscreen:
"DDR3 SO-DIMM"

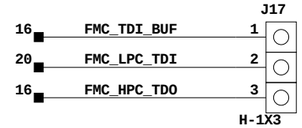
DDR3 SO-DIMM

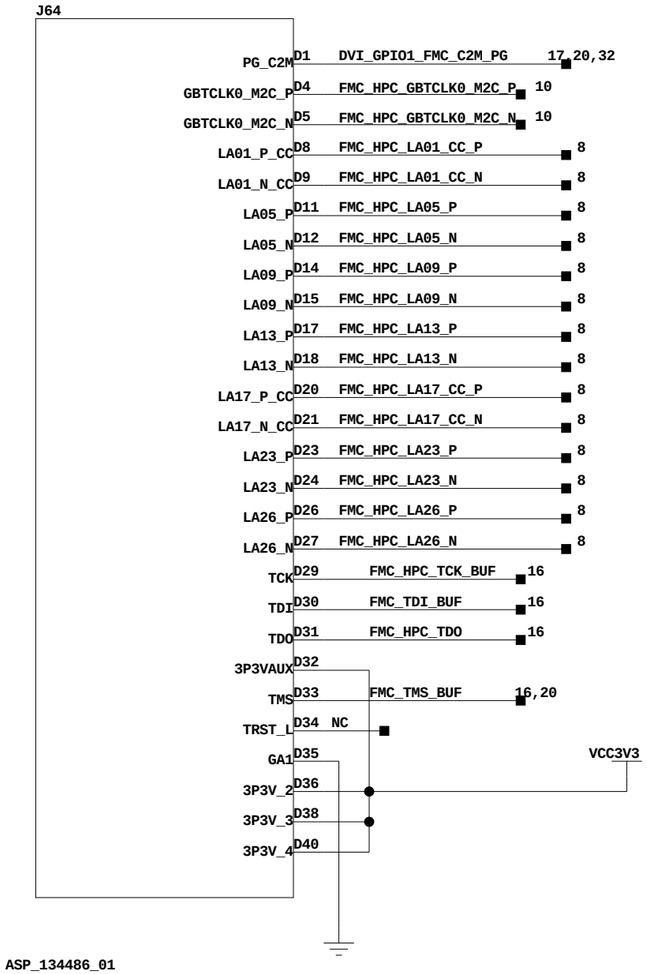
XILINX

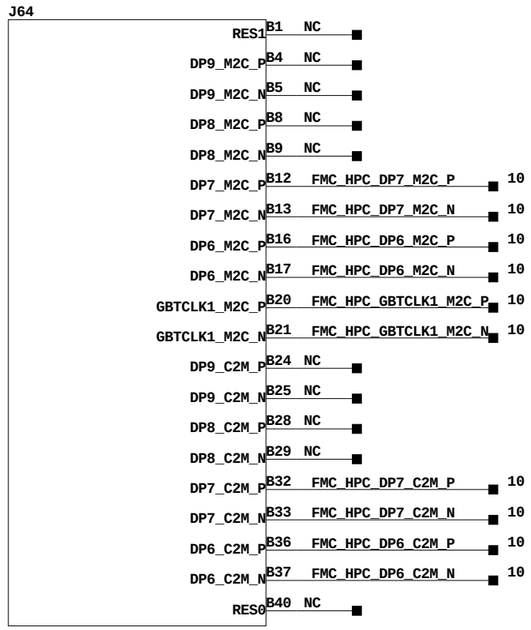
Title:	DDR3 SO-DIMM SCHEM, ROHS COMPLIANT ML605	ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311
Date:	9-17-2009_15:42	Ver: D
Sheet Size: B		Rev: 04
Sheet	15 of 48	Drawn By BF

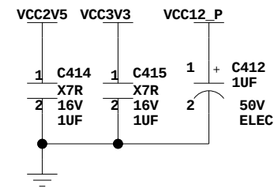


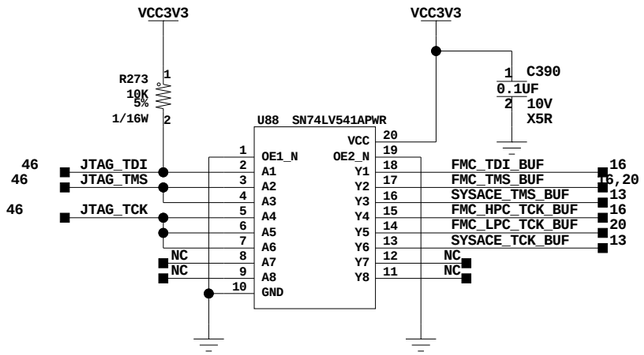






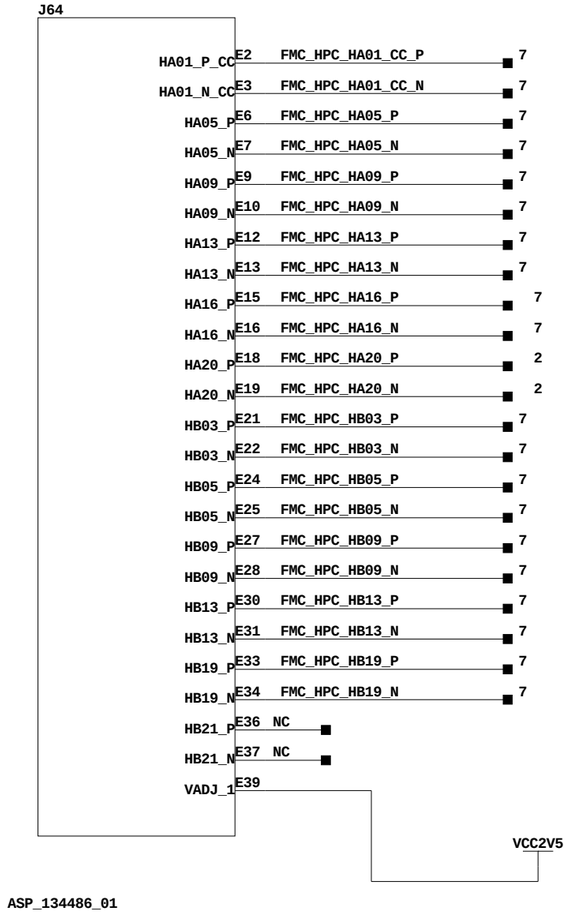




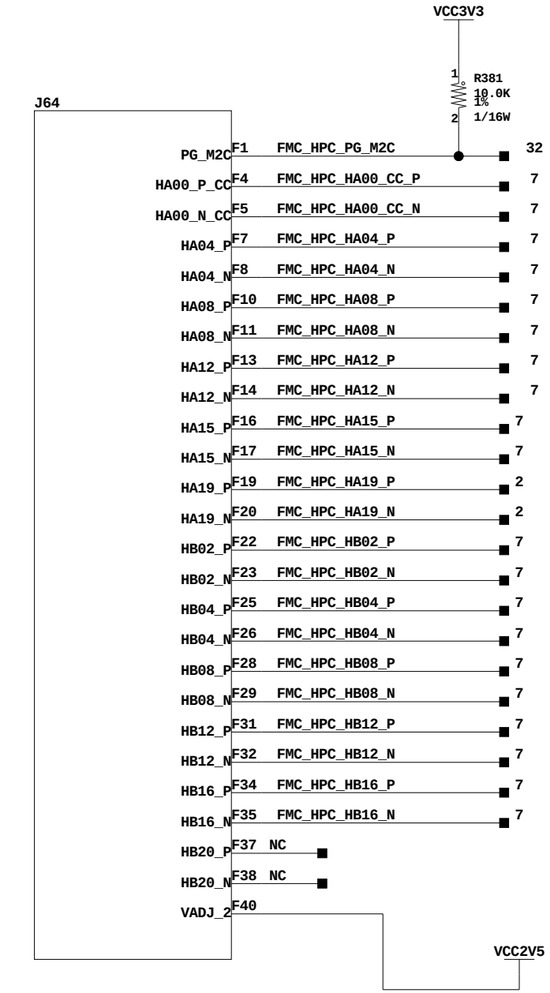


ANSI/VITA 57.1-2008 Version 1.1
FMC HPC Header, Rows A, B, C, D

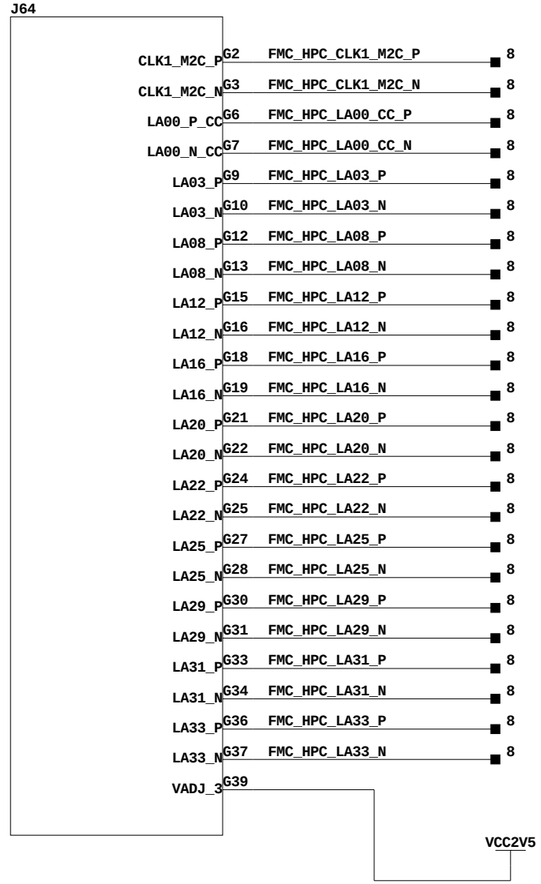
Title:	FMC HPC Header SCHEM, ROHS COMPLIANT ML605	ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311	
Date:	9-17-2009_15:42	Ver:	D
Sheet Size: B		Rev:	04
Sheet	16 of 48	Drawn By	BF



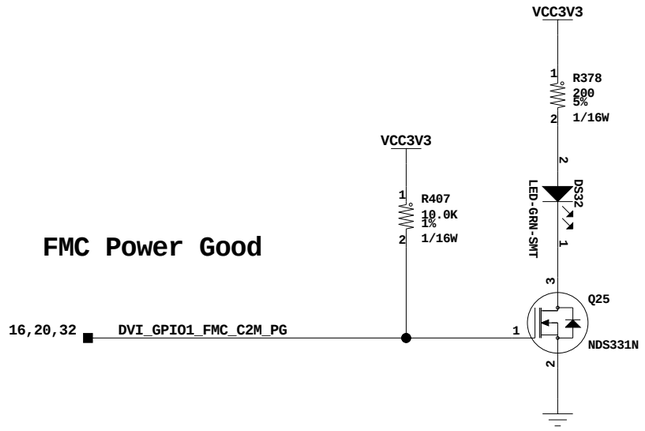
ASP_134486_01



ASP_134486_01

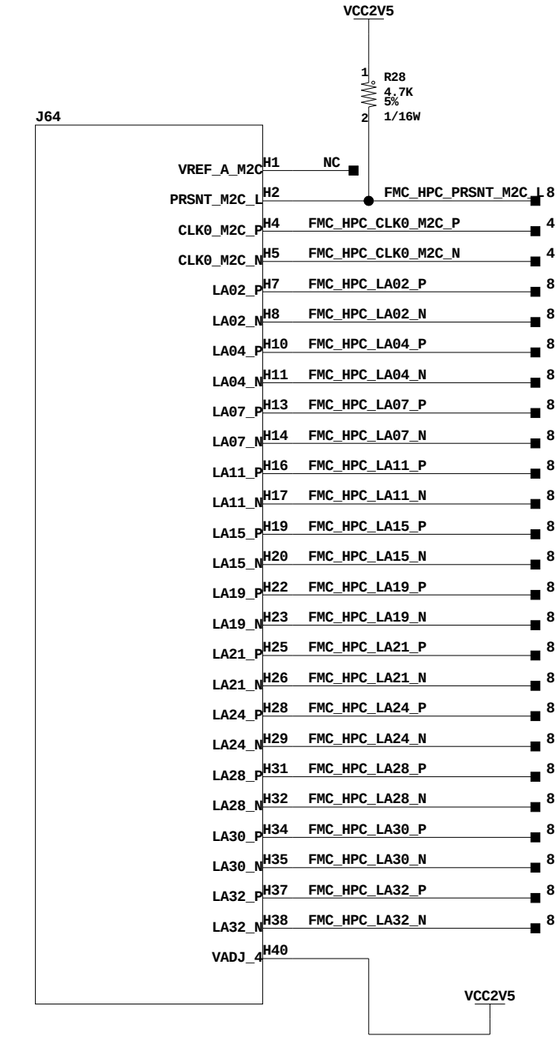


ASP_134486_01

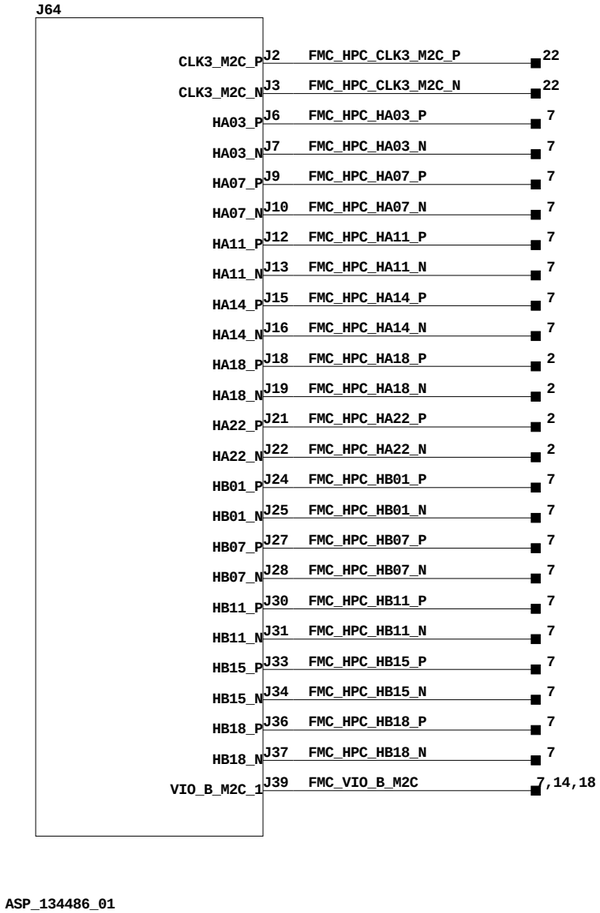


ANSI/VITA 57.1-2008 Version 1.1
FMC HPC Header, Rows E, F, G

Title:	FMC HPC Header SCHEM, ROHS COMPLIANT ML605	ASSY P/N: PCB P/N: SCH P/N:	0431540 1280479 0381311
Date:	9-17-2009_15:42	Ver:	D
Sheet Size: B		Rev:	04
Sheet	17 of 48	Drawn By	BF



ASP_134486_01



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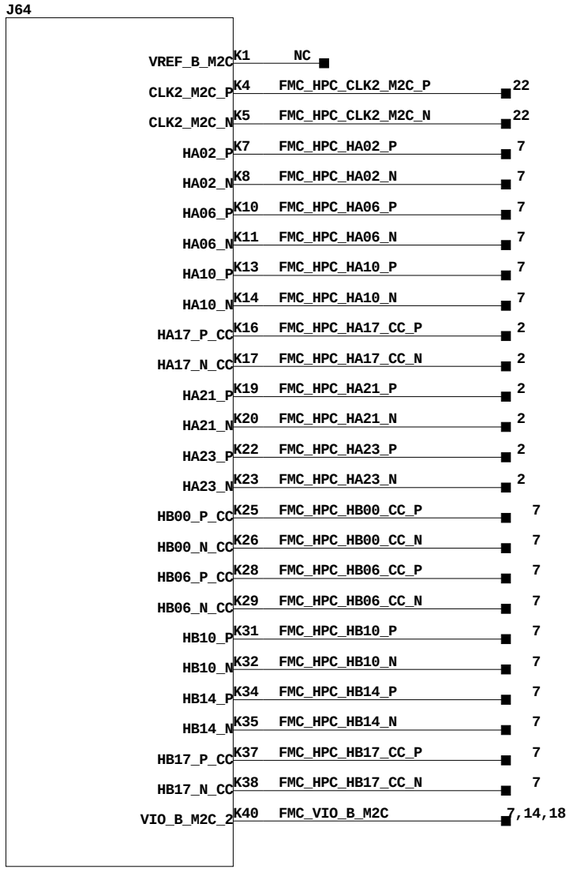
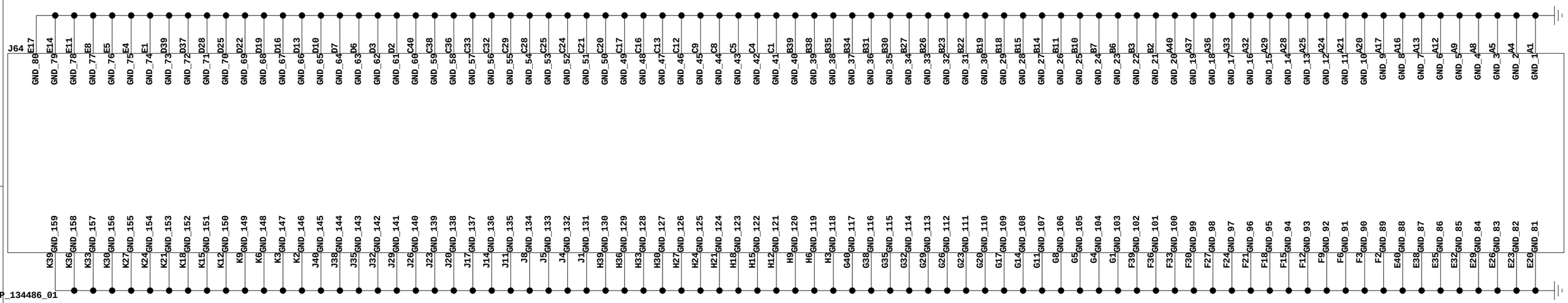


ASP_134486_01

ANSI/VITA 57.1-2008 Version 1.1
FMC HPC Header, Rows H, J, K

XILINX

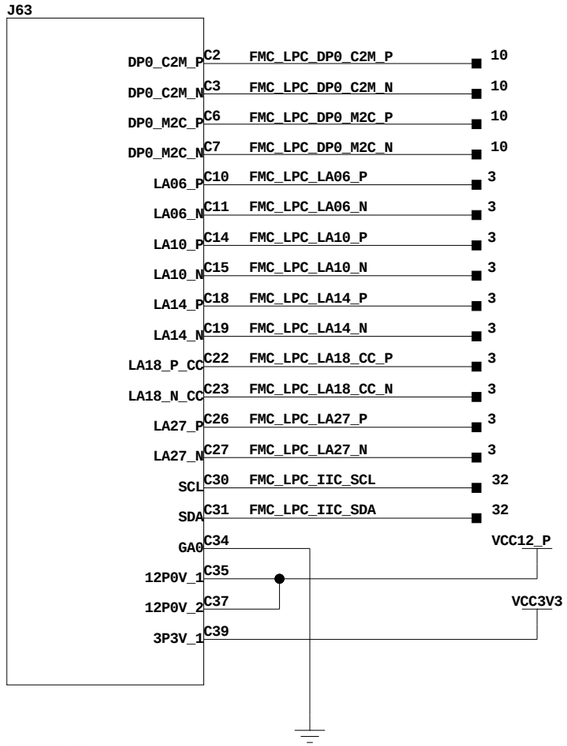
Title:	FMC HPC Header, Rows H, J, K SCHEM, ROHS COMPLIANT ML605	ASSY P/N:	0431540
		PCB P/N:	1280479
		SCH P/N:	0381311
Date:	9-17-2009_15:42	Ver:	D
Sheet Size: B		Rev:	04
Sheet	18 of 48	Drawn By	BF



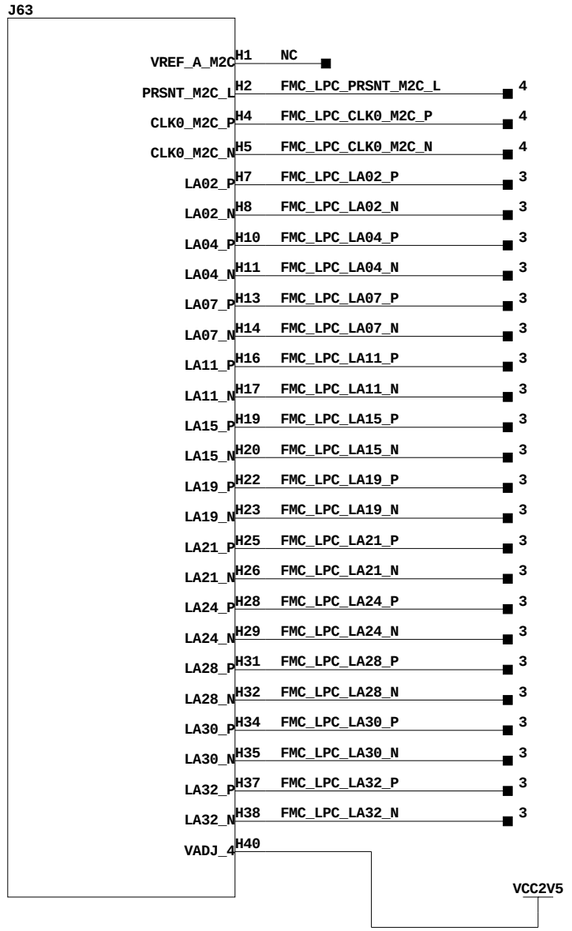
ANSI/VITA 57.1-2008 Version 1.1
FMC HPC Header, GND

XILINX

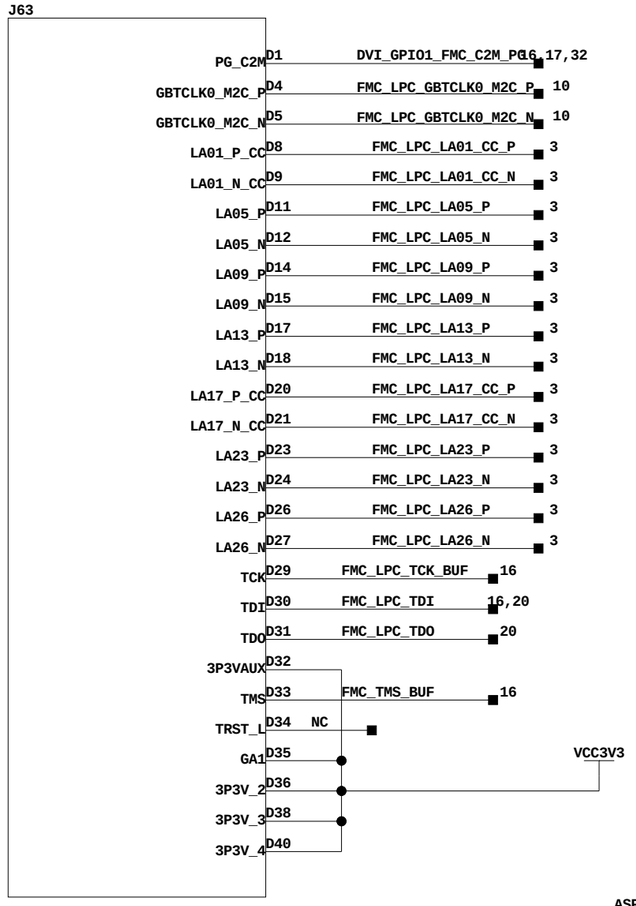
Title:	FMC HPC Header SCHEM, ROHS COMPLIANT ML605	ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311	
Date:	9-17-2009_15:42	Ver:	D
Sheet Size: B		Rev:	04
Sheet	19 of 48	Drawn By	BF



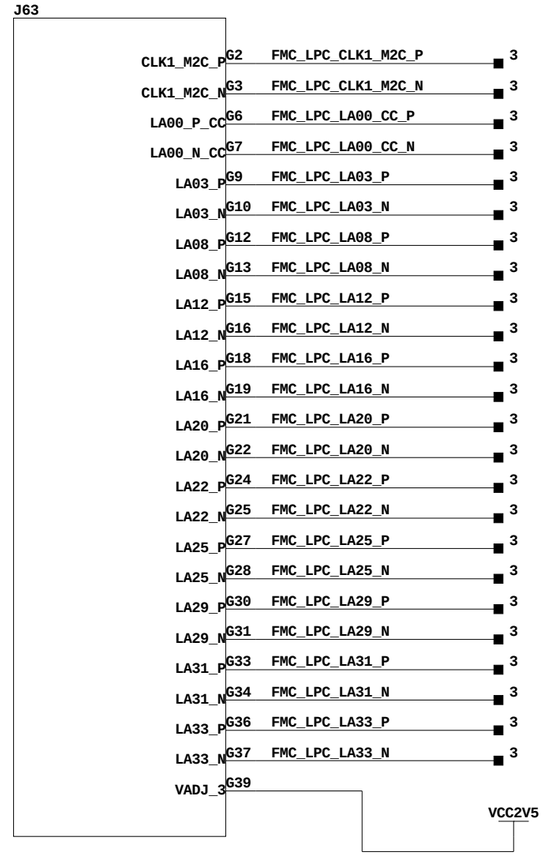
ASP_134603_01



ASP_134603_01



ASP_134603_01



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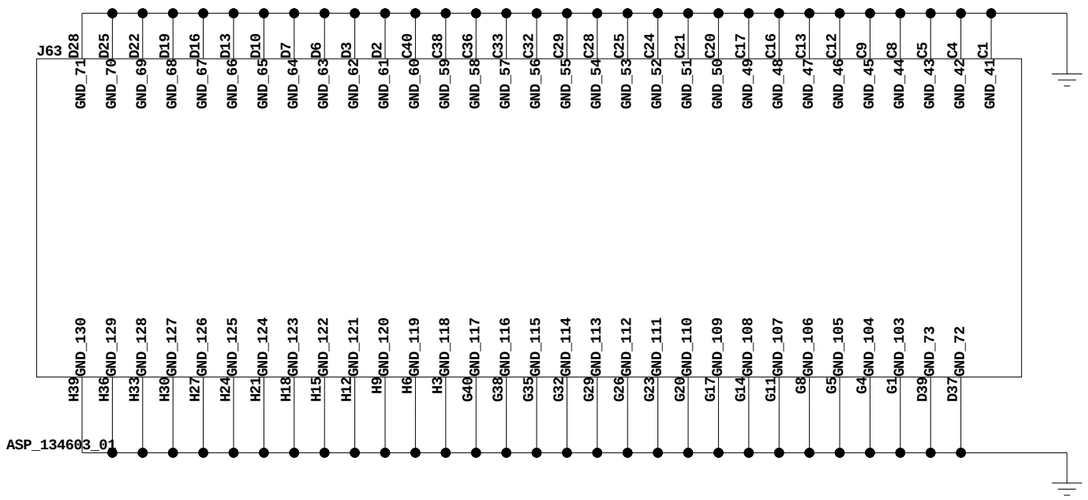
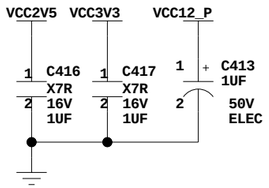
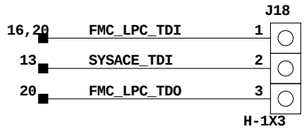


ASP_134603_01

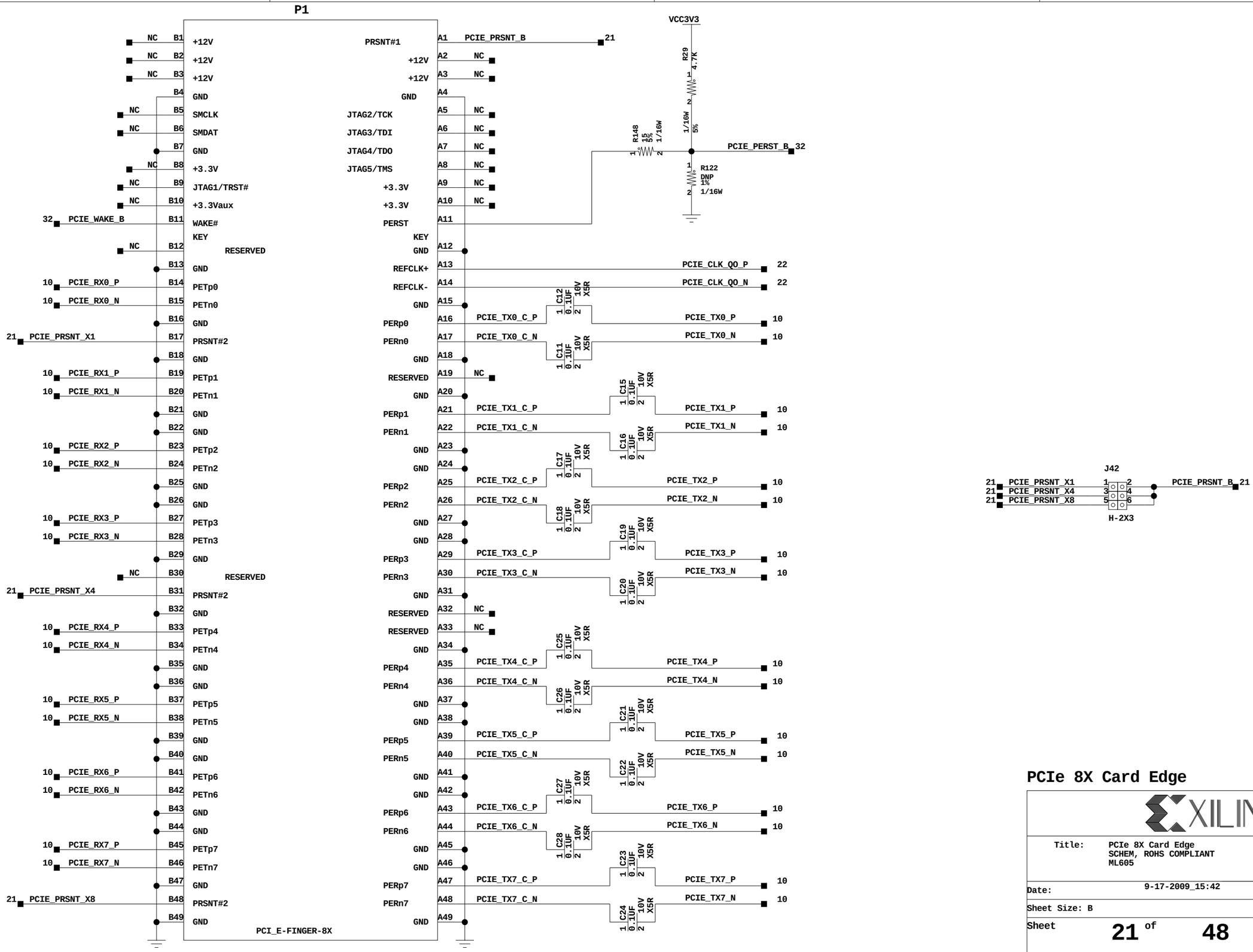


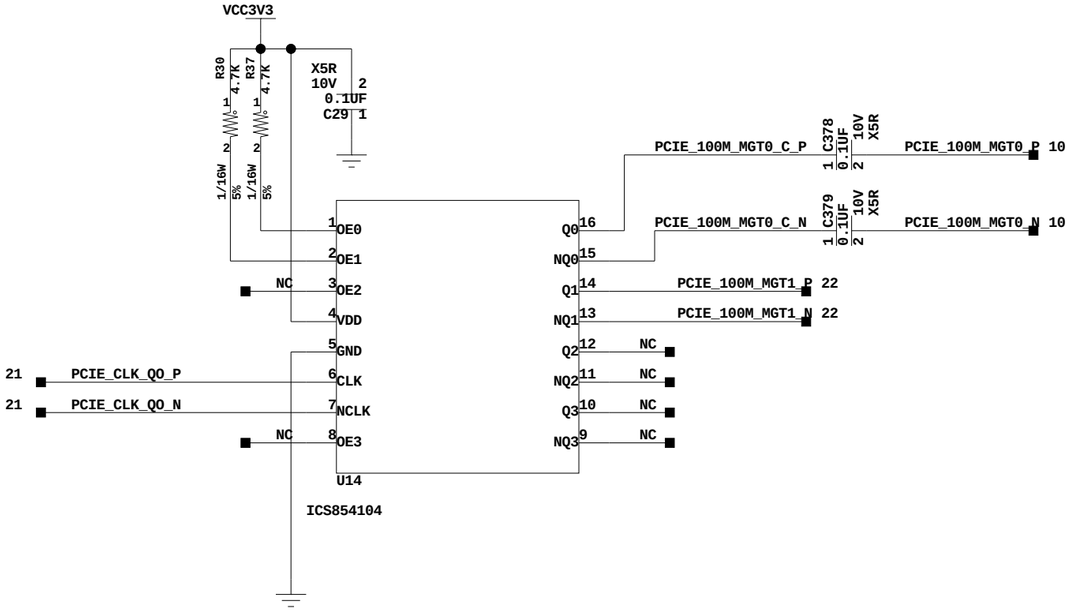


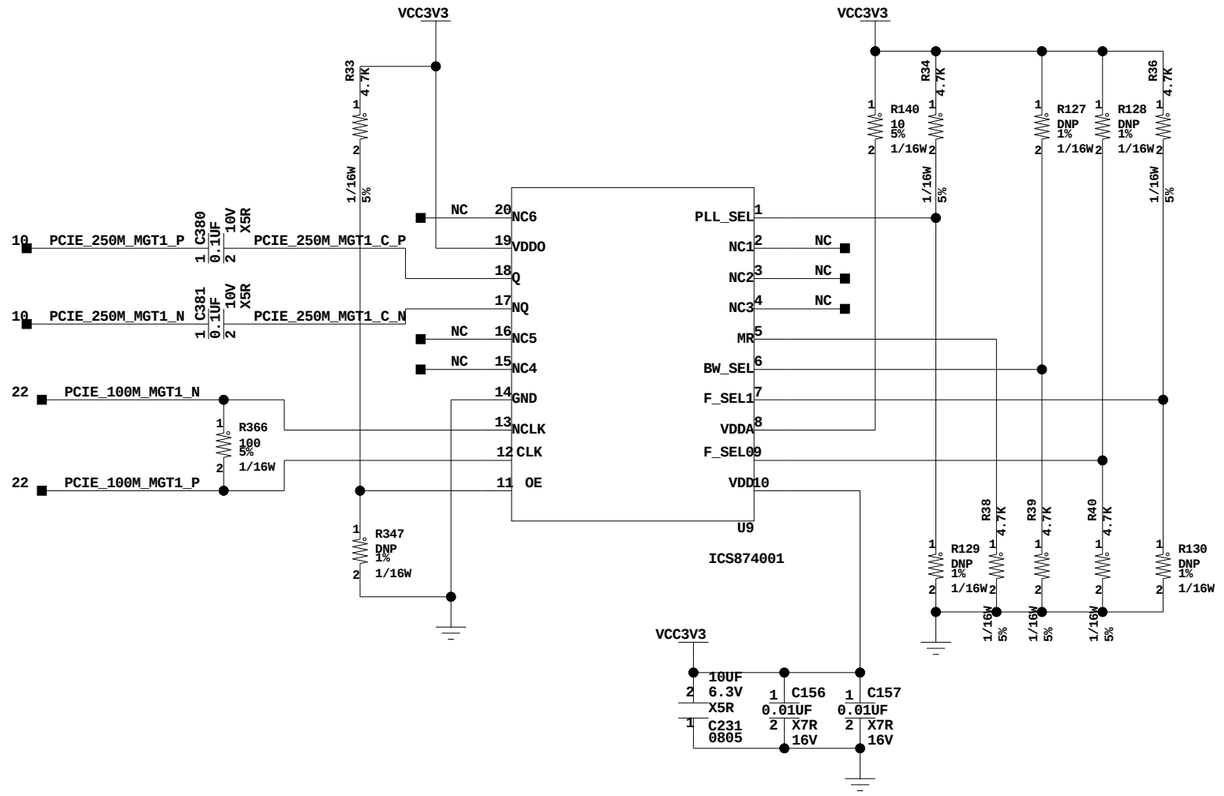
ANSI/VITA 57.1-2008 Version 1.1
FMC LPC Connector

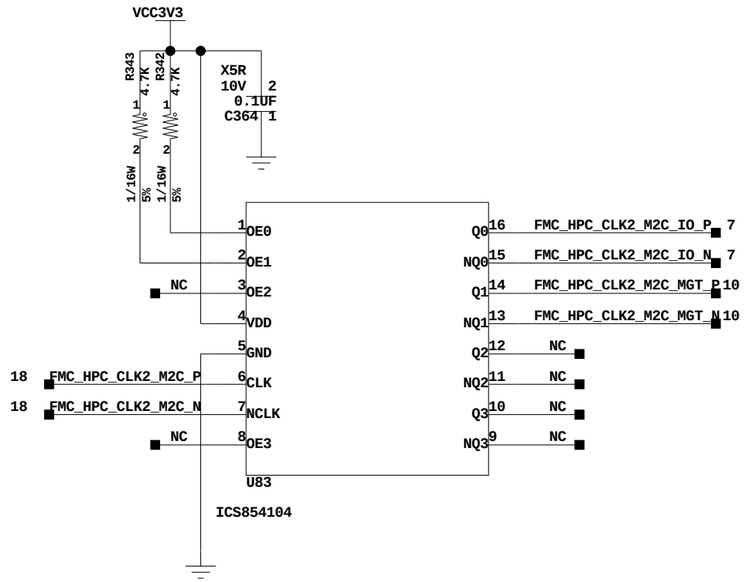
XILINX

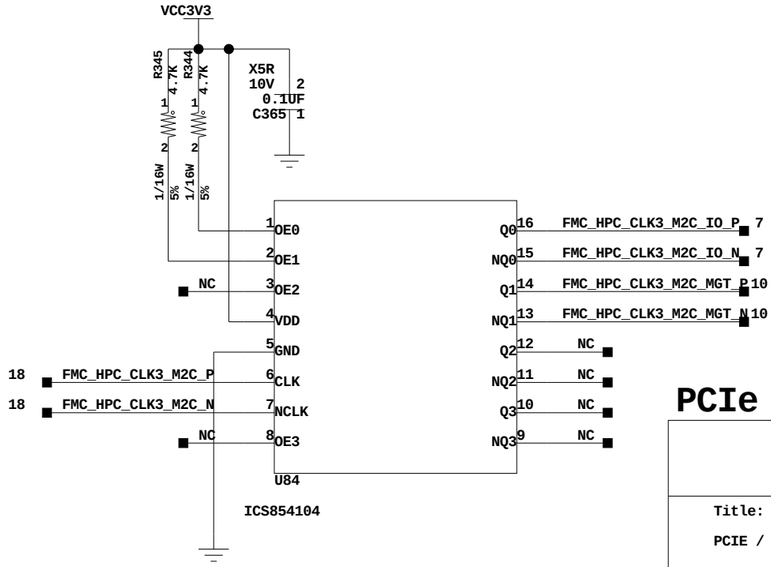
Title:	FMC LPC Connector SCHEM, ROHS COMPLIANT SA605 EVALUATION PLATFORM	ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311	
Date:	9-17-2009_15:42	Ver:	D
Sheet Size: B		Rev:	04
Sheet	20 of 48	Drawn By	BF


P1
PCI_E-FINGER-8X
VCC3V3
R29 4.7K 1/16W 5%
R148 15 5% 1/16W
R122 DNP 1% 1/16W
PCIE_PERST_B 32
J42
H-2X3
PCIE_PRSNT_B 21
PCIE_PRSNT_X1 21
PCIE_PRSNT_X4 21
PCIE_PRSNT_X8 21
PCIe 8X Card Edge
XILINX
Title: PCIe 8X Card Edge
SCHEM, ROHS COMPLIANT
ML605
ASSY P/N: 0431540
PCB P/N: 1280479
SCH P/N: 0381311
Date: 9-17-2009_15:42
Ver: D
Sheet Size: B
Rev: 04
Sheet 21 of 48
Drawn By BF







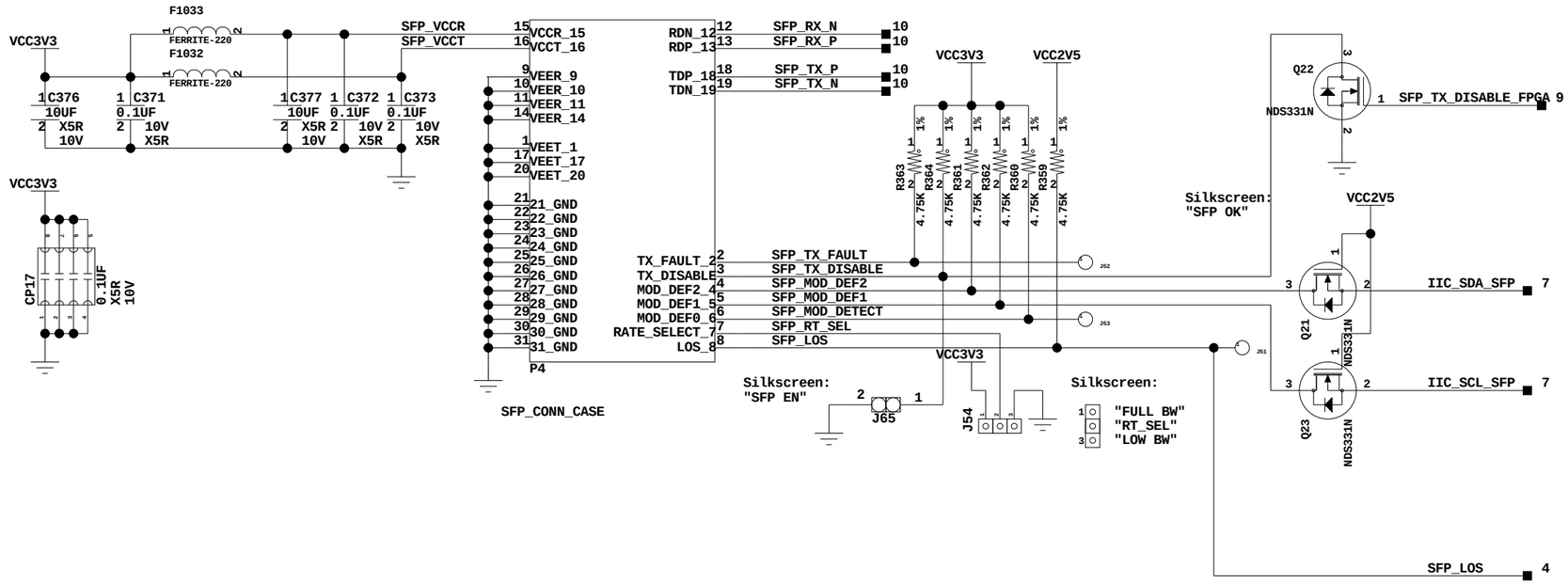


PCIe / MGT Clocking

XILINX

Title: SCHEM, ROHS COMPLIANT, PCIE / MGT CLOCKING		ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311	
Date:	9-24-2009_11:18	Ver:	D
Sheet Size: B		Rev:	04
Sheet	22 of 48	Drawn By	BF

SFP MODULE



SFP Cage

Title:	SCHEM, ROHS COMPLIANT SFP Cage	ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311	
Date:	9-24-2009_11:18	Ver:	D
Sheet Size: B		Rev:	04
Sheet	23 of 48	Drawn By	BF

The PHY MDIP Pins below are
Media Dependent Interface Pins (MDIP),
and are all bidirectional pins.

Pin to Constant Mapping	
Pin	Bit [2:0]
VCC2V5	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
GND	000

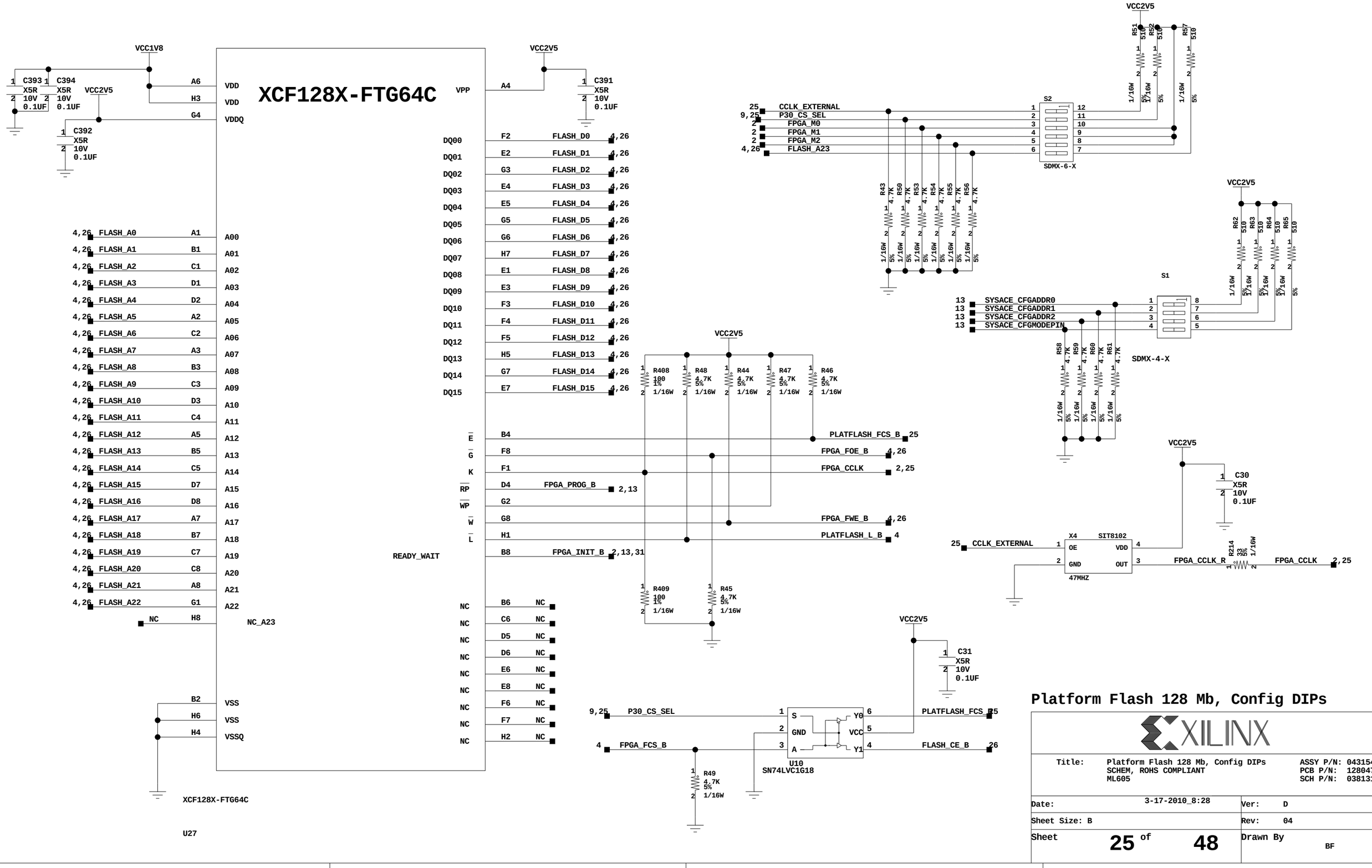
J66, J67 pins 1-2: GMII/MII to Cu
J66, J67 pins 2-3: SGMII to Cu, no clk
J66 pins 1-2, J68 ON: RGMII, modified MII in Cu

Pin	Bit[2]	Bit[1]	Bit[0]		
CFG0	PHYADR[2]	PHYADR[1]	PHYADR[0]	111	PHYAddr "00111". Don't advertise the PAUSE bit
CFG1	ENA_PAUSE	PHYADR[4]	PHYADR[3]	000	
CFG2	ANEG[3]	ANEG[2]	ANEG[1]	111	Auto-Neg en, advertise all caps; prefer slave. Auto crossover enabled.
CFG3	ANEG[0]	ENA_XC	DIS_125	111	125 CLK option disabled.
CFG4	HWCFG_MD[2]	HWCFG_MD[1]	HWCFG_MD[0]	111	GMII to Cu mode. Fiber/copper auto-detect diasabled.
CFG5	DIS_FC	DIS_SLEEP	HWCFG_MD[3]	111	Sleep mode disabled.
CFG6	SEL_BDT	INT_POL	75/50 OHM	010	MDC/MDIO selected. Active LOW interrupt 50Ohm SERDES option.

10/100/1000 PHY

XILINX

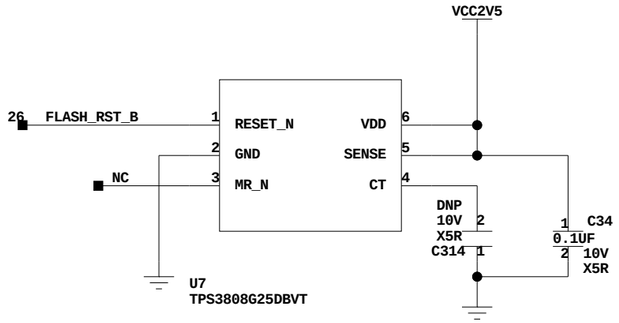
Title:	10/100/1000 PHY SCHEM, ROHS COMPLIANT ML605 EVALUATION PLATFORM	ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311	
Date:	9-24-2009_11:19	Ver:	D
Sheet Size: B		Rev:	04
Sheet	24 of 48	Drawn By	BF



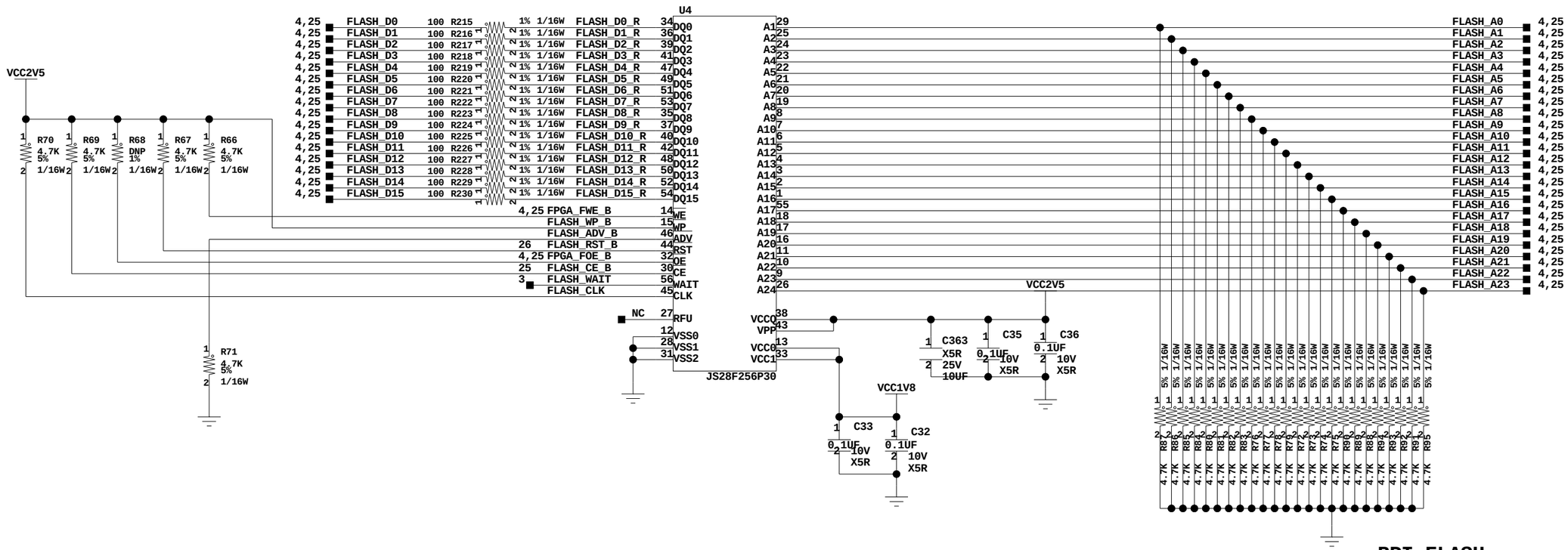
Platform Flash 128 Mb, Config DIPs

XILINX

Title:	Platform Flash 128 Mb, Config DIPs SCHEM, ROHS COMPLIANT ML605	ASSY P/N:	0431540 PCB P/N: 1280479 SCH P/N: 0381311
Date:	3-17-2010_8:28	Ver:	D
Sheet Size: B		Rev:	04
Sheet	25 of 48	Drawn By	BF



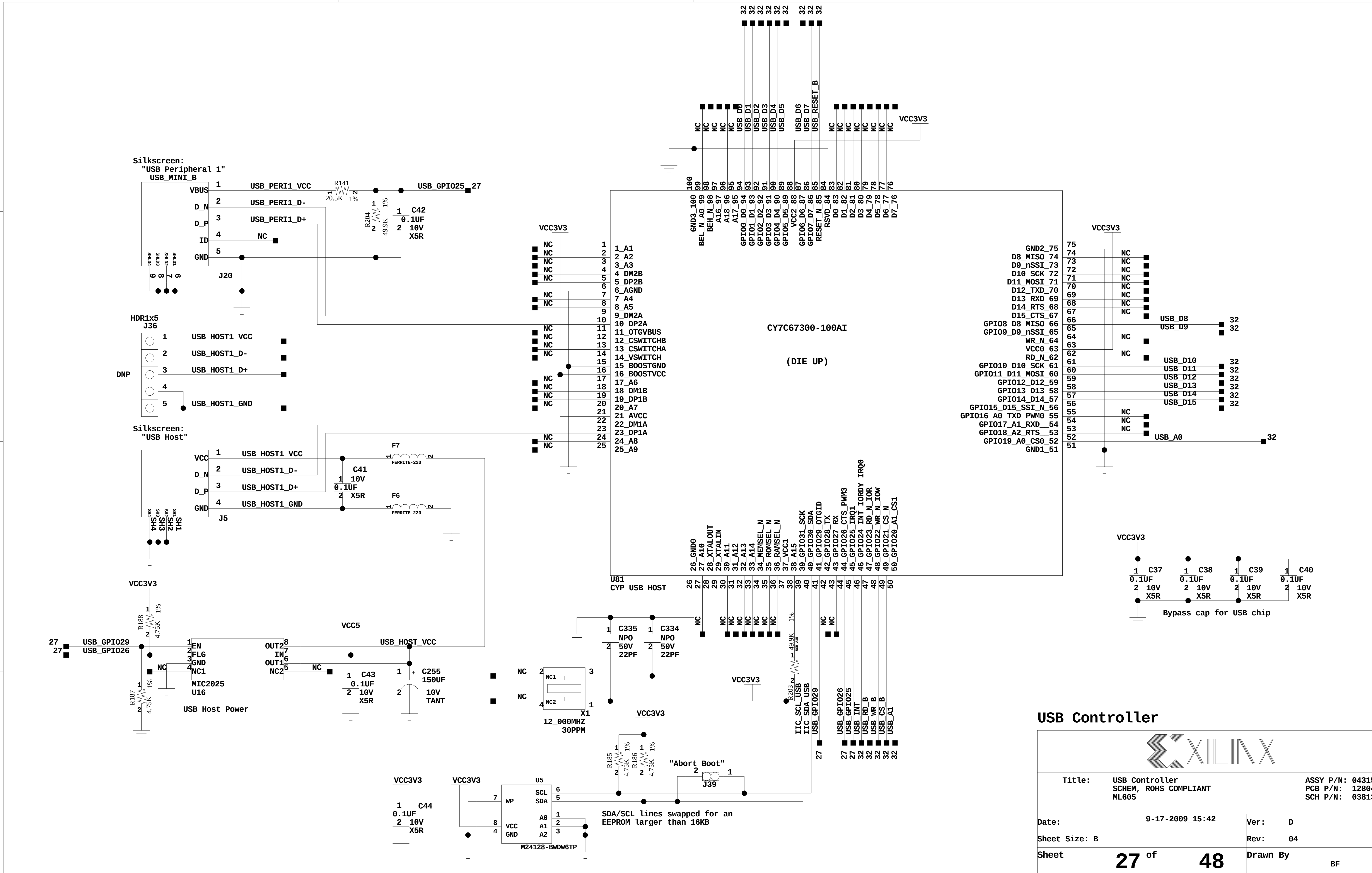
<Cap Value in nF> = ((<DELAY in S>) - (0.5*0.001)) * 175)



BPI FLASH

XILINX

Title:	BPI Flash SCHEM, ROHS COMPLIANT ML605	ASSY P/N: PCB P/N: SCH P/N:	0431540 1280479 0381311
Date:	9-17-2009_15:42	Ver:	D
Sheet Size: B		Rev:	04
Sheet	26 of 48	Drawn By	BF



USB Controller

XILINX

Title: USB Controller
SCHEM, ROHS COMPLIANT
ML605

ASSY P/N: 0431540
PCB P/N: 1280479
SCH P/N: 0381311

Date: 9-17-2009_15:42

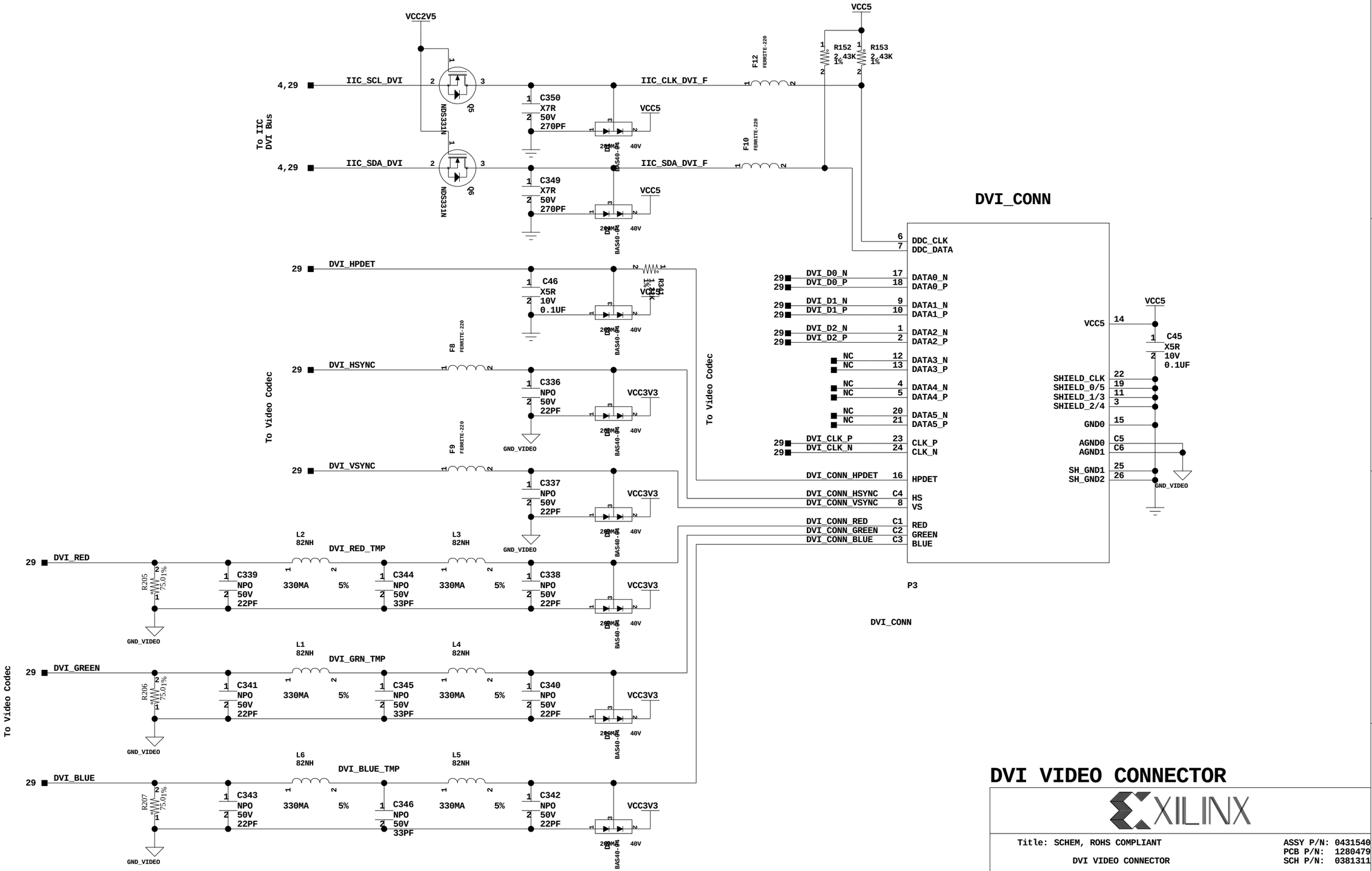
Ver: D

Sheet Size: B

Rev: 04

Sheet 27 of 48

Drawn By BF



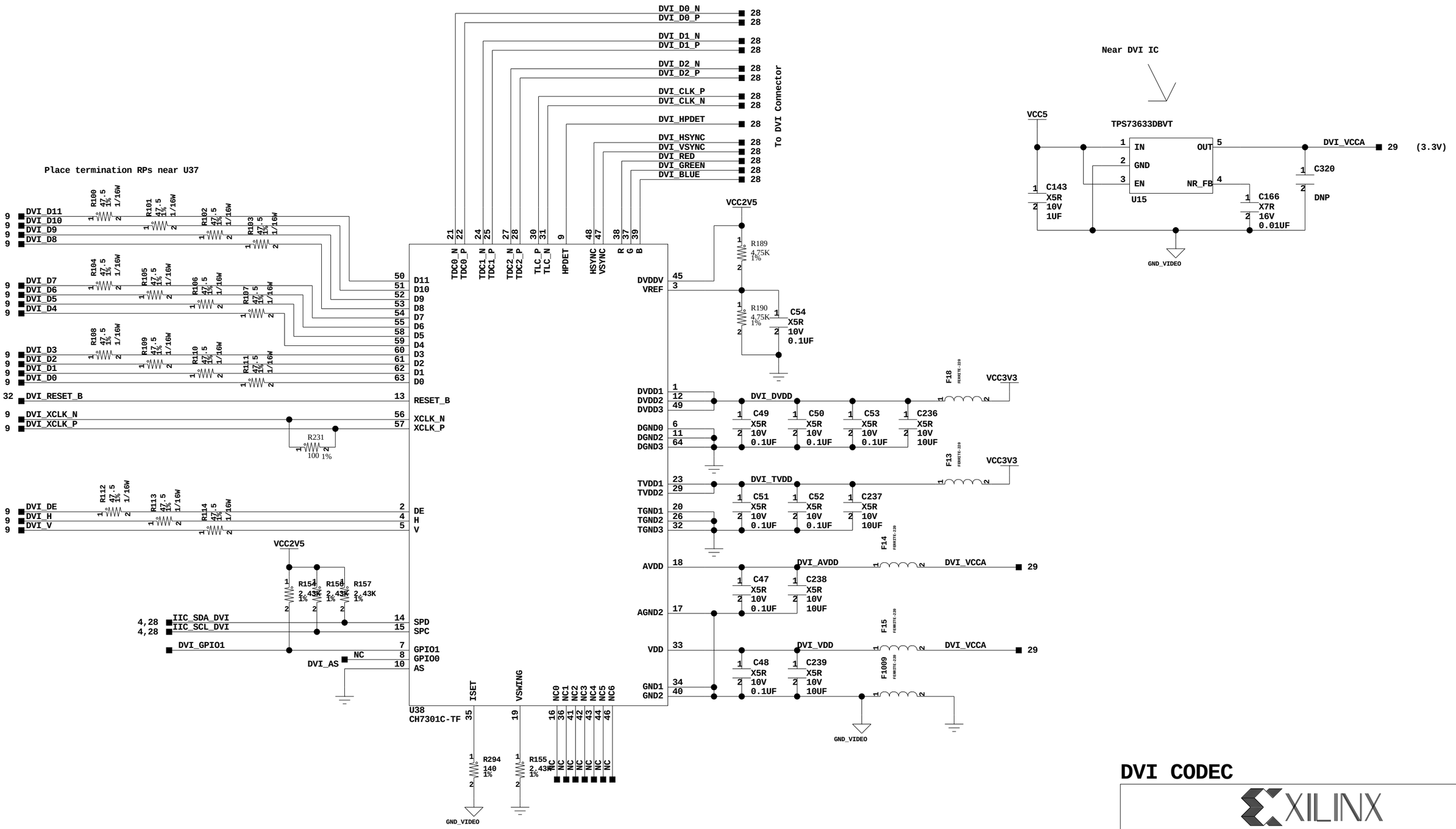
DVI VIDEO CONNECTOR

XILINX

Title: SCHEM, ROHS COMPLIANT
DVI VIDEO CONNECTOR

ASSY P/N: 0431540
PCB P/N: 1280479
SCH P/N: 0381311

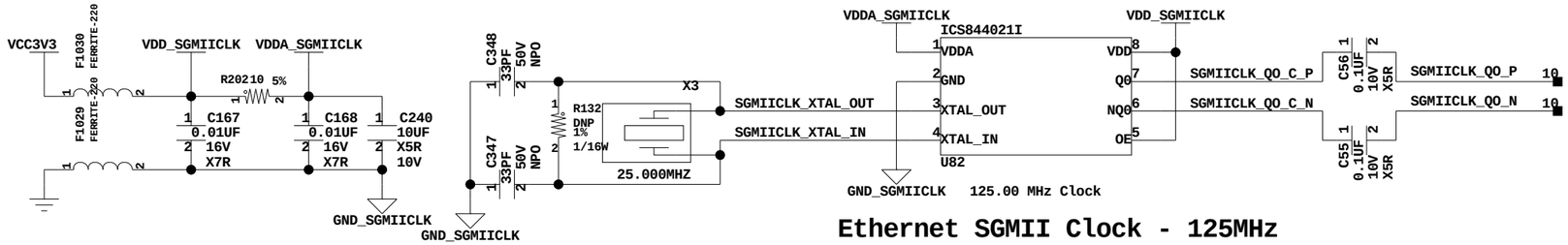
Date:	9-17-2009_15:42	Ver:	D
Sheet Size: B		Rev:	04
Sheet	28 of 48	Drawn By	BF



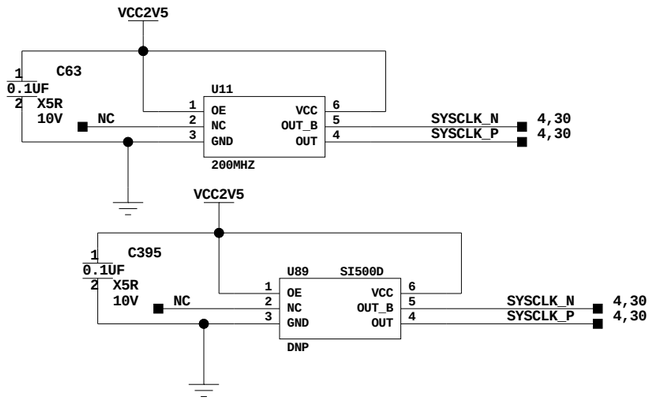
DVI CODEC

XILINX

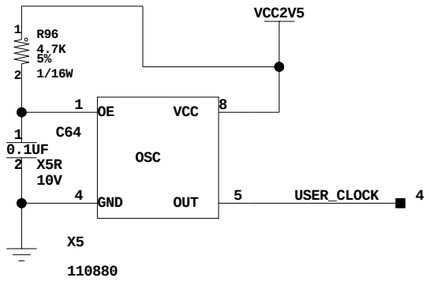
Title:	SCHEM, ROHS COMPLIANT, DVI CODEC	ASSY P/N:	0431540
		PCB P/N:	1280479
		SCH P/N:	0381311
Date:	9-17-2009_15:42	Ver:	D
Sheet Size: B		Rev:	04
Sheet	29 of 48	Drawn By	BF



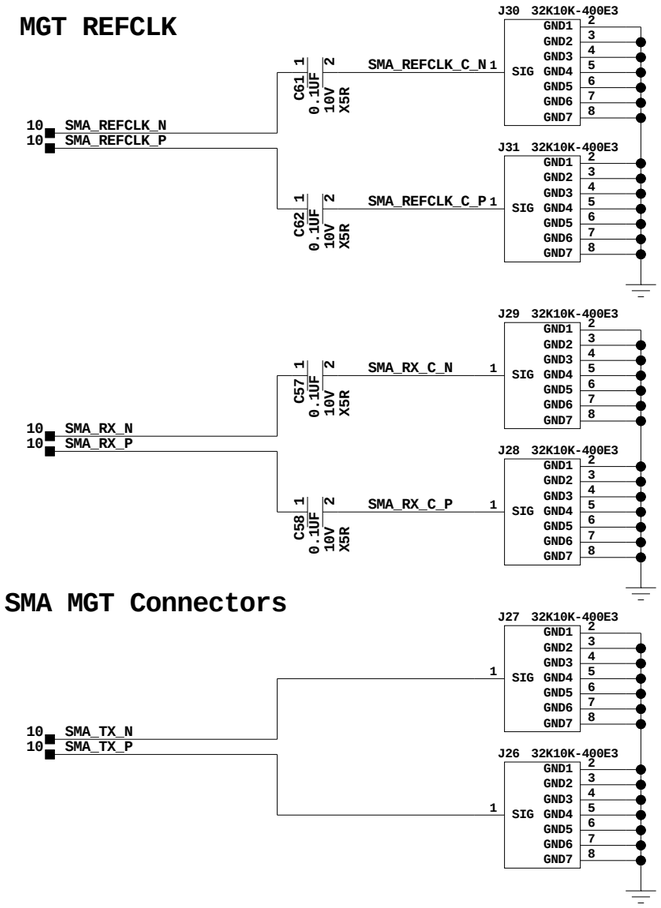
Ethernet SGMII Clock - 125MHz

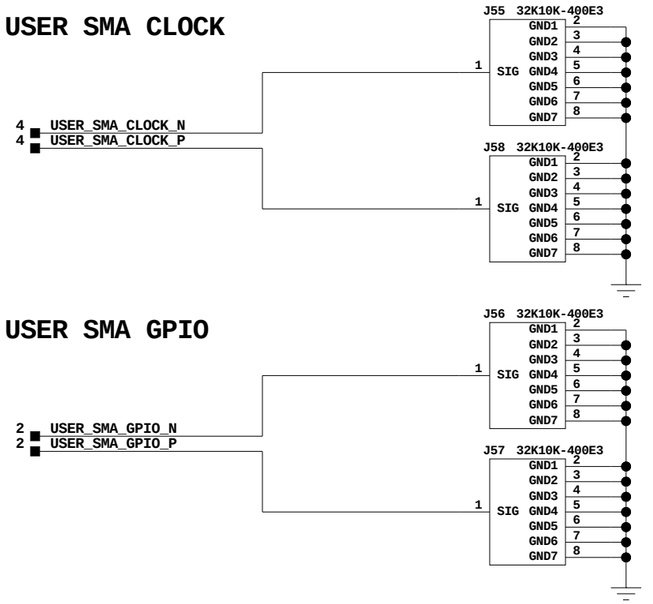


Differential System Clock



Single Ended User Clock

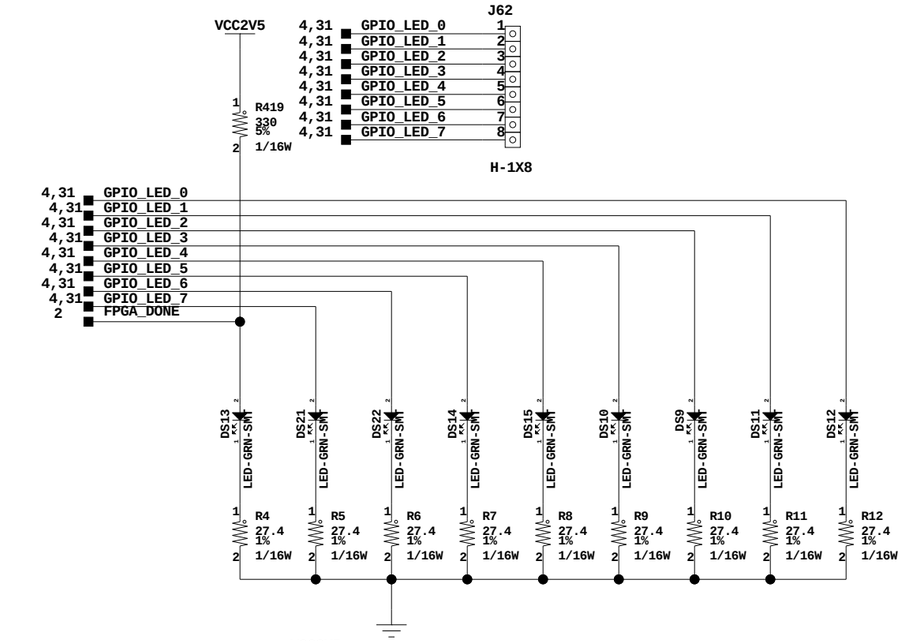


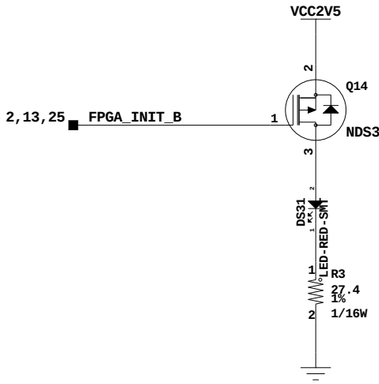


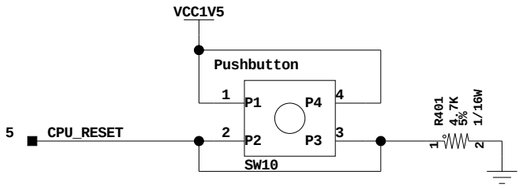
Clocks and MGTs

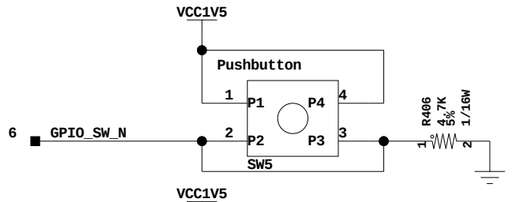
XILINX

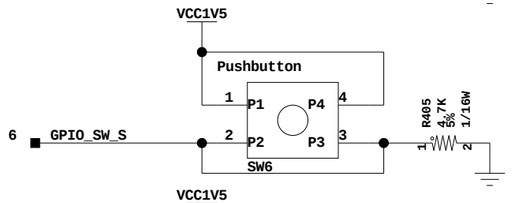
Title:	Clocks and MGTs SCHEM, ROHS COMPLIANT ML605	ASSY P/N: PCB P/N: SCH P/N:	0431540 1280479 0381311
Date:	3-17-2010_8:28	Ver:	D
Sheet Size: B		Rev:	04
Sheet	30 of 48	Drawn By	BF

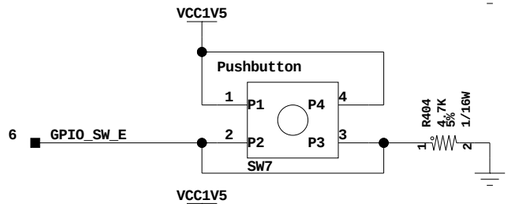


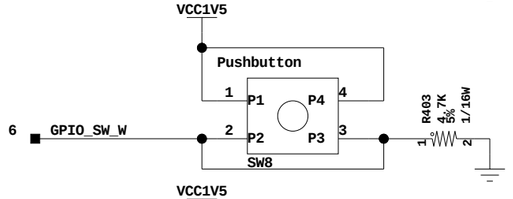


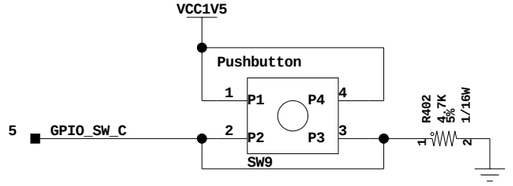


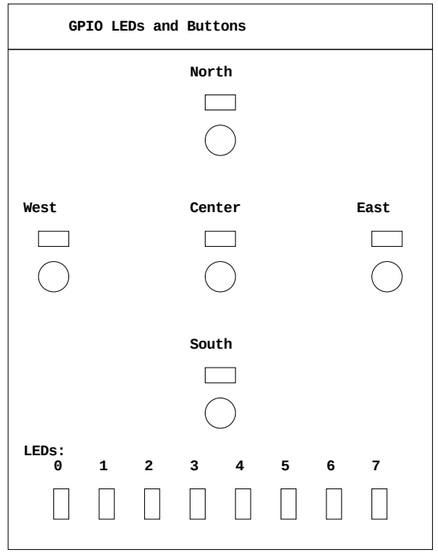


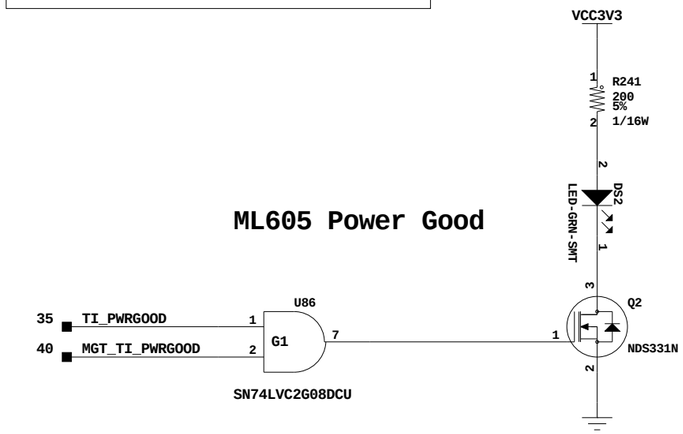




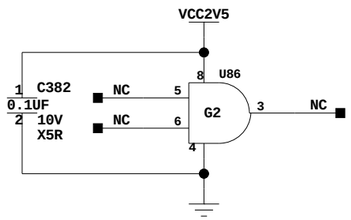


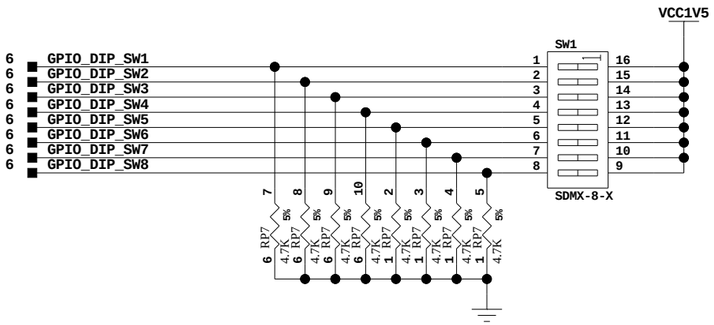


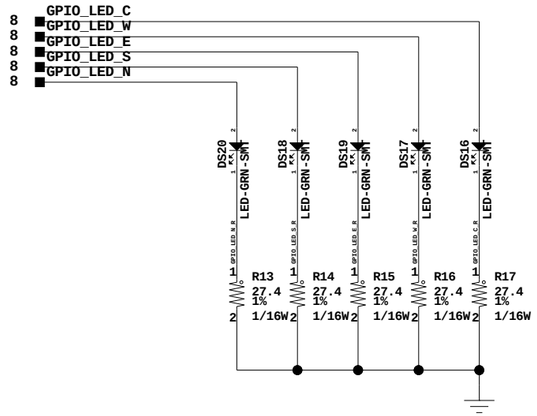




ML605 Power Good



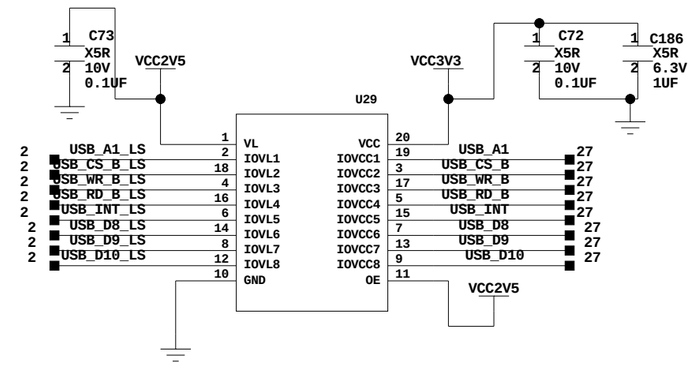


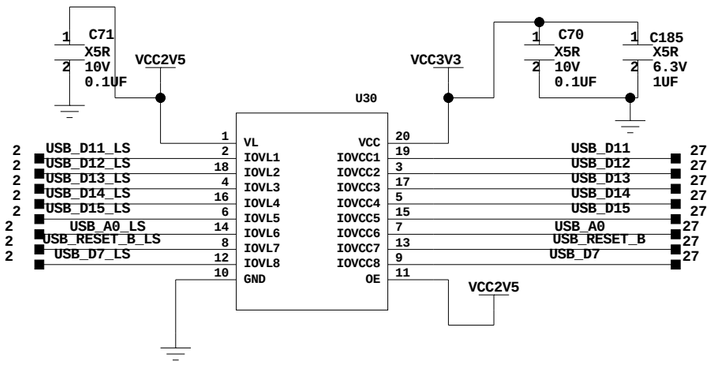


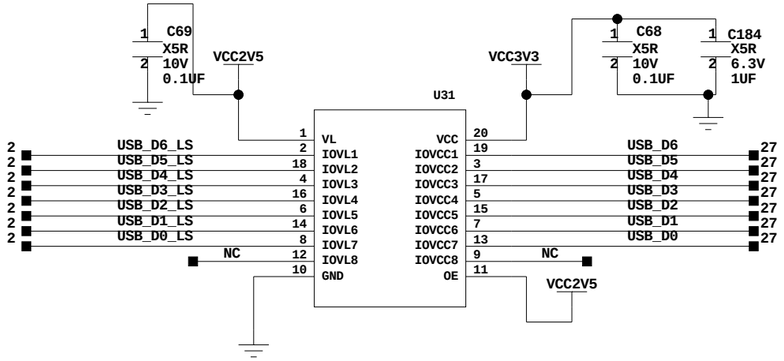
GPIO - Buttons, LEDs, Switches

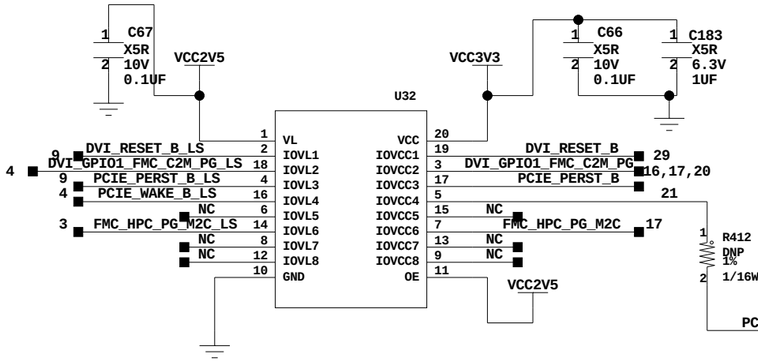
Title:	GPIO Buttons, LEDs, Switches,GPIO SCHEM, ROHS COMPLIANT ML605	ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311	
Date:	3-25-2010_10:38	Ver:	D
Sheet Size: B		Rev:	04
Sheet	31 of 48	Drawn By	BF

3.3V to 2.5V Level Shifters

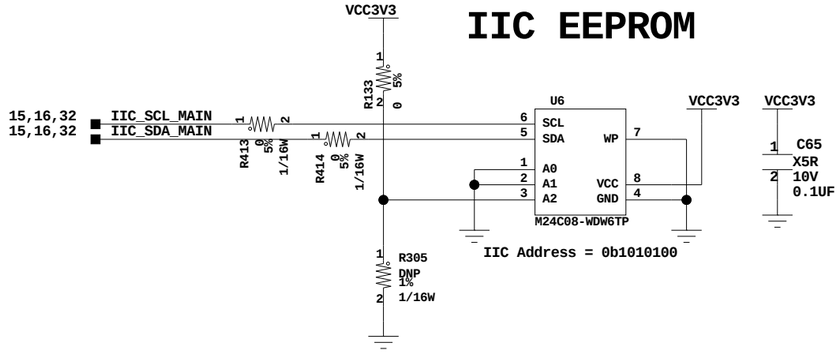


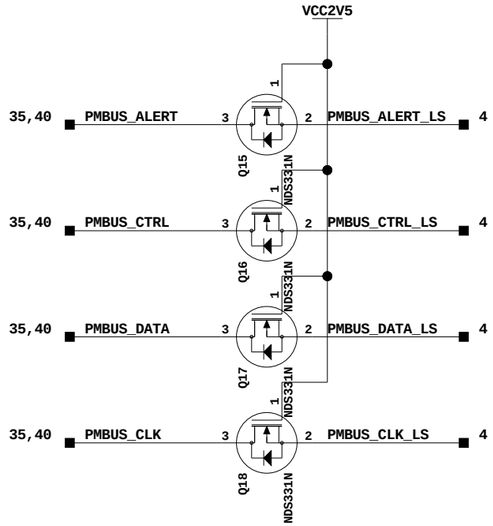


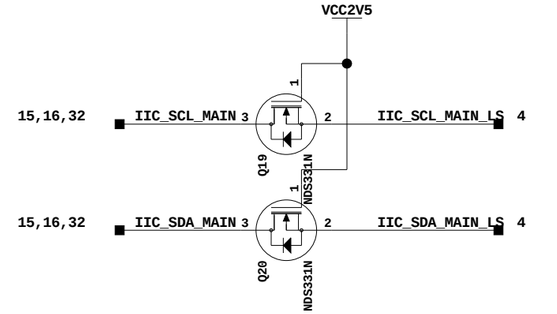


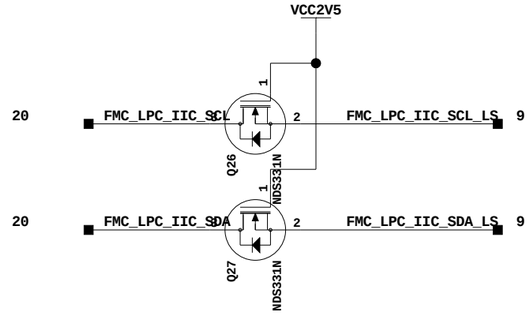


IIC EEPROM









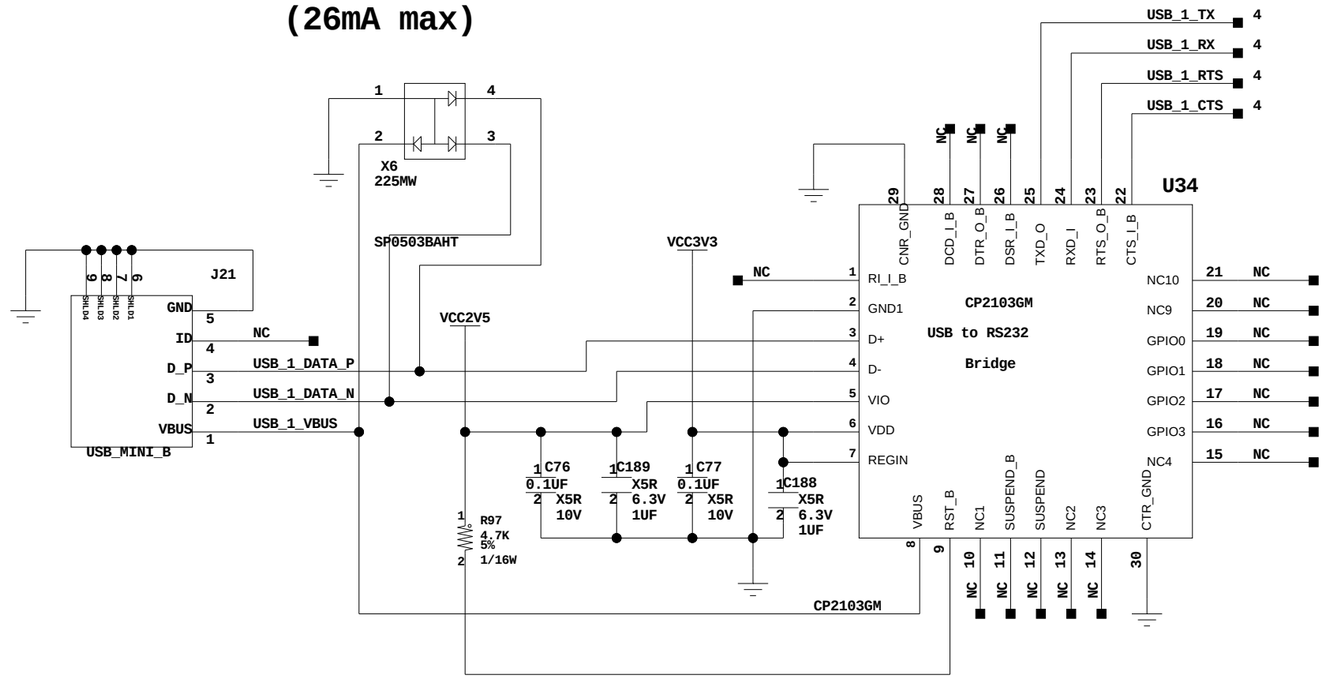
Misc - LCD, Level Shifters

XILINX

Title:	LCD, Level Shifters SCHEM, ROHS COMPLIANT ML605	ASSY P/N:	0431540 PCB P/N: 1280479 SCH P/N: 0381311
Date:	9-24-2009_11:19	Ver:	D
Sheet Size: B		Rev:	04
Sheet	32 of 48	Drawn By	BF

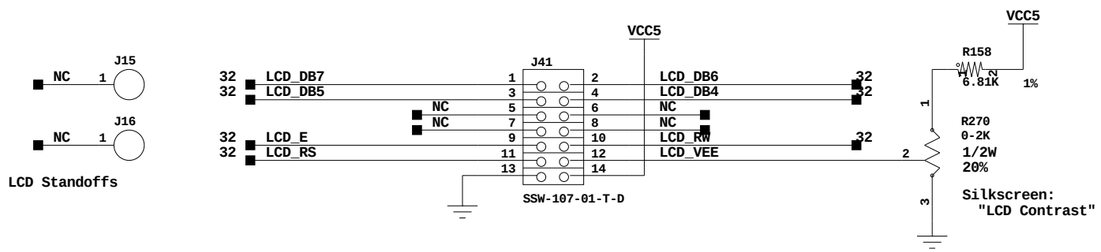
CP2103 USB Self-Powered

(26mA max)



The VIO voltage must match the appropriate bank IO voltage

LCD Header

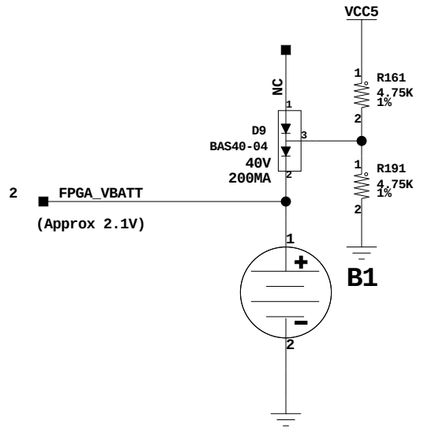


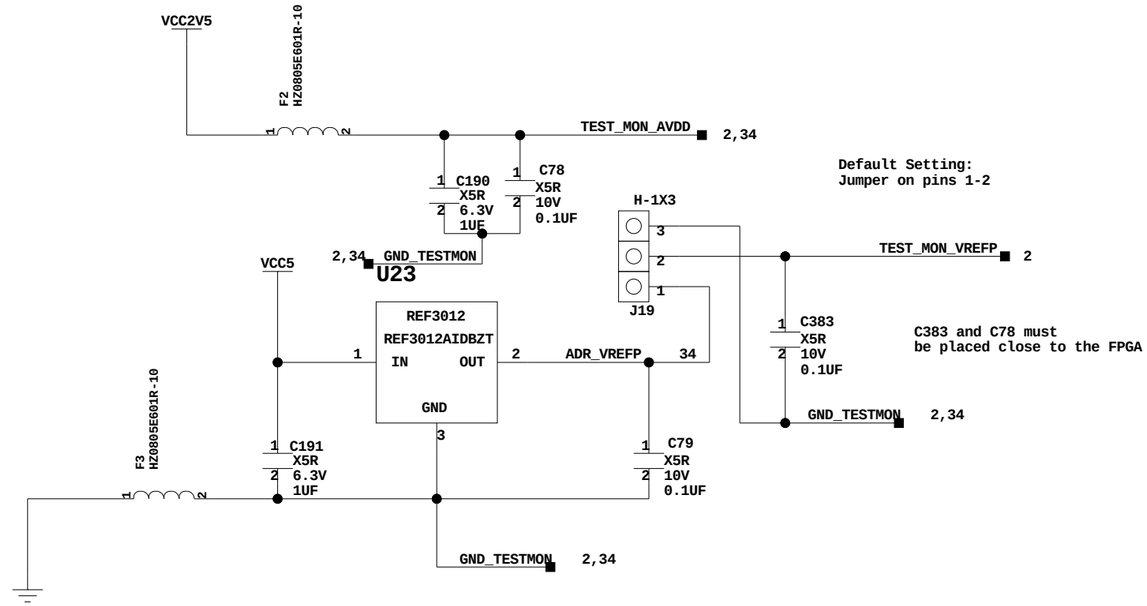
USB UART, LCD Header

XILINX

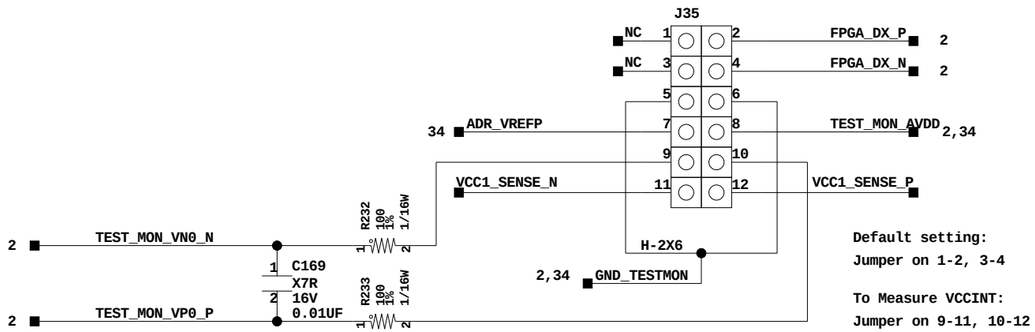
Title: SCHEM, ROHS COMPLIANT, USB UART, LCD HEADER	ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311
Date: 9-17-2009_15:42	Ver: D
Sheet Size: B	Rev: 04
Sheet 33 of 48	Drawn By BF

Rechargeable Battery





System Monitor Header for probing



place 100 ohm resistors and
0.01 cap near FPGA

SYSMON HEADER / AVDD VREFP SUPPLY / Battery

XILINX

Title:	SCHEM, ROHS COMPLIANT, SYSMON HEADER / AVDD VREFP SUPPLY / BATTERY	ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311	
Date:	9-17-2009_15:42	Ver:	D
Sheet Size: B		Rev:	04
Sheet	34 of 48	Drawn By	BF

PMBus Address is calculated as follows:

PMBus Address = 12 × Value(ADDRSEN1) + Value(ADDRSEN0)

Example: ADDRSEN1 R=27.4k and ADDRSEN0 R=27.4k

PMBus Address = (12 x 4) + 4 = 52 decimal

ADDRSENx Value	RPMBus
Open	-
11	210k
10	158k
9	115k
8	84.5k
7	63.4k
6	47.5k
5	36.5k
4	27.4k
3	21.5k
2	16.9k
1	13.0k
0	10.2k
Short	-

Note:

Do not use PMBus Addresses 0, 1, 2, 3, 12, 126 or 127

VCCxxxx_EAP/N are remote sense pairs wired back from power plane connections at FPGA

PMBus Connector

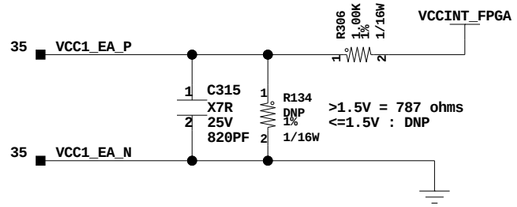
AGND should be a copper island underneath the 9240 and every associated module

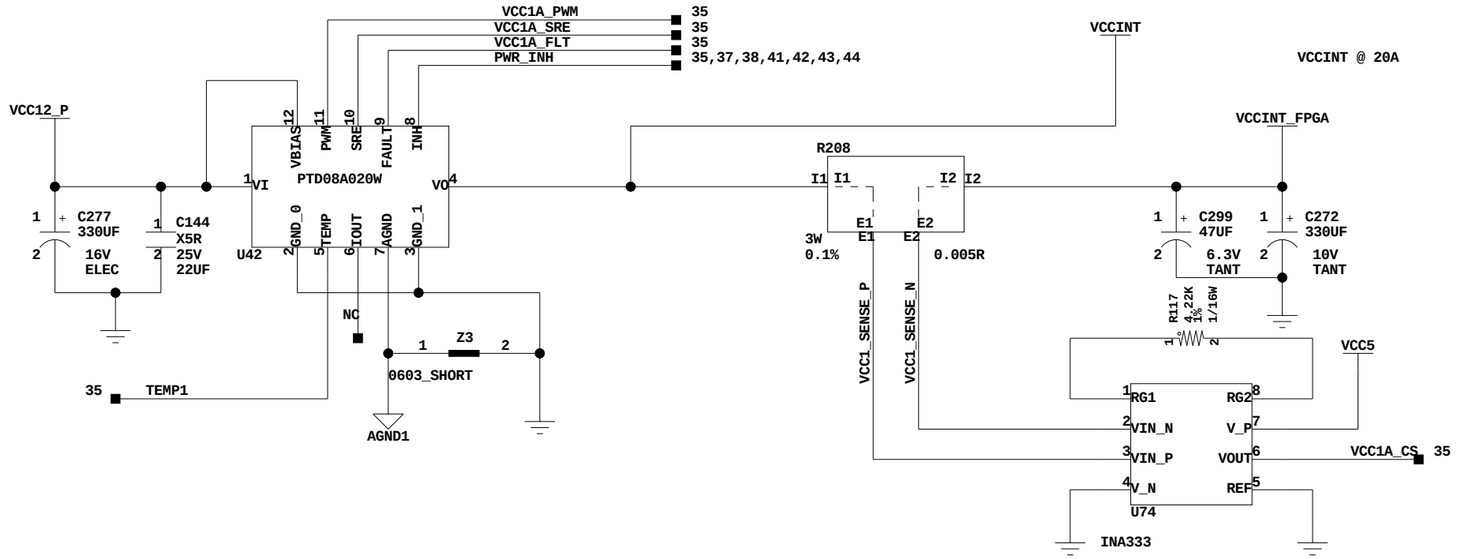
FPGA PMBus Regulator Shutdown (shuts off regulators)

FPGA UCD9240 PMBus Controller

XILINX

Title:	SCHEM, ROHS COMPLIANT TI UCD9240 Power System	ASSY P/N:	0431540
		PCB P/N:	1280479
		SCH P/N:	0381311
Date:	9-24-2009_11:19	Ver:	D
Sheet Size: B		Rev:	04
Sheet	35 of 48	Drawn By	BF

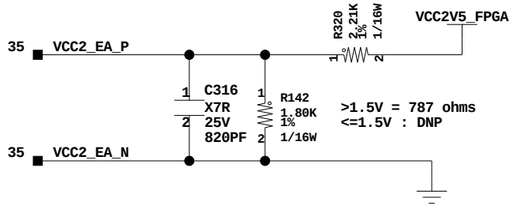


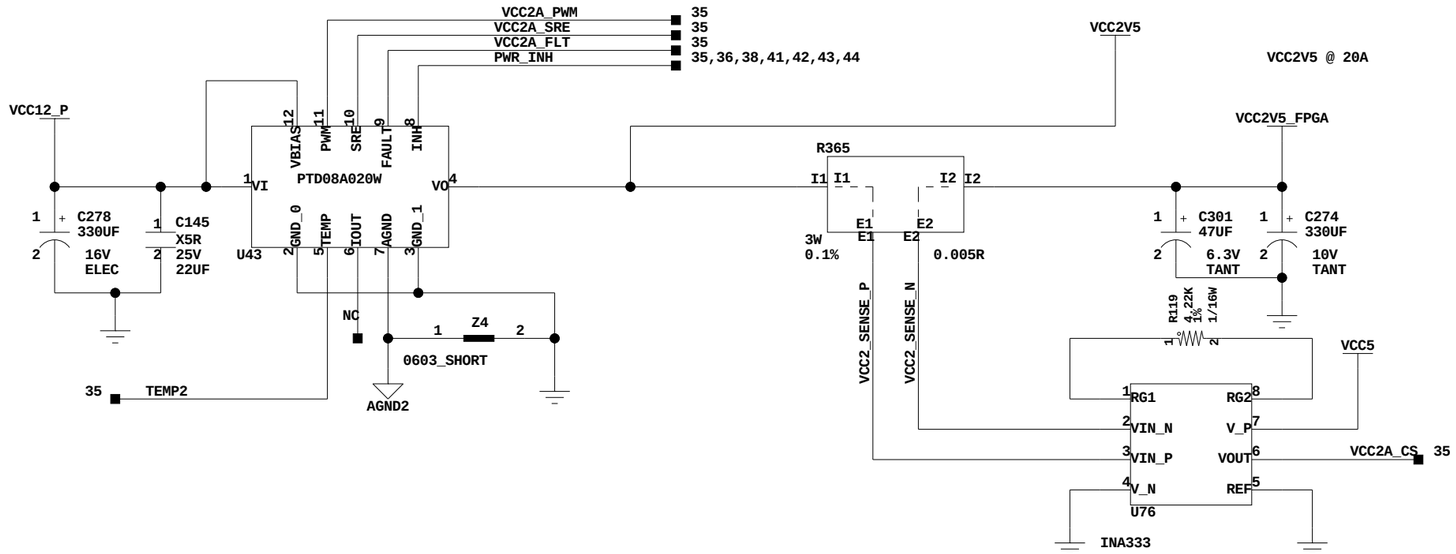


PTD08A020W 20A Max. Power Channel

XILINX

Title:	SCHEM, ROHS COMPLIANT PTD08A020W 20A Max. Power Channel	ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311	
Date:	9-17-2009_15:42	Ver:	D
Sheet Size: B		Rev:	04
Sheet	36 of 48	Drawn By	BF

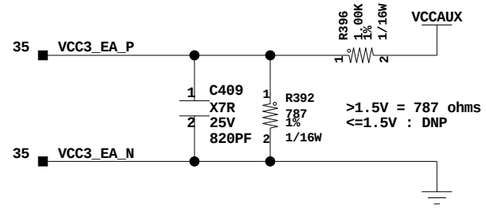


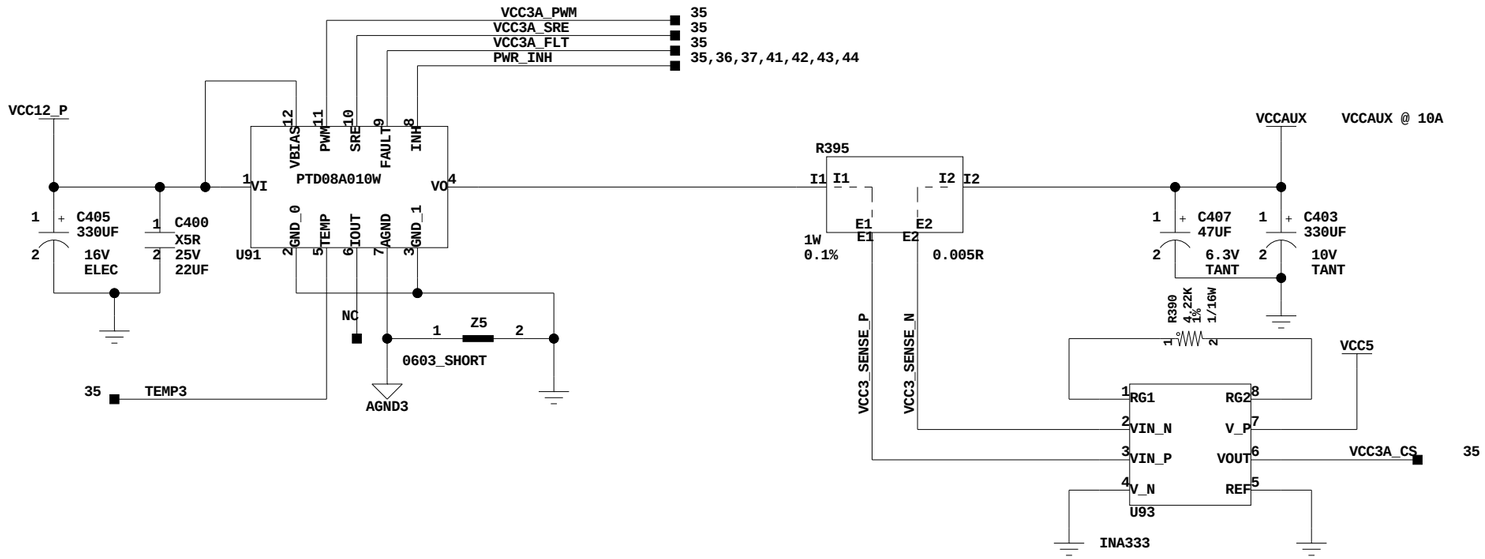


PTD08A020W 20A Max. Power Channel

XILINX

Title:	SCHEM, ROHS COMPLIANT PTD08A020W 20A Max. Power Channel	ASSY P/N: PCB P/N: SCH P/N:	0431540 1280479 0381311
Date:	9-17-2009_15:42	Ver:	D
Sheet Size: B		Rev:	04
Sheet	37 of 48	Drawn By	BF

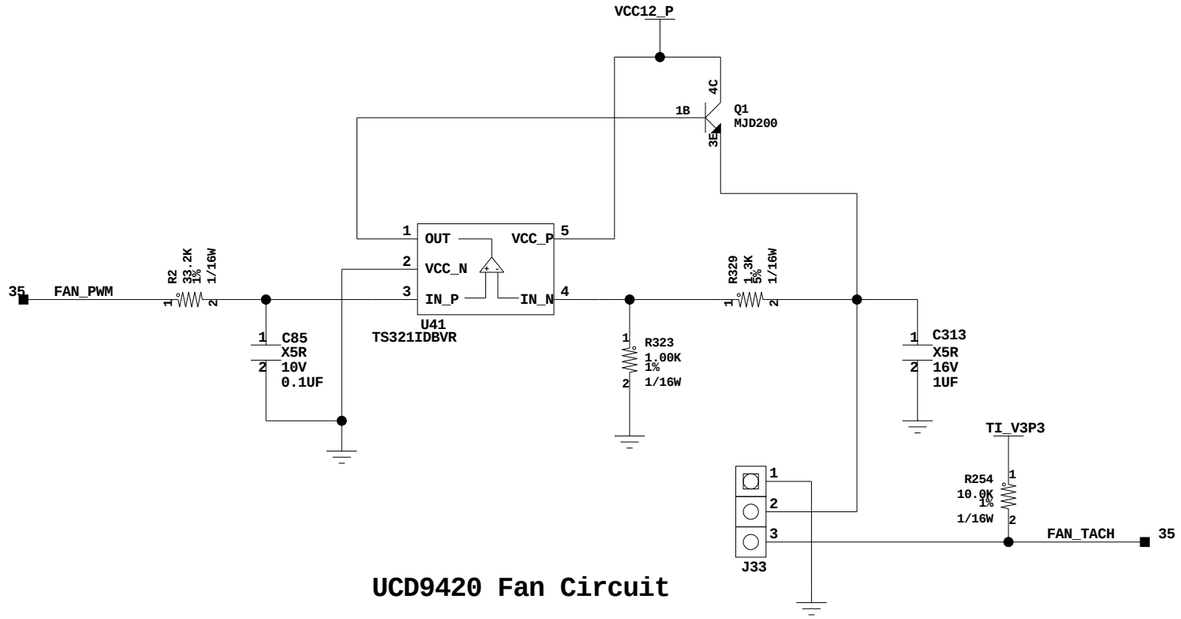




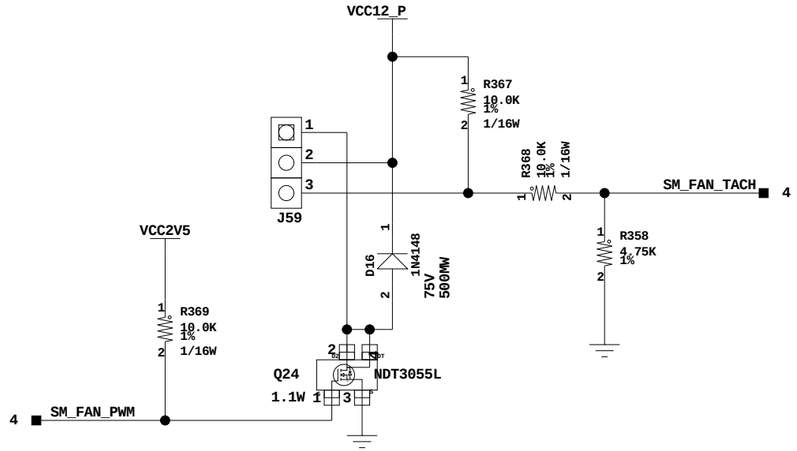
PTD08A010W 10A Max. Power Channel

XILINX

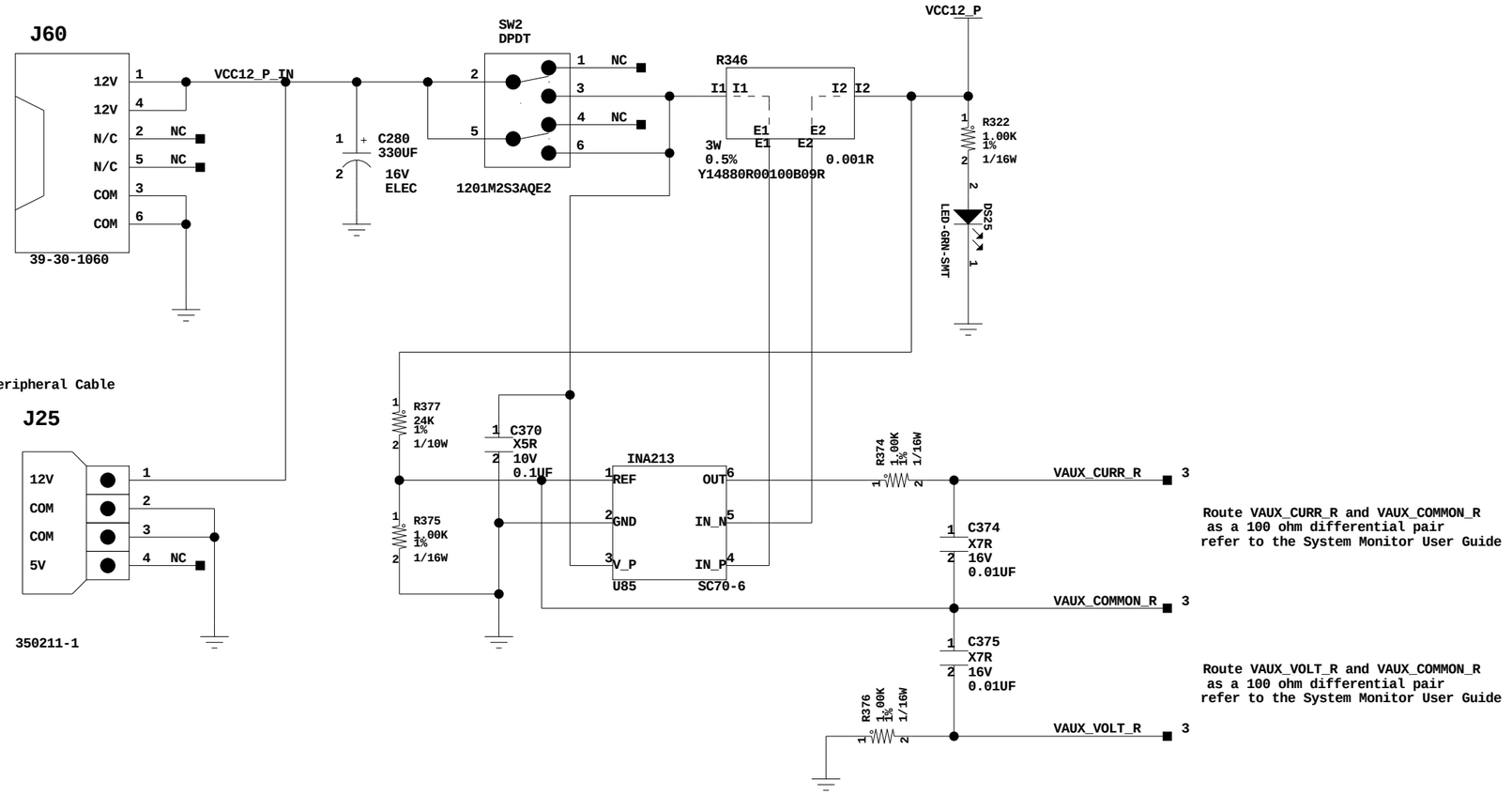
Title:	SCHEM, ROHS COMPLIANT PTD08A010W 10A Max. Power Channel	ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311	
Date:	9-17-2009_15:42	Ver:	D
Sheet Size: B		Rev:	04
Sheet	38 of 48	Drawn By	BF



UCD9420 Fan Circuit



System Monitor Fan Circuit



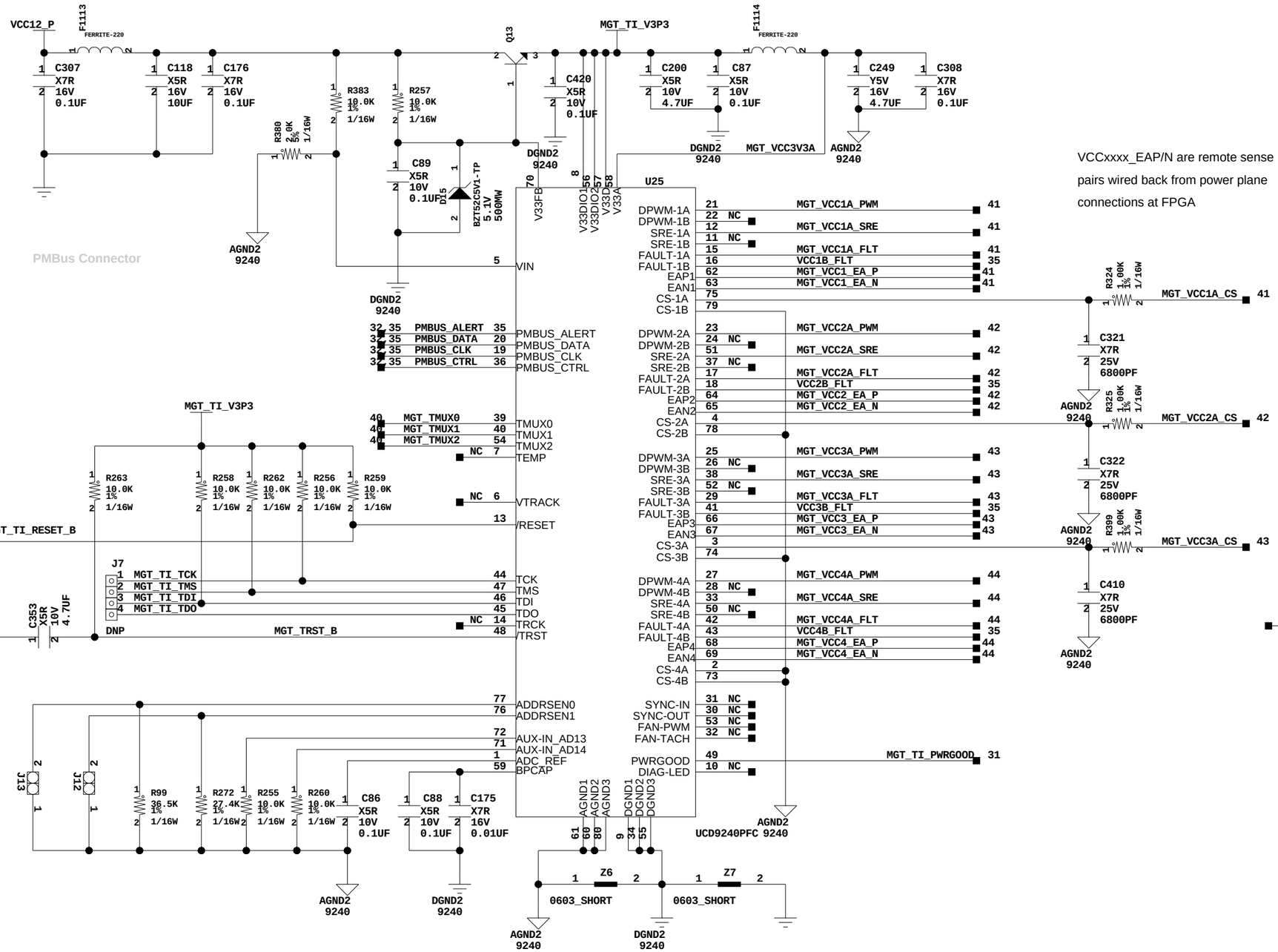
Route VAUX_CURR_R and VAUX_COMMON_R as a 100 ohm differential pair refer to the System Monitor User Guide

Route VAUX_VOLT_R and VAUX_COMMON_R as a 100 ohm differential pair refer to the System Monitor User Guide

12V Power Jacks, 12V Fan

XILINX

Title:	SCHEM, ROHS COMPLIANT TI UCD9240 Power System	ASSY P/N:	0431540
		PCB P/N:	1280479
		SCH P/N:	0381311
Date:	10-14-2009_14:48	Ver:	D
Sheet Size: B		Rev:	04
Sheet	39 of 48	Drawn By	BF



VCCxxxx_EAP/N are remote sense pairs wired back from power plane connections at FPGA

PMBus Address is calculated as follows:

PMBus Address = 12 × Value(ADDRSEN1) + Value(ADDRSEN0)

Example: ADDRSEN1 R=27.4k and ADDRSEN0 R=27.4k

PMBus Address = (12 x 4) + 4 = 52 decimal

ADDRSENx Value	RPMBus
Open	-
11	210k
10	158k
9	115k
8	84.5k
7	63.4k
6	47.5k
5	36.5k
4	27.4k
3	21.5k
2	16.9k
1	13.0k
0	10.2k
Short	-

Note:

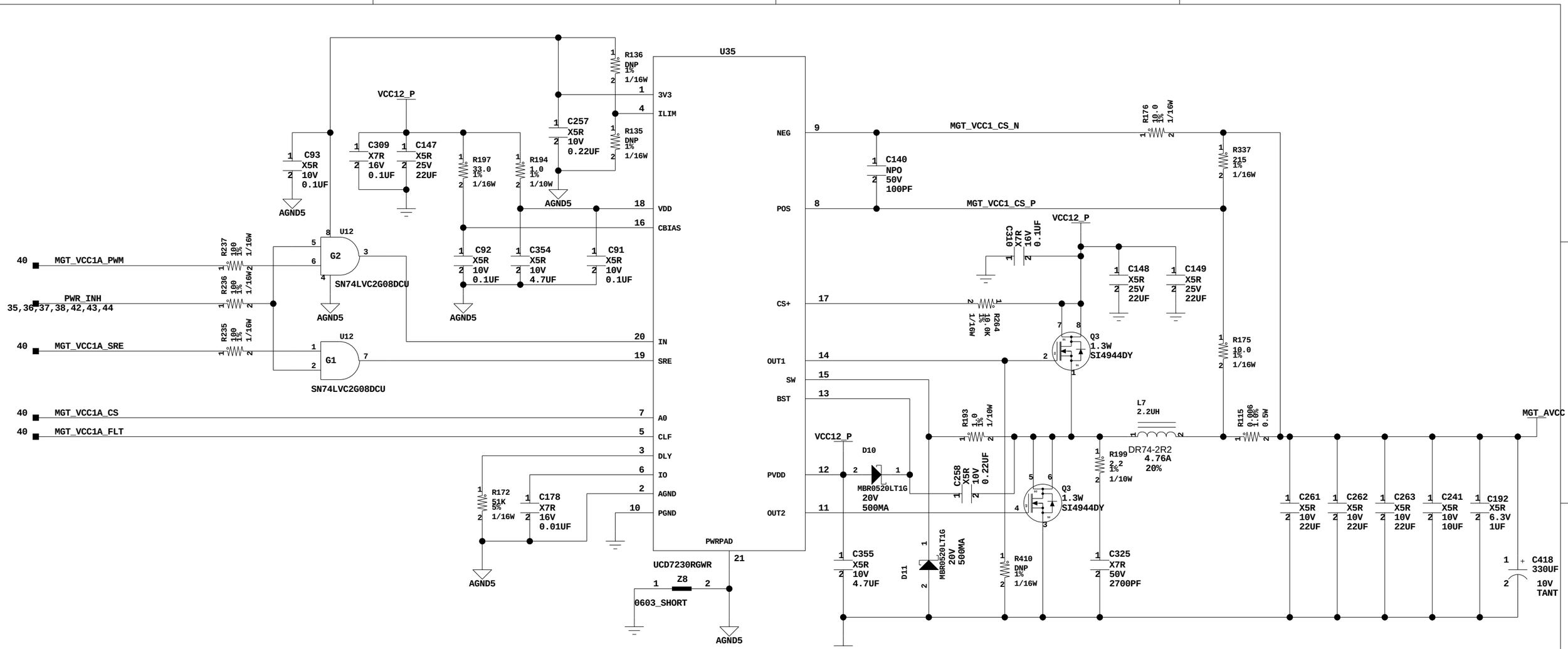
Do not use PMBus Addresses 0, 1, 2, 3, 12, 126 or 127

AGND should be a copper island underneath the 9240 and every associated module

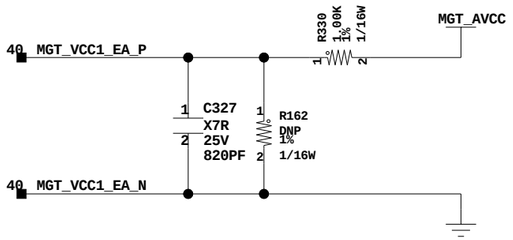
FPGA UCD9240 PMBus Controller

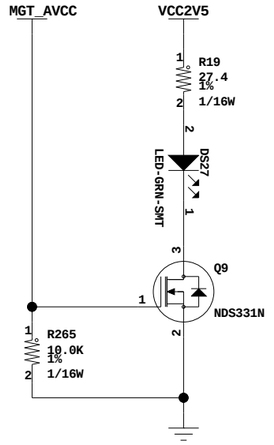
XILINX

Title:	SCHEM, ROHS COMPLIANT TI UCD9240 Power System	ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311	
Date:	9-24-2009_11:19	Ver:	D
Sheet Size: B		Rev:	04
Sheet	40 of 48	Drawn By	BF



Local AGND to be tied to local GND
See UCD7230 datasheet layout recommendations

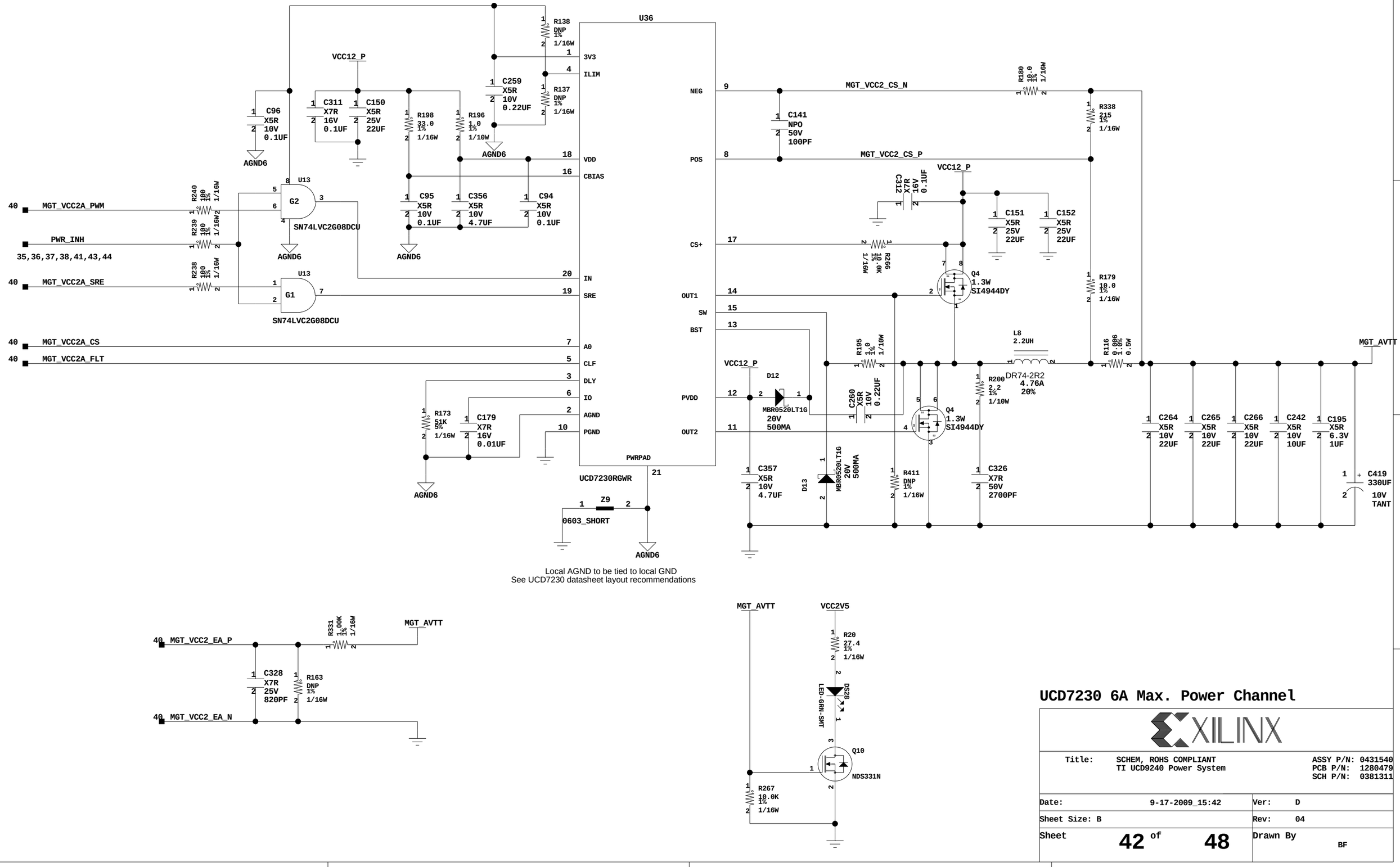




UCD7230 6A Max. Power Channel

XILINX

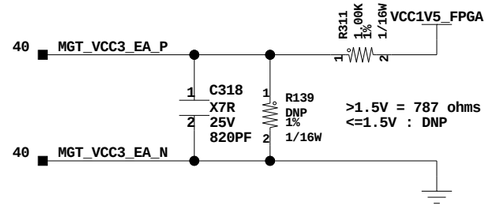
Title:	SCHEM, ROHS COMPLIANT TI UCD9240/UCD7230 Power System	ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311	
Date:	9-17-2009_15:42	Ver:	D
Sheet Size: B		Rev:	04
Sheet	41 of 48	Drawn By	BF

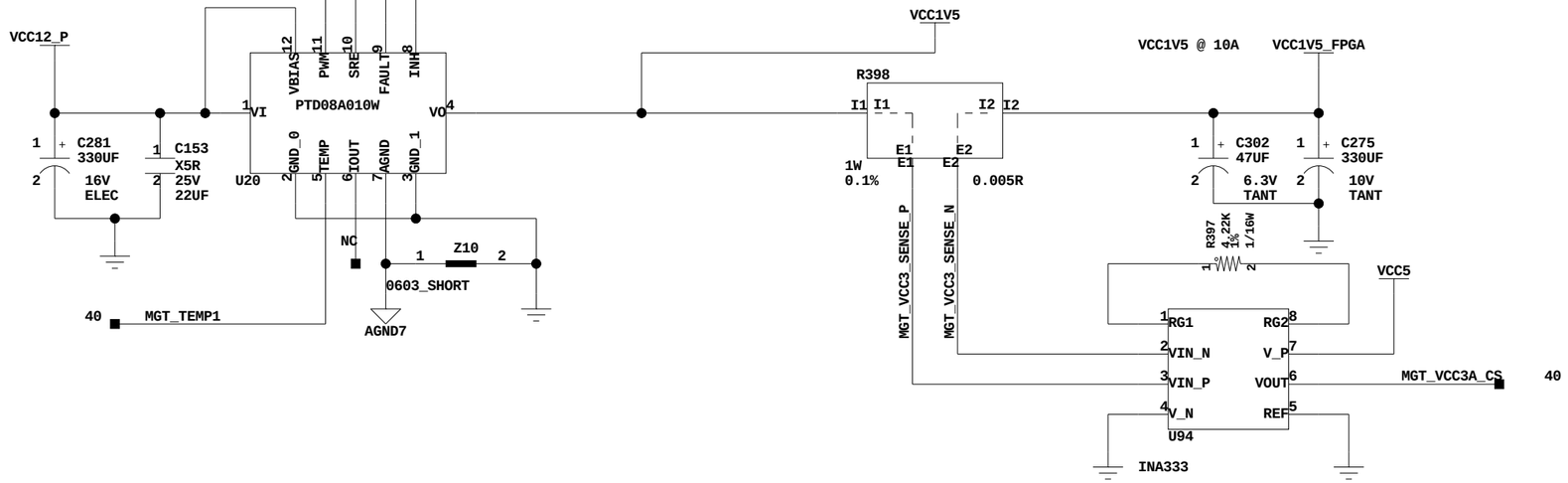


UCD7230 6A Max. Power Channel

XILINX

Title:	SCHEM, ROHS COMPLIANT TI UCD9240 Power System	ASSY P/N: 0431540 PCB P/N: 1280479 SCH P/N: 0381311	
Date:	9-17-2009_15:42	Ver:	D
Sheet Size: B		Rev:	04
Sheet	42 of 48	Drawn By	BF

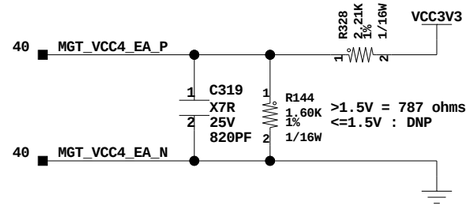


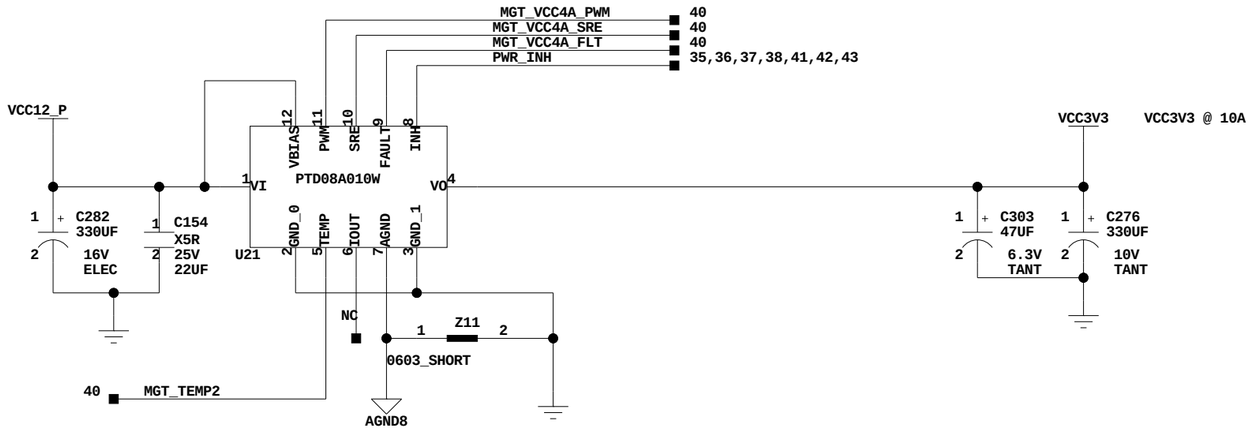


PTD08A010W 10A Max. Power Channel

XILINX

Title:	SCHEM, ROHS COMPLIANT PTD08A010W 10A Max. Power Channel	ASSY P/N: PCB P/N: SCH P/N:	0431540 1280479 0381311
Date:	9-17-2009_15:42	Ver:	D
Sheet Size: B		Rev:	04
Sheet	43 of 48	Drawn By	BF

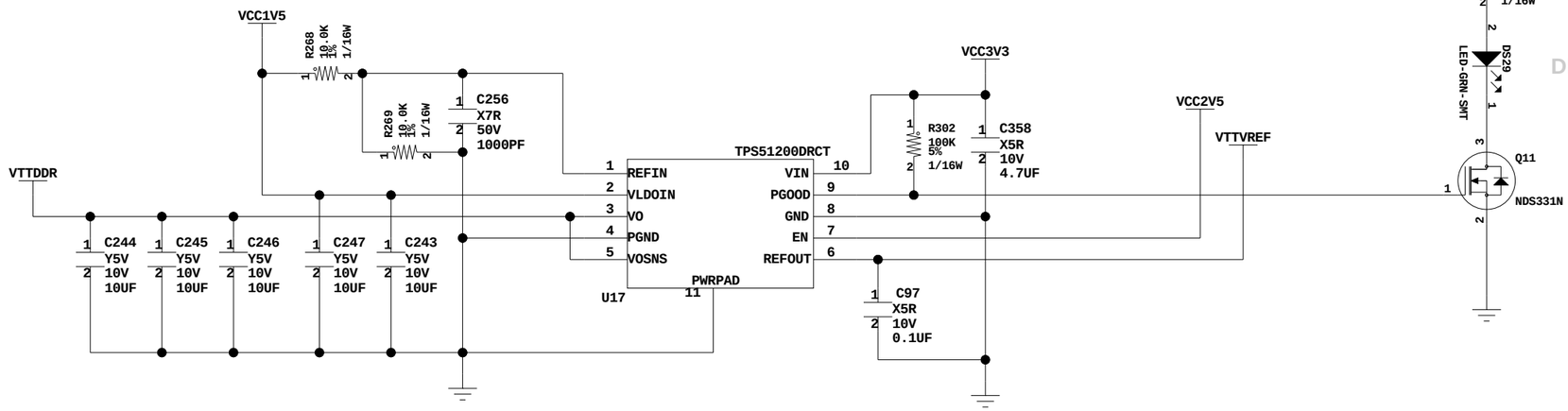




PTD08A010W 10A Max. Power Channel

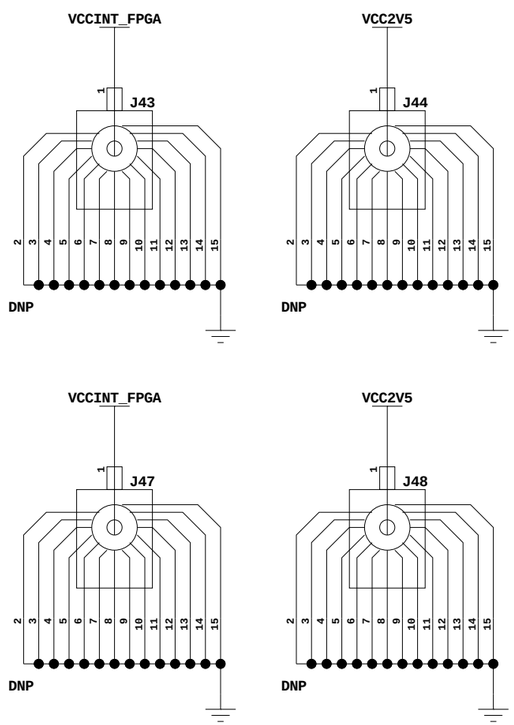
XILINX

Title:	SCHEM, ROHS COMPLIANT PTD08A010W 10A Max. Power Channel	ASSY P/N: PCB P/N: SCH P/N:	0431540 1280479 0381311
Date:	9-17-2009_15:42	Ver:	D
Sheet Size: B		Rev:	04
Sheet	44 of 48	Drawn By	BF

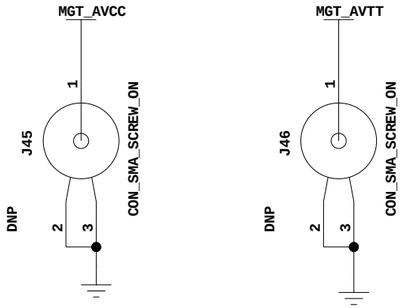


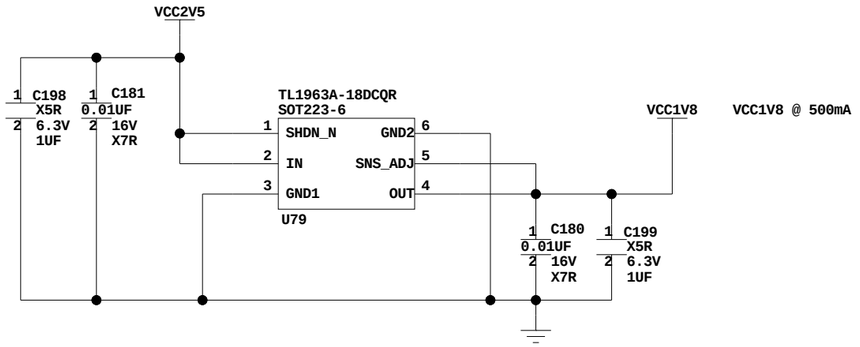
DDR3 Power Good

VCCINT_FPGA, VCCAUX Power Probe Channels



MGT Power Probe Channels





DDR3 Termination Regulator, power probes

XILINX

Title:	SCHEM, ROHS COMPLIANT DDR3 Termination Regulator	ASSY P/N: PCB P/N: SCH P/N:	0431540 1280479 0381311
Date:	9-17-2009_15:42	Ver:	D
Sheet Size: B		Rev:	04
Sheet	45 of 48	Drawn By	BF

The Embedded USB JTAG Download circuit on this page is for reference only!
This circuit should not be designed into an end customer product or solution.
Xilinx will not provide support on this embedded USB JTAG Download circuit.

U26

PART_NUMBER=CY7C68013A
TQFP100

USB CONTROLLER

U22

PART_NUMBER=XC2C256
VQFP100

PARALLEL TO SERIAL CONVERTER

USB CONNECTOR

USB TYPE B RECEPTACLE

NOTE: EMBEDDED VERSION IS NOT BUS POWERED

TARGET INTERFACE CONNNECTIONS	
FROM	TO JTAG
FPGA_TCK	TCK ALL DEVICES
FPGA_TMS	TMS ALL DEVICES
USB_HEADER_TDI	FIRST DEVICE TDI
JTAG_TDO	LAST DEVICE TDO
EMBEDDED_INIT	NO CONNECTION

3.3V INTERFACE TO LOCAL JTAG OR SLAVE-SERIAL DEVICE CHAIN.
FOR LONG CHAINS OR TRACES, DISTRIBUTE EMBEDDED_TCK
AND EMBEDDED_TMS WITH LVDS BUFFERS.

LEGEND:

- (K1) OPTIONAL NETS ROUTED IN PARALLEL TO LOCAL 2MM CABEL CONNECTOR J1.
- COMPONENTS TO BE LOADED FOR THE PRODUCTION ASSEMBLY VERSION ONLY.
- OPTIONAL COMPONENTS THAT SUPPORT DEBUG AND/OR DIAGNOSTICS.

NOTE:

MAKE PARALLEL CONNECTIONS TO J1 (OPTION B) AT EACH OF THE NETS MARKED (K1) TO FACILITATE FASTER IN-CIRCUIT RE-PROGRAMMING OF THE CPLD DURING BOARD TEST.
J1 DOES NOT NEED TO BE POPULATED DURING PRODUCTION, BUT THE ASSEMBLY FOOTPRINT IS RECOMMENDED FOR THE PWB LAYOUT.

Embedded USB JTAG: USB Controller, CPLD

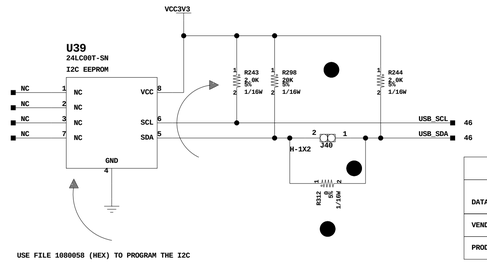
ASSY P/N: 0431540
PCB P/N: 1280479
SCH P/N: 0381311

Drawing Number: 0381242	
Date: 14-JUNE-2006	Ver: B
Sheet Size: D	Rev: 04
Sheet 46 of 48	Drawn By SCHWEIGLER

LAST REVISION: 9-24-2009_11:19

The Embedded USB JTAG Download circuit on this page is for reference only!
This circuit should not be designed into an end customer product or solution.
Xilinx will not provide support on this embedded USB JTAG Download circuit.

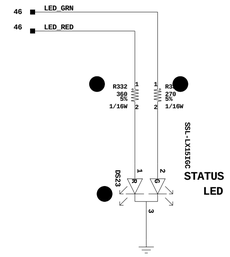
DEFAULT PID/VID EEPROM



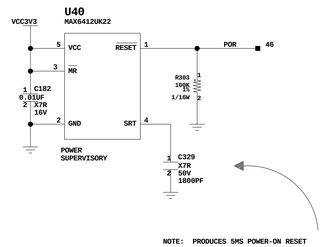
USE FILE 1080058 (HEX) TO PROGRAM THE I2C PROM PRIOR TO ASSEMBLY.

LOW POWER BOOT CONDITIONS		
DATA FIELD	CYPRESS DEFAULT	XILINX EMBEDDED
VENDOR ID	0x004B4	0x03FD
PRODUCT ID	0x8613	0x000D

STATUS LEDS (OPTION A)

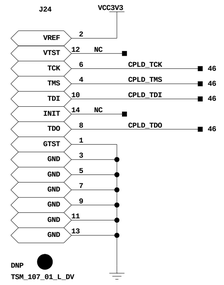


POWER-ON RESET

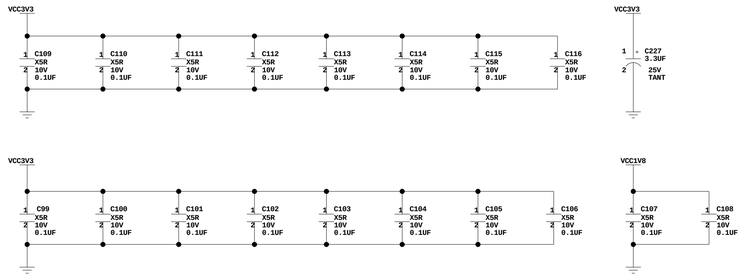


NOTE: PRODUCES 5MS POWER-ON RESET

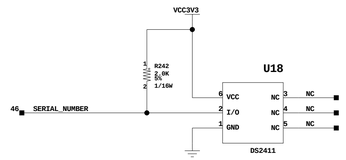
PC4 JTAG CONNECTOR (OPTION B)



BYPASS CAPACITORS



ELECTRONIC SERIAL NUMBER



Embedded USB JTAG: IIC, POR, Decoupling, LED, JTAG Header, Serial Number

ASSY P/N: 0431540
PCB P/N: 1280479
SCH P/N: 0381311

Drawing Number: 0381242	
Date: 14-JUNE-2006	Ver: B
Sheet Size: D	Rev: 04
Sheet 47 of 48	Drawn By SCHWEIGLER

LAST REVISION: 9-24-2009_11:19

MS1

MACHINE_SCREW_SS_PHILHD_4-40_X_3-8

MS5

MACHINE_SCREW_SS_PHILHD_4-40_X_3-8

MS4

MACHINE_SCREW_SS_PHILHD_4-40_X_3-8

MS2

MACHINE_SCREW_SS_PHILHD_4-40_X_3-8

MS3

MACHINE_SCREW_SS_PHILHD_4-40_X_3-8

MN1

NUT_SS_4-40

MN5

NUT_SS_4-40

MN3

NUT_SS_4-40

MN2

NUT_SS_4-40

MN4

NUT_SS_4-40

MSO2

MSO5

MSO3

MSO1

MSO4

MRB3

RUBBER_BUMPER

MRB5

RUBBER_BUMPER

MRB2

RUBBER_BUMPER

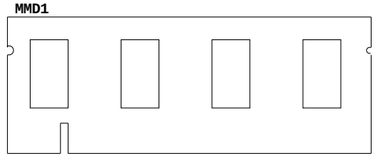
MRB1

RUBBER_BUMPER

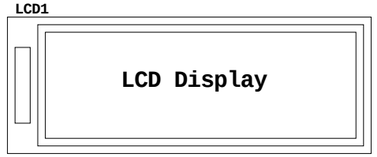
MRB4

RUBBER_BUMPER

MMD1



LCD1

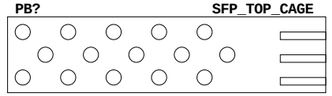


PB1

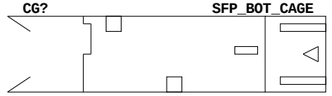
CBL1

Power Cord

PB?



CG?



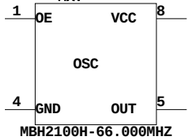
MN?

WASHER

MS?

1ZB34

MX?



MBH2100H-66.000MHZ

MH1 MH_125_250 1

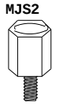
MH2 MH_125_250 1

MH3 MH_125_250 1

MH4 MH_125_250 1

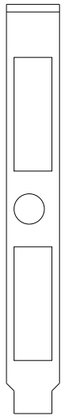
MH6 MH_125_250 1

MJS2



MJS1

PL1



MJB1

JUMPER_BLOCK_2-PIN

MJB3

JUMPER_BLOCK_2-PIN

MJB4

JUMPER_BLOCK_2-PIN

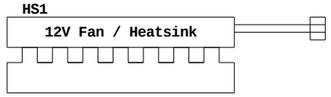
MJB2

JUMPER_BLOCK_2-PIN

CBL2

USB Mini-B Cable

HS1



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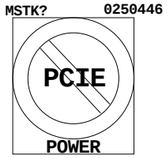

Mechanical Components

BSC Footprint, FPGA Components

XILINX

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Date:	9-24-2009_11:19	Ver:	D
Sheet Size: B		Rev:	04
Sheet	48 of 48	Drawn By	BF