

ML605 MIG Design Creation

May 2010

Overview

- **Virtex-6 DDR3 Memory Interface**
- **ML605 Board**
- **ML605 Setup**
- **Generate MIG Example Design**
- **Modifications to Example Design**
- **Compile Example Design**
- **Run MIG Example Design**
- **Adjust Data Pattern using VIO Console**
- **Example Design VIO Consoles**
- **References**

Note: This presentation applies to the ML605

Virtex-6 DDR3 Memory Interface

- **Pre-Engineered Controller and Physical Layer (PHY) memory interface**
- **300-533 MHz (600-1066 Mb/s) Performance**
 - Center Column Interfaces
 - 400 MHz in a -1 speed device
 - 533 MHz in -2, -3 devices
- **1 Gb density memory device support**
- **X4, x8, x16 device support**
- **Configurable data bus widths**
 - Multiples of 8 bits, up to 72 bits

Virtex-6 Memory Controller and Interfaces

■ Improved performance

- Higher data rates
 - Faster circuitry (40 nm)
 - Enhanced I/O (50 ps IODELAY)
 - Dedicated clocking paths
 - Real-time calibration
- Higher effective bandwidth
 - Reordering controller (DDR3/DDR2)

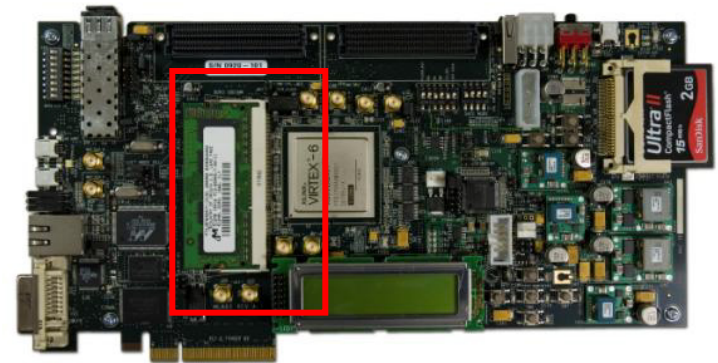
■ Improved functionality

- DDR3 DIMM write leveling

■ Easy to use

- MIG for ISE design flow
- MPMC for EDK design flow

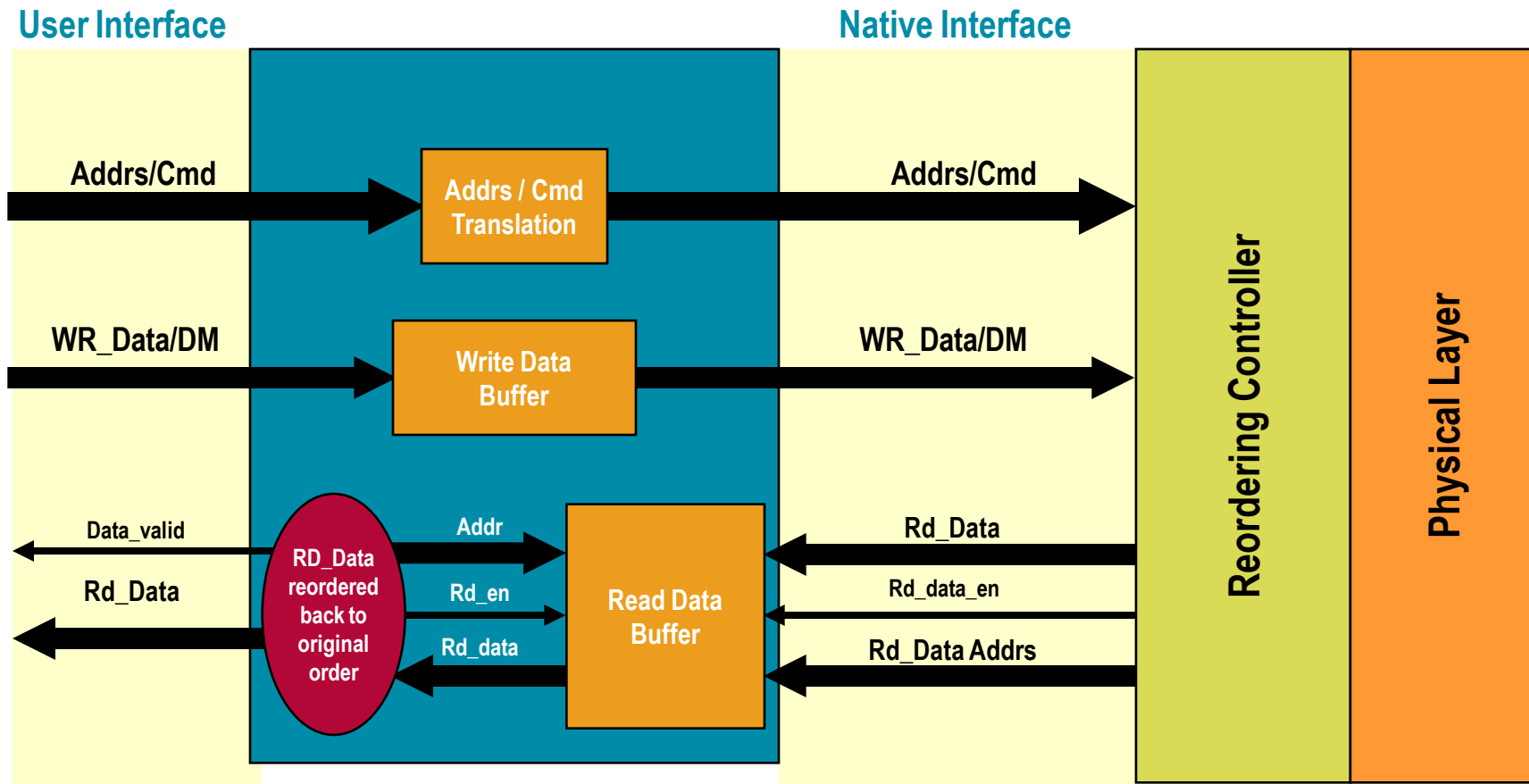
ML605 provides DDR3 SO-DIMM



Xilinx makes it easier and faster to design with Virtex-6

DDR3 User Interfaces

- **Virtex-6 FPGA user interface similar to Virtex-5 architecture**
 - Native interface option available for the advanced users to achieve lower latency

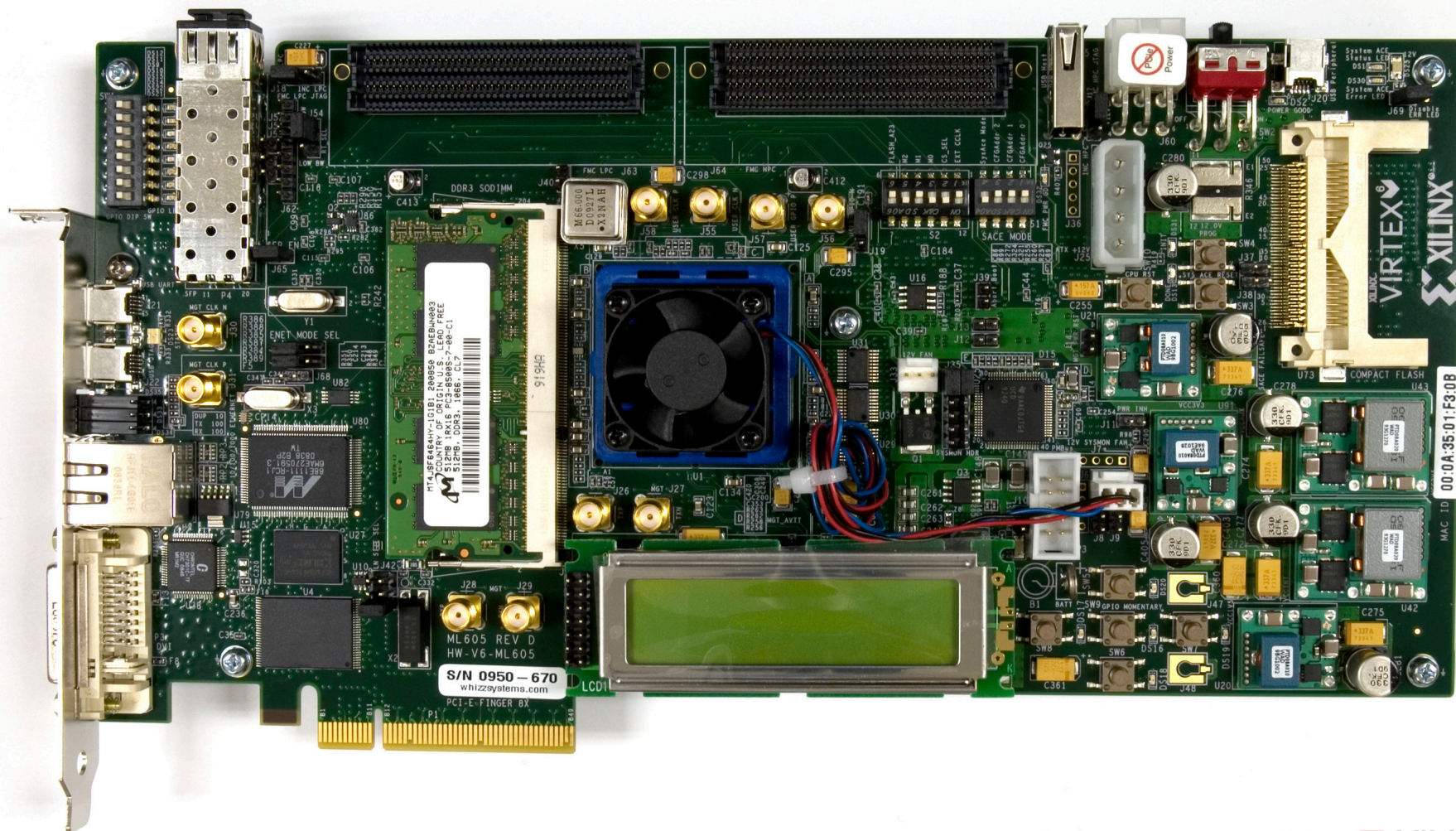


Reordering for Higher Effective Bandwidth

- **Half-frequency DDR2/DDR3 controller**
 - Control state machine runs at half the memory clock rate
- **Reorder READs to avoid precharge time penalty**
 - Example : Execute out-of-order READs to a different bank while performing precharge for the current bank
- **Regroup READs and WRITEs to minimize bus turnaround**
 - Example : Read A - Write B - Read C - Write D
 - Reordered to: Read A - Read C - Write B - Write D
- **Reordering controller looks ahead several commands**
 - Efficiency is dependent on applications (address / command patterns)

Reordering can more than double the throughput

Xilinx ML605 Board



Note: Presentation applies to the ML605

ISE Software Requirements

- **Xilinx ISE 12.1 software**



ChipScope Pro Software Requirement

- **Xilinx ChipScope Pro 12.1 software**

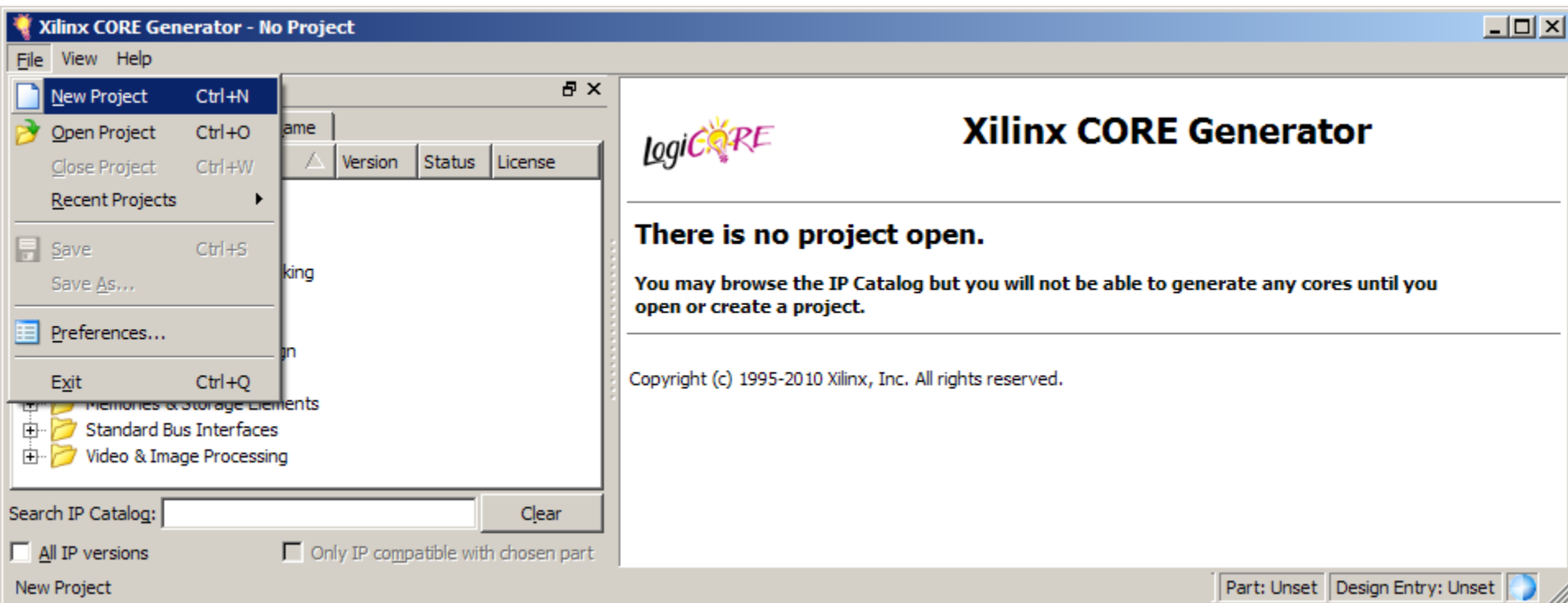


Generate MIG Example Design

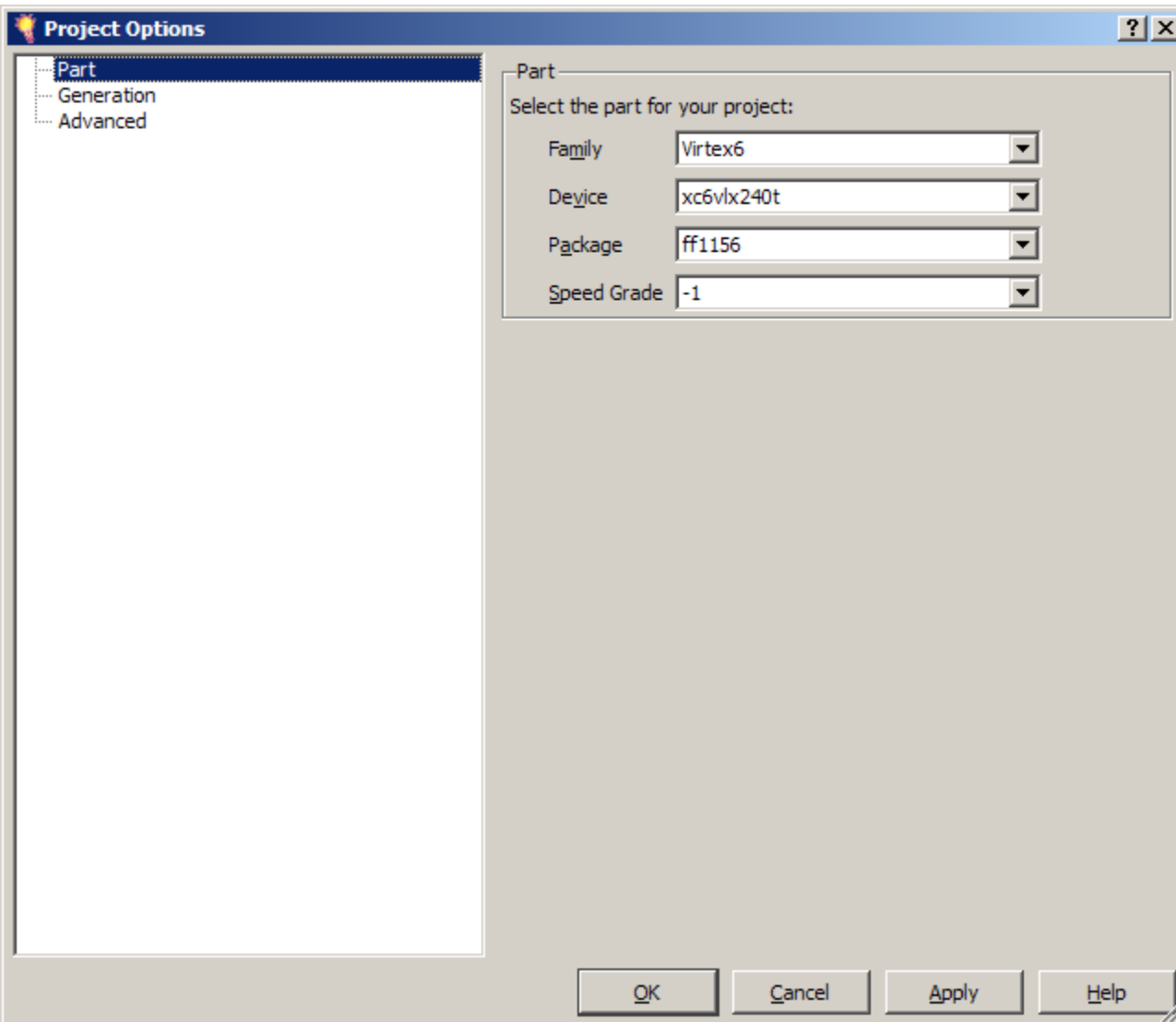
- **Open the CORE Generator**

Start → All Programs → Xilinx ISE Design Suite 12.1 → ISE → Accessories → CORE Generator

- **Create a new project; select File → New Project**



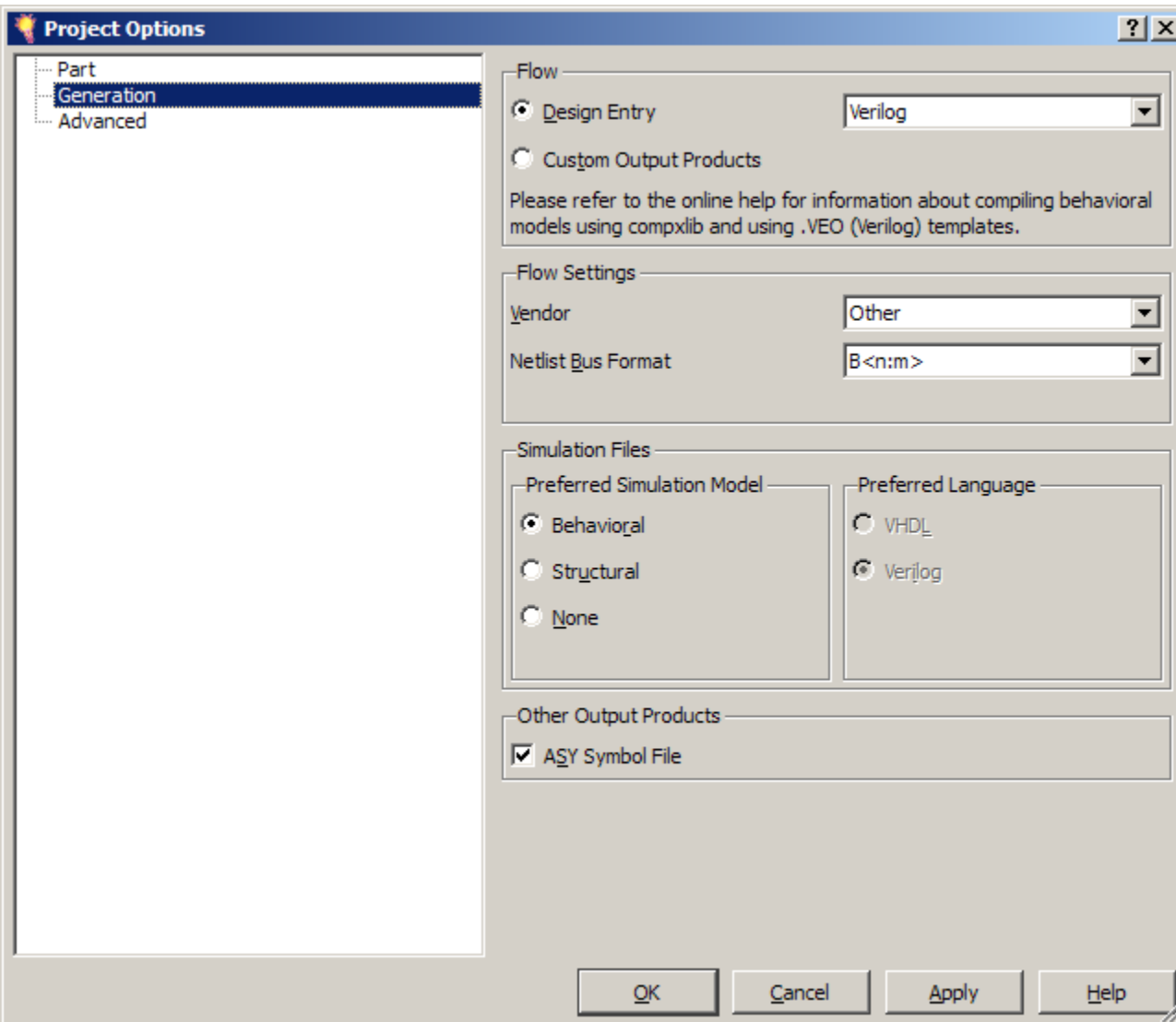
Generate MIG Example Design



- Create a project directory:
ml605_mig_design
- Name the project:
ml605_mig_design.cgp
- Set the Part (as shipped on the ML605):
 - Family: Virtex6
 - Device: xc6vlx240t
 - Package: ff1156
 - Speed Grade: -1

Note: Presentation applies to the ML605

Generate MIG Example Design





- Select Generation
- Set the Design Entry to Verilog
- Click OK

Note: Presentation applies to the ML605

Generate MIG Example Design

- **Right click on MIG Version 3.4**
 - **Select Customize and Generate**

The screenshot shows the Xilinx CORE Generator interface. The IP Catalog on the left lists various IP cores, with 'MIG' selected under 'Memory Interface Generators'. A context menu is open over the 'MIG' entry, showing options: 'Customize and Generate', 'View Answer Records', 'View Data Sheet', and 'View Version Information'. The 'Information' pane on the right displays the following details:

REFERENCE DESIGN  **MIG**  [Show Project](#)

This core is supported at status **Pre-Production** by your chosen part.

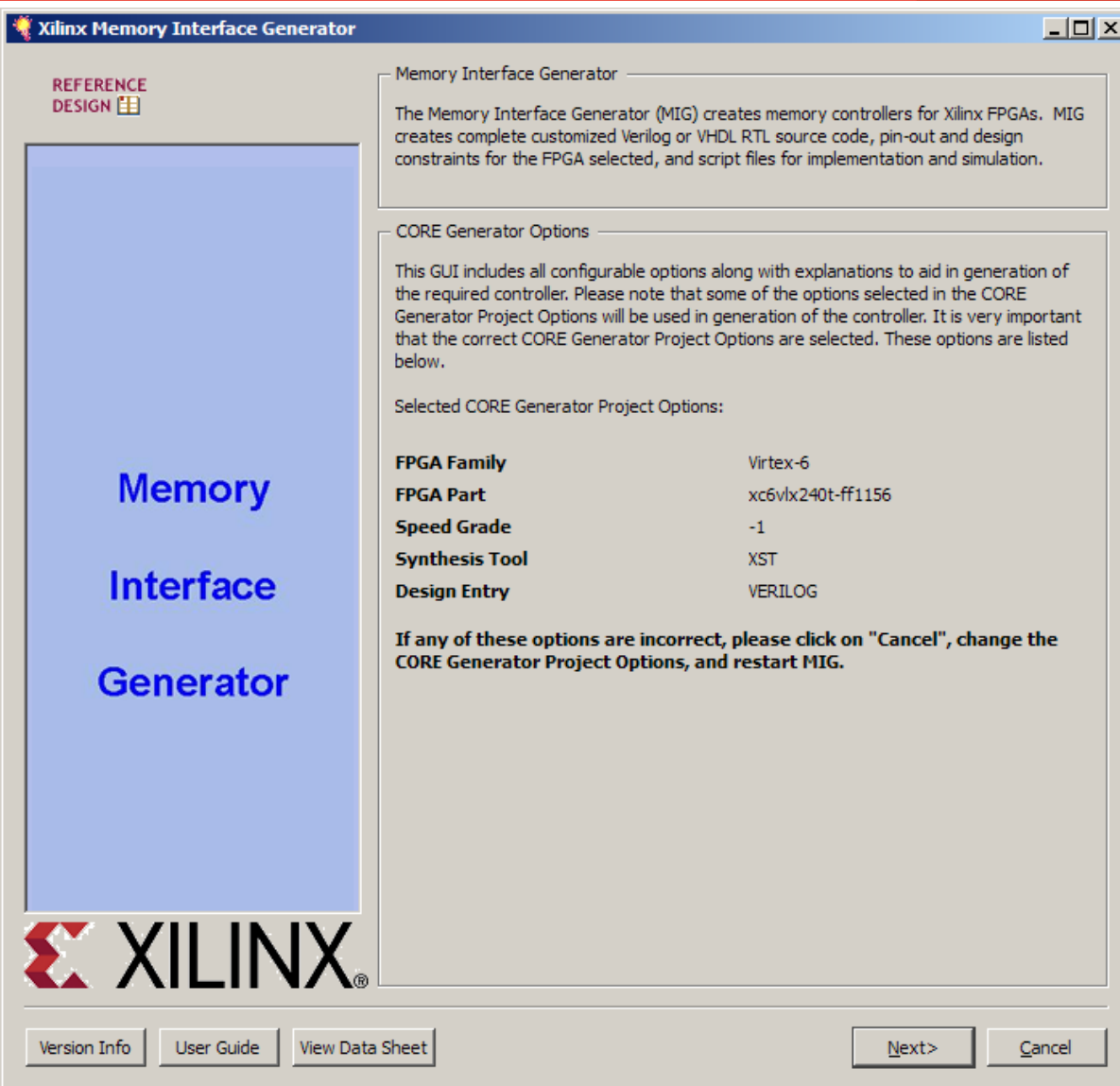
Information

Core type: MIG
Version: 3.4
Core Summary: This Memory Interface Generator is a simple menu driven tool to generate advanced memory interfaces. This tool generates HDL and pin placement constraints that will help you design your application. Spartan-3 family supports DDR & DDR2 SDRAM. Spartan-6 supports LPDDR, DDR, DDR2 & DDR3 SDRAM. Virtex-4 supports DDR & DDR2 SDRAM and QDRII & DDRII SRAM and RLDRAM II. Virtex-5 supports DDR & DDR2 SDRAM, QDRII SRAM and DDRII SRAM. Virtex-6 supports DDR2 & DDR3 SDRAM. RLDRAM II and ODRII+ SRAM.

Part: xc6vlx240t-1ff1156 Design Entry: Verilog

Note: Presentation applies to the ML605

Generate MIG Example Design



- Leave this page as is
 - Click Next

Generate MIG Example Design



- Leave this page as is
 - Click Next

Generate MIG Example Design

REFERENCE DESIGN

Pin Compatible FPGAs

Memory Selection

Controller Options

Memory Options

FPGA Options

Extended FPGA Options

Bank Selection

Summary

Memory Model

PCB Information

Design Notes

Pin Compatible FPGAs

Pin Compatible FPGAs include all devices with the same package and speed grade as the target device. Different FPGA devices with the same package do not have the same bonded pins. By selecting Pin Compatible FPGAs, MIG will only select pins that are common between the target device and all selected devices. Use the default UCF in the par folder for the target part. If you change the target part, use the appropriate UCF in the compatible_ucf folder. **If you do not choose a Pin Compatible FPGA now and need to use a different FPGA later, the generated UCF may not work for the new device and a board spin may be required.** A device is considered compatible only if the package and speed grade matches to the target part. MIG only ensures that MIG generated pin out is compatible among the selected compatible FPGA devices. Unselected devices will not be considered for compatibility during the pin allocation process.

Blank list indicates that there are no compatible parts exist for the selected target part and this page can be skipped.

Target FPGA

Pin Compatible FPGAs

- virtex6
 - lx
 - xc6vlx130t-ff1156
 - xc6vlx195t-ff1156
 - xc6vlx365t-ff1156
 - sx
 - xc6vsx475t-ff1156
 - xc6vsx315t-ff1156

Version Info User Guide View Data Sheet < Back Next > Cancel

- Leave this page as is
 - Click Next

Generate MIG Example Design



■ Select Memory Type

- DDR3 SDRAM
- Click Next

Generate MIG Example Design

Options for Controller 0 - DDR3 SDRAM

Frequency: The allowed frequency range is a function of the selected FPGA part, FPGA speed grade, and memory controller type. Choose the clock period for the desired frequency. Refer to User Guide for supported frequency range.

2500 ps 400.00 MHz

The frequency range shown here is preliminary value. Final range will be determined after characterization.

Memory Type: Select the memory type. Parts marked with a warning symbol are not compatible with the frequency selection above. Based on the FPGA package, DIMMs selection is not allowed due to the unavailability of required number of pins. For RLDRAM II only CIO parts are supported.

SODIMMs

Memory Part: Select the memory part. Parts marked with a warning symbol are not compatible with the frequency selection above. If the exact part that you will be using is not available here, you may be able to find an equivalent part. Alternately, you can create a part using the "Create Custom Part" selection at the bottom of this drop box. Refer to User Guide for complete list of memory devices supported.

MT4JSF6464HY-1G1

Data Width: MIG supports multiples of 64 for components up to 64 bits. Note that the selection is dependent upon the previously selected parameters.

64

ECC: MIG supports ECC for 72 bit and 144 bit data width configurations. To be able to select ECC, you will need to select a data width that has ECC supported.

Disabled

Data Mask: You will be able to enable/disable the generation of Data Mask (DM) pins using this check box. This option can be selectable only if the memory part you have selected has DM pins. Uncheck this box if you would like to not use data masks and save FPGA I/Os that are used for DM signals. ECC designs will not use Data Mask.

ORDERING: Normal mode allows the memory controller to reorder commands to the memory to obtain the highest possible efficiency. Strict mode forces the controller to execute commands in the exact order received.

Strict

Memory Details: 512MB, x16, row:13, col:10, bank:3, unbuffered, data bits per strobe:8, with data mask, single rank

Sheet < Back Next > Cancel

■ Select

- Type: SODIMMs
- Part: MT4JSF6464HY-1G1
- Ordering: Strict

Generate MIG Example Design

Memory Options for Controller 0 - DDR3 SDRAM

Choose the Memory Options for the memory device. Memory Option selections are restricted to those supported by the controller. Consult the memory vendor data sheet for more information.

Burst Length
Determines the maximum number of column locations that can be accessed for a given READ or WRITE command.

Read Burst Type
The ordering of accesses within a burst is determined by the burst type.

Write Recovery
Delays the internal auto precharge operation by WR clocks from the last data burst.

Output Driver Impedance Control
Programmable impedance for the output buffer.

RTT (nominal) - On Die Termination (ODT)
Select the nominal value of ODT for the DQ, DQS/DQS# and DM signals on the DIMM. This value will be used for the unwritten slot during a write in 2 slot configurations. The value will also be used for the unselected slot during a read in 2 slot configurations. Use board level simulation to choose the optimum value. The default is the value listed at the JEDEC 2007 DDR3 Workshop (http://www.jedecddr3.org/Todd_Farreell_ODT_And_Dynamic_ODT.pdf).

- Leave this page as is
 - Click Next

Generate MIG Example Design

REFERENCE DESIGN

- Pin Compatible FPGAs ✓
- Memory Selection ✓
- Controller Options ✓
- Memory Options ✓
- FPGA Options
- Extended FPGA Options
- Bank Selection
- Summary
- Memory Model
- PCB Information
- Design Notes

System Clock

Choose the desired input clock configuration. Both Design clock and Idelay Control clock will be affected. Either both the clocks can be Differential or both can be Single-Ended.

System Clock Differential

Debug Signals Control

This allows the debug signals to be monitored on the ChipScope tool. Selecting this option will port map the debug signals to the ChipScope modules in the design top module. The debug signals width is calibrated based on the selected design data width. If the design data width is greater than 72 bit and/or the number of DQS/DQS# pins of the design is greater than 18, then the debug signals width is calibrated only for first 72 bits of data.

Debug Signals for Memory Controller ON

IODELAY Power Versus Performance

Choose **High** Performance Mode for lowest IODELAY jitter and maximum interface performance. Choose **Normal** Performance Mode to reduce power by approximately "(TBD)" per pin when interface performance requirements are less stringent.

Performance Mode HIGH

Internal Vref

Internal Vref can be used to allow the use of the Vref pins as normal IO pins. This can free 2 pins per bank where inputs are used. In some topologies these 2 additional free pins will improve bank utilization. This setting has no effect on banks with only outputs.

Internal Vref

Version Info User Guide View Data Sheet < Back Next > Cancel

■ Select

- Debug: ON

Generate MIG Example Design

REFERENCE DESIGN

- Pin Compatible FPGAs ✓
- Memory Selection ✓
- Controller Options ✓
- Memory Options ✓
- FPGA Options ✓
- Extended FPGA Options
- Bank Selection
- Summary
- Memory Model
- PCB Information
- Design Notes

DDR3 SDRAM

Digitally Controlled Impedance (DCI)

The DCI (Digitally Controlled Impedance) I/O Standard is applied only for certain signals in Data group banks. In Address/Control group bank, DCI Standard is not applied on any signals. In Data group bank, only DQ and DQS/DQS# signals have DCI Standards (SSTL15_T_DCI for DQ's and DIFF_SSTL15_T_DCI for DQS and DQS#). If VRN/VRP pins in any of Address/Control group or Data group banks are utilized, then DCI Cascading have to be applied. In such scenario, you have to select a Master Bank from the drop down box in the bank selection page. Consult the User Guide for more information and use IBIS simulation to determine the best termination strategy.

Pin/Bank Selection Mode

- New Design: Pick the optimum banks for a new design
- Fixed Pin Out: Pre-existing pin out is known and fixed

Version Info | User Guide | View Data Sheet | < Back | Next > | Cancel

- **Select New Design**
 - Click Next

Generate MIG Example Design

Bank Selections | Description

Bank Selection For Controller 0 - DDR3 SDRAM

Address/Control: 25/25 ✓ Data: 96/96 ✓ System Clock: 9/9 ✓

Master Bank [] Master Bank [] Master Bank []

Left Column **Inner Left Column** **Inner Right Column**

Bank	Available IOs	Address/Control	Data	System Clock	MMCM
Bank: 16	40	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
Bank: 15	40	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
Bank: 14	40	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
Bank: 26	2	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Bank: 25	14	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>
Bank: 24	2	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Bank: 36	14	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Bank: 35	30	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	
Bank: 34	40	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	

Notes:
Press "Next" to proceed.

Deselect Banks Restore Defaults

< Back Next > Cancel

- On this screen select the banks as used on the ML605 SODIMM interface
- Click Deselect Banks

Generate MIG Example Design

- All Banks Deselected

Bank Selections | Description

Bank Selection For Controller 0 - DDR3 SDRAM

Address/Control: 0/25 ✖ Data: 0/96 ✖ System Clock: 0/9 ✖

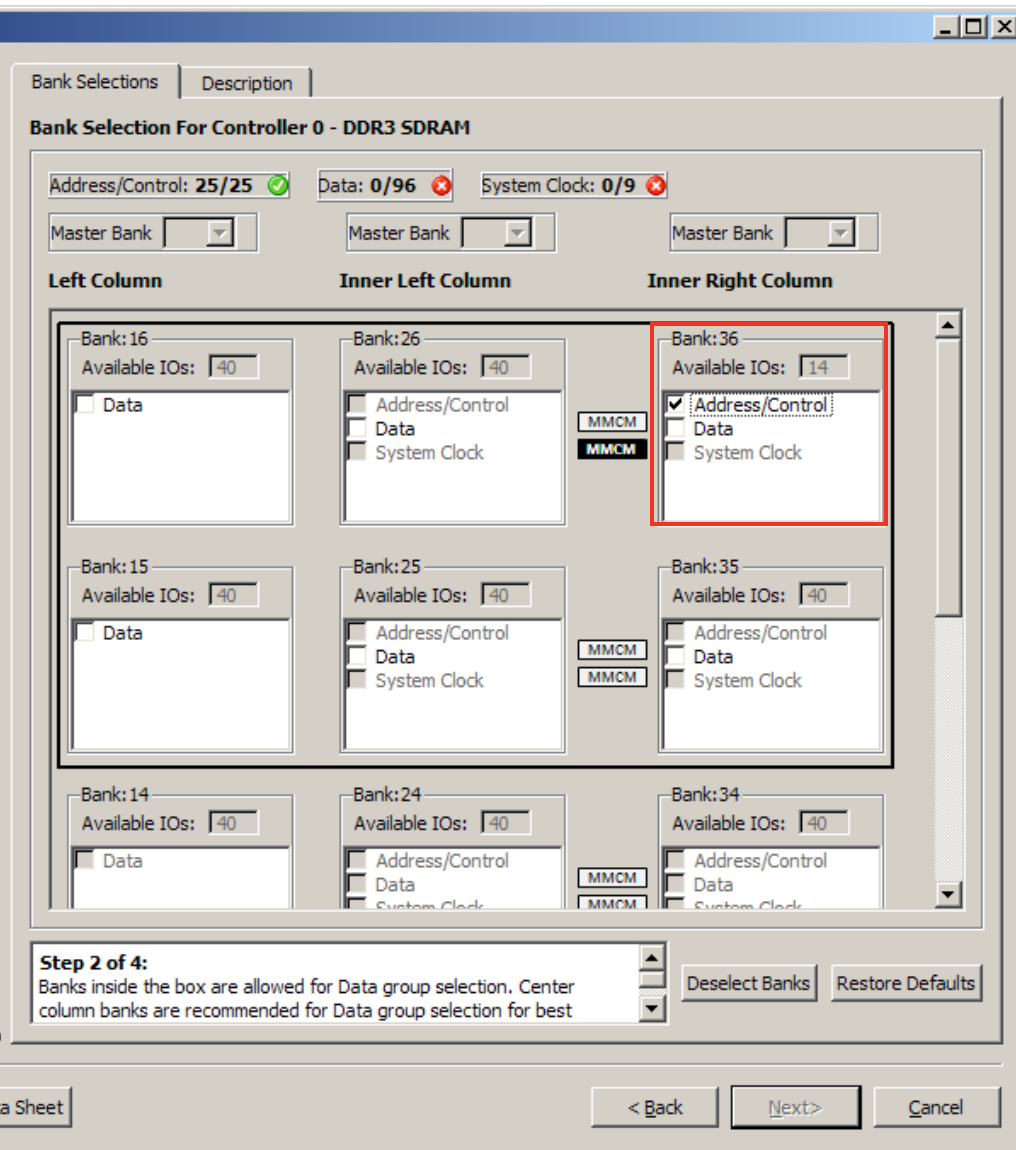
Master Bank [] Master Bank [] Master Bank []

Left Column **Inner Left Column** **Inner Right Column**

Bank	Available IOs	Address/Control	Data	System Clock	MMCM
Bank: 16	40	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
Bank: 26	40	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
Bank: 36	40	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
Bank: 15	40	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
Bank: 25	40	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
Bank: 35	40	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
Bank: 14	40	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
Bank: 24	40	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>
Bank: 34	40	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>

Step 1 of 4:
Only center column banks are allowed for Address/Control group selection. Select the "Restore Defaults" for recommended bank

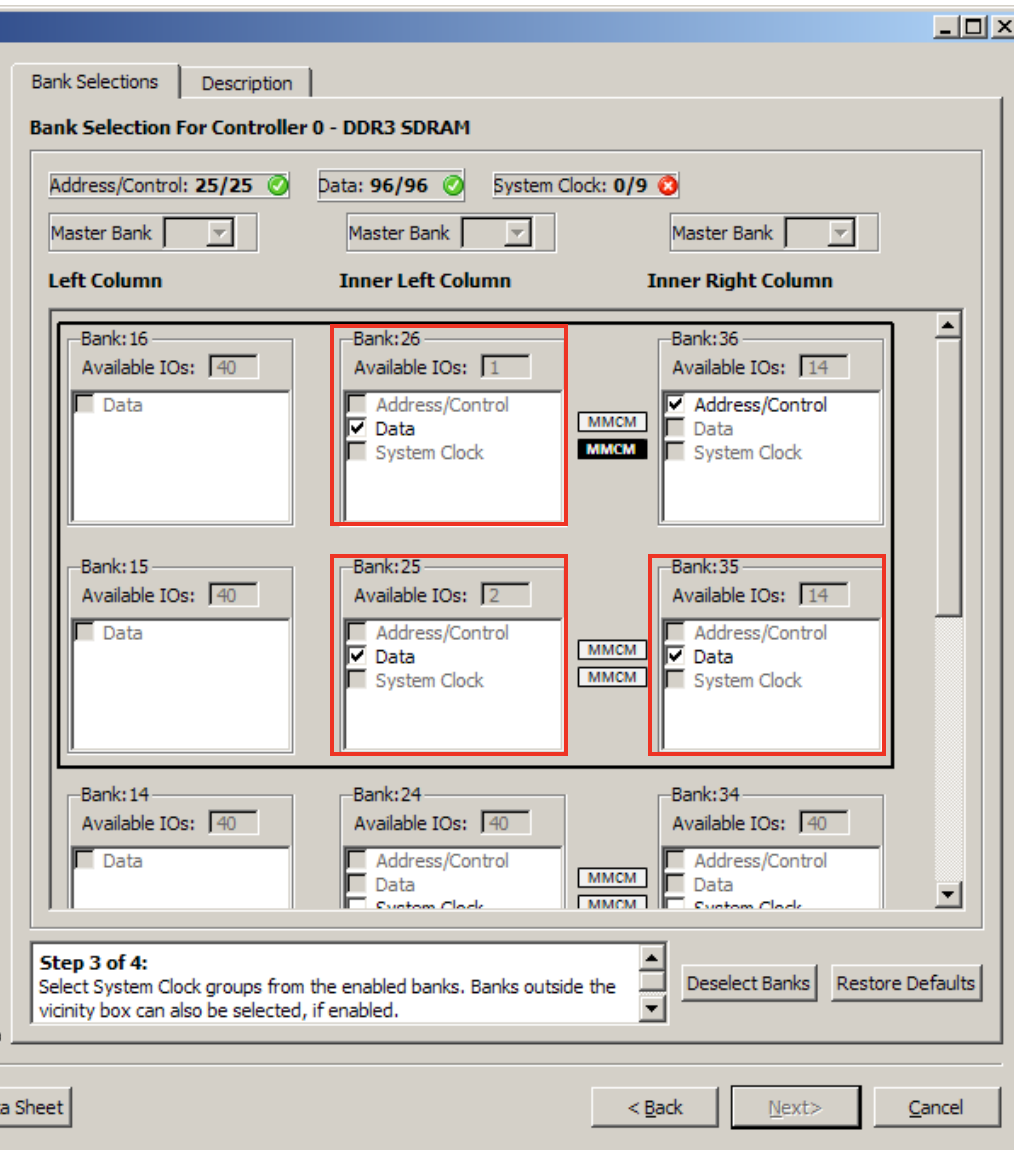
Generate MIG Example Design



■ Select

- Bank 36: Address/Control

Generate MIG Example Design



■ Select

- Bank 26: Data
- Bank 25: Data
- Bank 35: Data

Generate MIG Example Design

Bank Selections | Description

Bank Selection For Controller 0 - DDR3 SDRAM

Address/Control: 25/25 ✓ Data: 96/96 ✓ System Clock: 9/9 ✓

Master Bank [] Master Bank 25 ✓ Master Bank []

Left Column **Inner Left Column** **Inner Right Column**

Bank	Available IOs	Address/Control	Data	System Clock	MMCM
Bank: 16	40	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
Bank: 26	1	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Bank: 36	14	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
Bank: 15	40	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
Bank: 25	2	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Bank: 35	14	<input type="checkbox"/>	<input checked="" type="checkbox"/>	<input type="checkbox"/>	
Bank: 14	40	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	
Bank: 24	40	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
Bank: 34	31	<input type="checkbox"/>	<input type="checkbox"/>	<input checked="" type="checkbox"/>	

Notes:
Press "Next" to proceed.

Deselect Banks Restore Defaults

< Back Next > Cancel

■ Select

- Master Bank: 25
- Click Next

Generate MIG Example Design

REFERENCE DESIGN

- Pin Compatible FPGAs ✓
- Memory Selection ✓
- Controller Options ✓
- Memory Options ✓
- FPGA Options ✓
- Extended FPGA Options ✓
- Bank Selection ✓
- Summary
- Memory Model
- PCB Information
- Design Notes

CORE Generator Options:

Target Device	: xc6vlx240t-ff1156
Speed Grade	: -1
HDL	: verilog
Synthesis Tool	: XST

If any of the above options are incorrect, please click on "Cancel", change the CORE Generator Project Options, and restart MIG.

MIG Output Options:

Module Name	: mig_v3_4
No of Controllers	: 1
Selected Compatible Device(s)	: --

FPGA Options:

Clock Type	: Differential
Debug Port	: OFF
Internal Vref	: disabled

Extended FPGA Options:

DCI for DQ,DQS/DQS#,DM	: enabled
DCI for Address/Control	: enabled

```
/*  
Controller 0  
*/
```

Print

Version Info | User Guide | View Data Sheet | < Back | Next > | Cancel

- Leave this page as is
 - Click Next

Generate MIG Example Design

The screenshot shows the Xilinx Memory Interface Generator (MIG) software interface. The window title is "Xilinx Memory Interface Generator". On the left side, there is a "REFERENCE DESIGN" section with a grid icon. Below it is a list of design options, each with a green checkmark: Pin Compatible FPGAs, Memory Selection, Controller Options, Memory Options, FPGA Options, Extended FPGA Options, Bank Selection, Summary, Memory Model, PCB Information, and Design Notes. The main area displays the "Micron Technology, Inc. Simulation Model License Agreement". The text reads: "PLEASE READ THIS SIMULATION MODEL LICENSE AGREEMENT ('AGREEMENT') FROM MICRON TECHNOLOGY, INC. ('MTI') CAREFULLY BEFORE INSTALLING OR USING THIS SIMULATION MODEL (THE 'MODEL'). BY INSTALLING OR USING THE MODEL, YOU ARE ACCEPTING AND AGREEING TO THE TERMS AND CONDITIONS OF THIS AGREEMENT. IF YOU DO NOT AGREE WITH THE TERMS AND CONDITIONS OF THIS AGREEMENT, THEN DO NOT INSTALL OR USE THE MODEL." Below this, there are sections for "SOFTWARE LICENSE" and "MODEL LICENSE". At the bottom, there are radio buttons for "Accept" and "Decline", and a "Print" button. The Xilinx logo is visible in the bottom left corner.

- **Accept Simulation license, if desired**
 - Otherwise, Decline license
 - Click Next

Generate MIG Example Design

Xilinx Memory Interface Generator

REFERENCE DESIGN

Pin Compatible FPGAs ✓

Memory Selection ✓

Controller Options ✓

Memory Options ✓

FPGA Options ✓

Extended FPGA Options ✓

Bank Selection ✓

Summary ✓

Memory Model ✓

PCB Information

Design Notes

Creating Printed Circuit Boards for MIG Designs

The Virtex-6 Memory Interface User Guide, UG406, has information on printed circuit board (PCB) design guidelines. These important rules must be followed to ensure that the design generated by MIG works correctly in hardware. The User Guide can be accessed by clicking the User Guide button in the lower left corner of this tool.

The following rules apply when changing pin assignments after the MIG tool has generated a design:

- The address and control pin assignments can be swapped with each other as needed except clock pins
- DQ and DM pin assignments within the same byte can be swapped with each other

The affected bits require a change to the pin assignment LOC constraints in the UCF.

Print

Version Info User Guide View Data Sheet < Back Next > Cancel

- Leave this page as is
 - Click Next

Generate MIG Example Design

Xilinx Memory Interface Generator

REFERENCE DESIGN

- Pin Compatible FPGAs ✓
- Memory Selection ✓
- Controller Options ✓
- Memory Options ✓
- FPGA Options ✓
- Extended FPGA Options ✓
- Bank Selection ✓
- Summary ✓
- Memory Model ✓
- PCB Information ✓
- Design Notes

DDR3 SDRAM Design for Virtex-6 FPGAs

Design Notes

1. This design is tested with ISE 12.1 and Synplify Pro D-2009.12
2. Inner and Outer Column banks are permitted for selection
3. Only Single Rank memory parts are supported
4. In case of DCI Cascading, a Master bank must be selected. In between the Master and Slave banks or in between two Slave banks, there cannot be a bank with different IO Standard (viz., System Clock bank)
5. Users with components must lay out their board using fly by topology as if on a DIMM
6. The frequency range is preliminary and subject to characterization
7. Hardware test bench logic does not support: ECC enable designs and Burst Length "On the Fly"
8. Design control and status pins (viz., sys_rst, error, phy_init_done,..) are allocated in System Clock bank
9. ModelSim simulation error "#
sim_tb_top.comp_inst.mem_8_4.gen_mem[2].u_comp_dds at time 18790687.0 ps WARNING: tWLS violation on DQS bit 0 positive edge. Indeterminate CK capture is possible.
#sim_tb_top.comp_inst.mem_8_4.gen_mem[2].u_comp_dds at time 18790687.0 ps Write Leveling @ DQS ck = 1" can be ignored

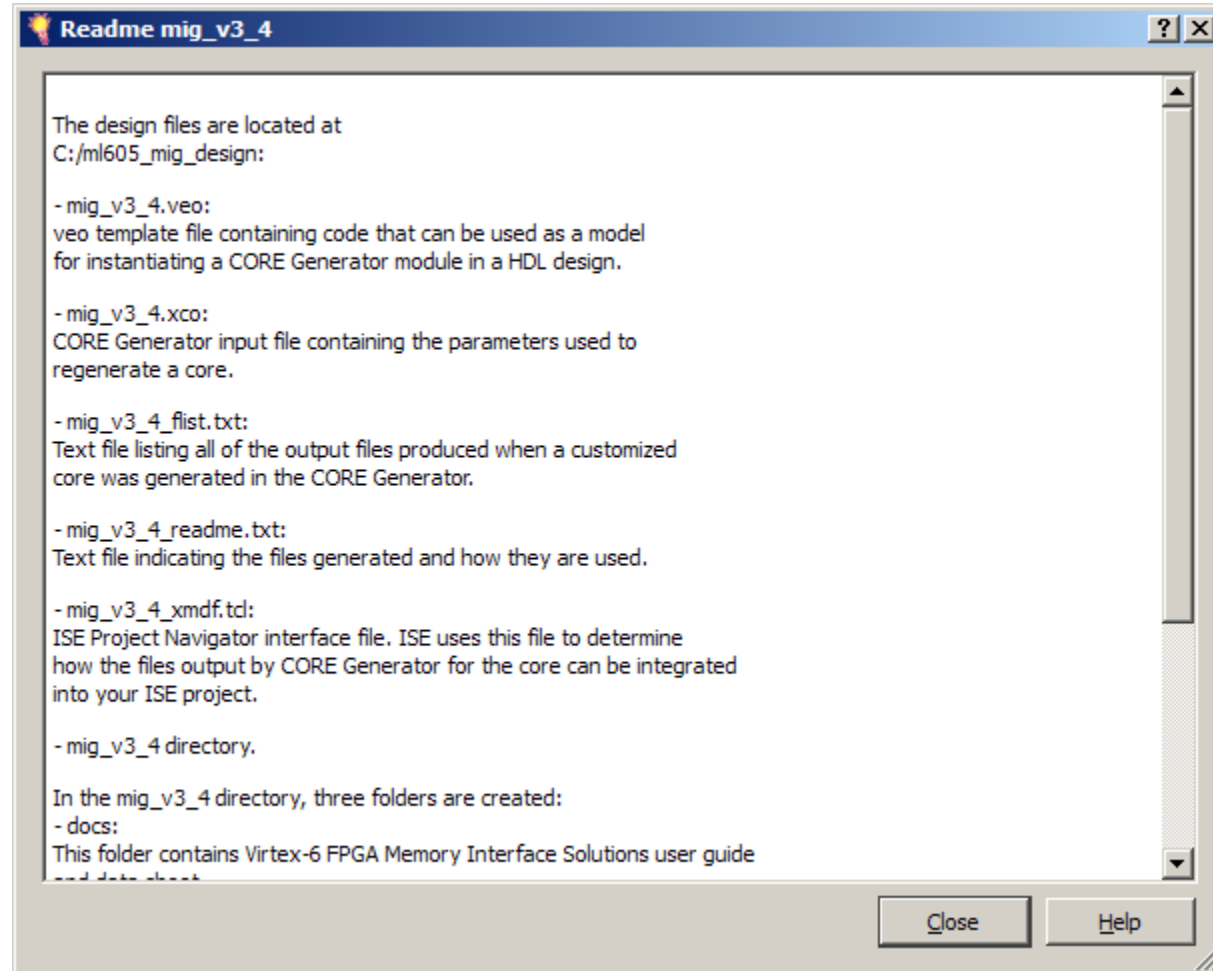
Print

Version Info User Guide View Data Sheet < Back Generate Cancel

- Click Generate

Generate MIG Example Design

- After the MIG core finishes generating, click **Close** on the Datasheet window



Generate MIG Example Design

- MIG design appears in Project IP

The screenshot shows the Xilinx CORE Generator interface. The title bar reads "Xilinx CORE Generator - C:\ml605_mig_design\ml605_mig_design.cgp". The menu bar includes "File", "Project", "View", and "Help".

The "Project IP" window is open, displaying a table with the following data:

Instance Name	Core Name	Version	Last Modified	Status
mig_v3_4	MIG	3.4	2010-04-29 at 09:21	Pre-Production

Below the table is a "Search Project IP:" field with a "Clear" button. At the bottom left, there are buttons for "Project IP" and "IP Catalog".

The main content area displays "REFERENCE DESIGN" and "MIG" in large text. A "Show Project" button is visible in the top right. The text below reads:

Core Selected: **MIG**

This core was generated for a virtex6 (xc6vlx240t-1ff1156) on 2010-04-29 at 09:21

This core is supported at status **Pre-Production** by your chosen part.

Information

Core type: MIG
Version: 3.4
Core Summary: This Memory Interface Generator is a simple menu driven tool to generate advanced memory interfaces. This tool generates HDL and pin placement constraints that will help you design your application. Spartan-3 family supports DDR & DDR2 SDRAM. Spartan-6 supports LPDDR, DDR, DDR2 & DDR3 SDRAM. Virtex-4 supports DDR & DDR2 SDRAM and QDRII & DDRII SRAM and RLD RAM II. Virtex-5 supports

At the bottom right, the status bar shows "Part: xc6vlx240t-1ff1156" and "Design Entry: Verilog".

Modifications to Example Design

- **RDF0011.zip includes**

- ChipScope Project File, UCF, and Verilog Files

- **Modifications to RTL Files for ML605 Example Design**

- Changed design to support a single 200 MHz LVDS clock input
- Added Debug display code to drive LEDs
- Added ChipScope ILA and VIO port assignments for ML605 board debug
- Removed IIC Signals – sda, scl
- Changed various parameter to match the ML605 board
 - DIVCLK_DIVIDE = 1 (was 2 in MIG 3.4 output)
 - OUTPUT_DRV to “HIGH”
 - nDQS_COLx
 - DQS_LOC_COLx
 - RST_ACT_LOW = 0 (was 1)

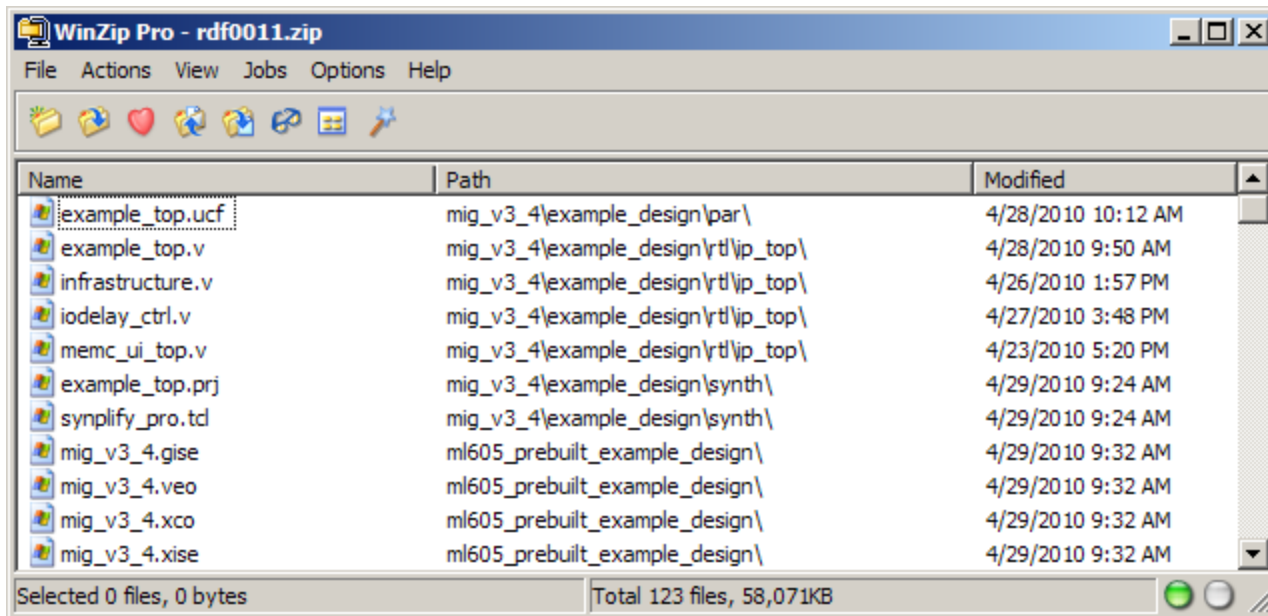
Modifications to Example Design

▪ Updates to UCF file specifically required for ML605 board:

- Updated IO Locations to match ML605
- Remove IIC Signals – sda, scl
- Merged Default two clocks into one clock for ML605
- Moved sys_reset to CPU_RESET
- Edited DCI_CASCADE to match ML605
- Removed CONFIG_PROHIBIT lines
- Added LOC for GPIO LED signals (2.5V bank voltage)
- Added LOCs for RSYNC OSERDES and IODELAY

Modifications to Example Design

- **Unzip the rdf0011.zip file to your C:\ml605_mig_design directory**
 - Available through <http://www.xilinx.com/ml605>
 - This adds modifications to the example design (1)
 - A fully pre-built ML605 example design is included in the zip file (2)
 - Use the included bitstream to [run MIG with ChipScope](#)
 - Run **ise_flow.bat** in <design directory>\ml605_prebuilt_example_design\mig_v3_4\example_design\par to recompile the pre-built example design

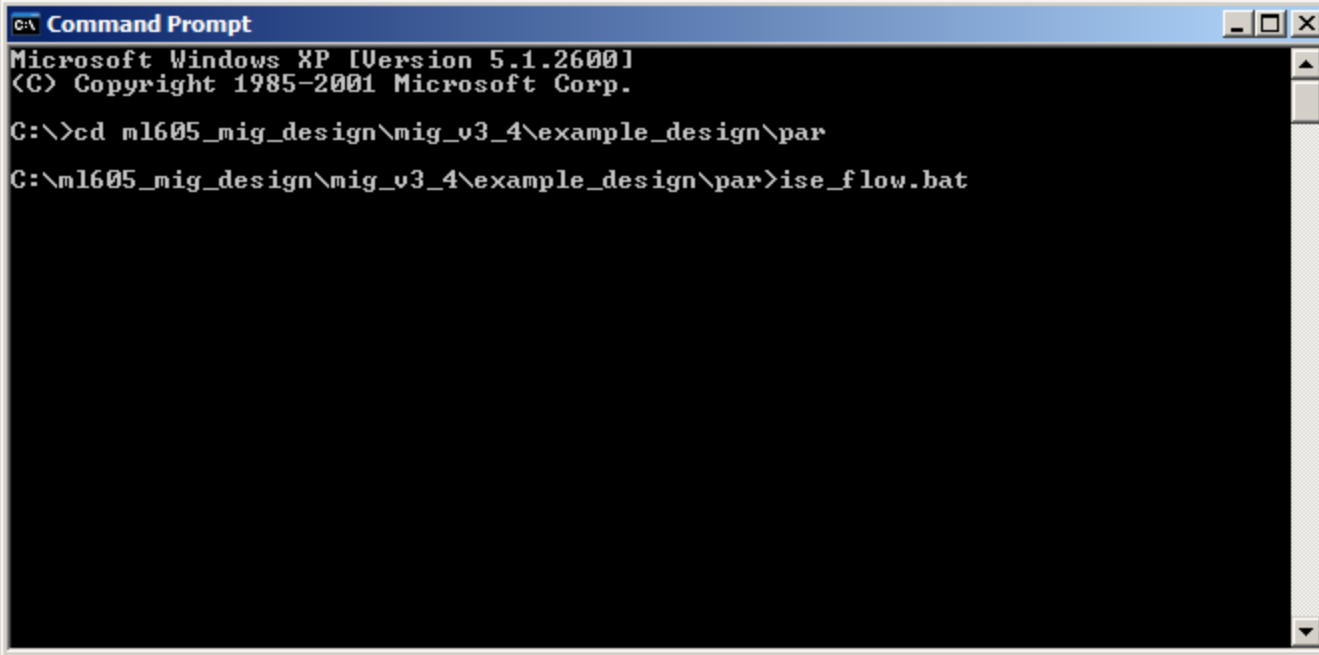


Note: Overwrites Core Generator output files with ML605 specific files (1)

Compile Example Design

- Start a windows command shell and enter these commands:

```
cd ml605_mig_design\mig_v3_4\example_design\par  
ise_flow.bat
```



```
C:\ Command Prompt  
Microsoft Windows XP [Version 5.1.2600]  
(C) Copyright 1985-2001 Microsoft Corp.  
  
C:\>cd ml605_mig_design\mig_v3_4\example_design\par  
C:\ml605_mig_design\mig_v3_4\example_design\par>ise_flow.bat
```

Run MIG Example Design

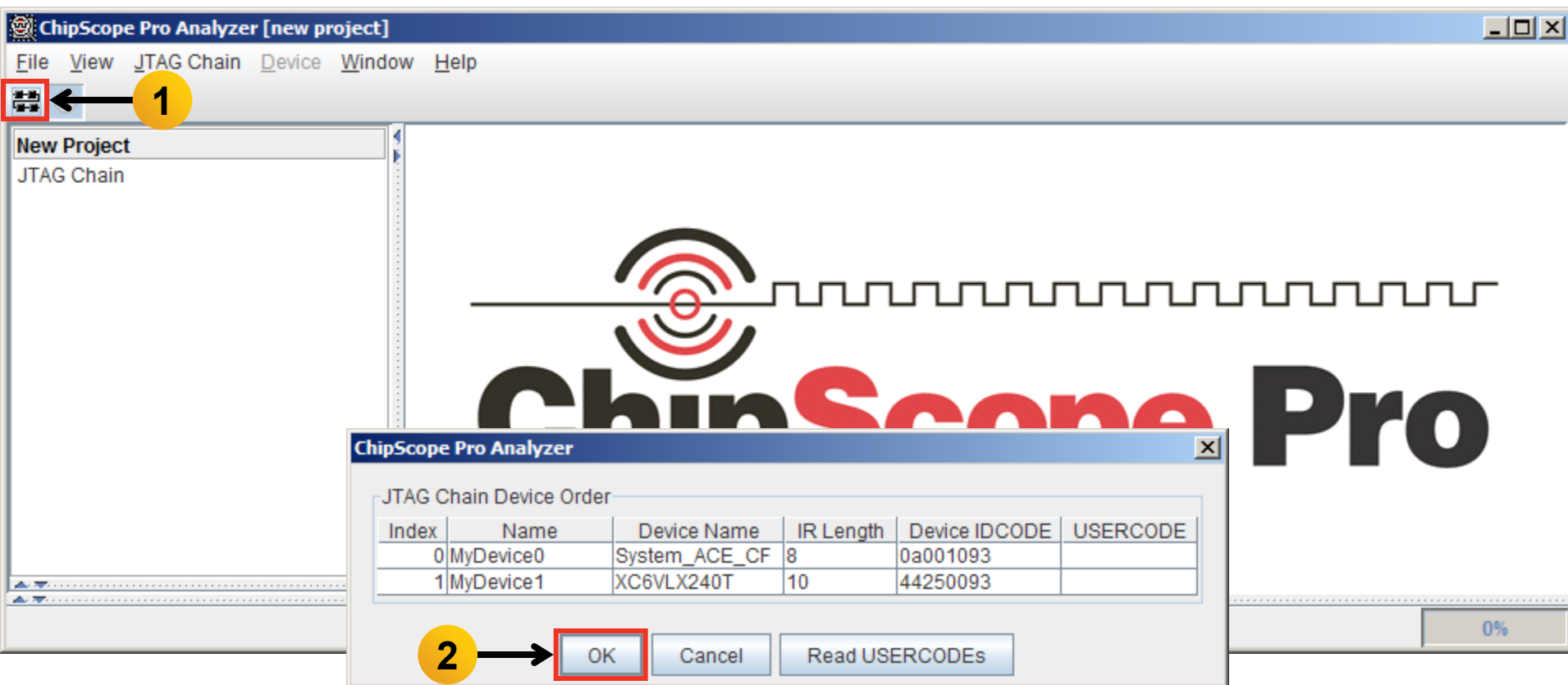
- Power on the ML605 board
- Connect a USB Type-A to Mini-B cable to the USB JTAG connector on the ML605 board
 - Connect this cable to your PC



Note: Presentation applies to the ML605

Run MIG Example Design

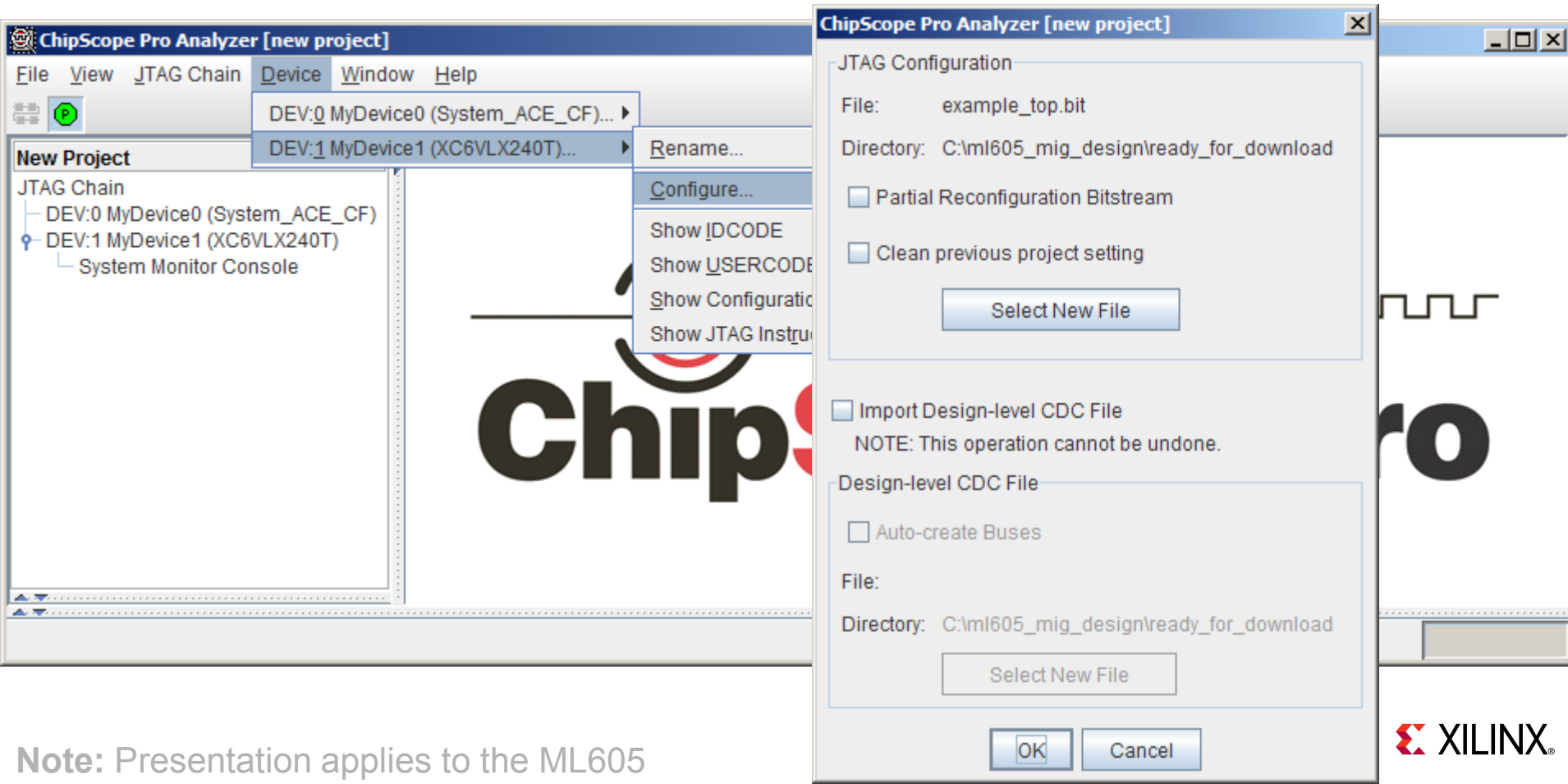
- **After the design compiles, open ChipScope Pro Analyzer**
 - Click on the Open Cable Button (1)
 - Click OK (2)



Note: Presentation applies to the ML605

Run MIG Example Design

- Select Device → DEV:0 MyDevice0 (XC6VLX240T) → Configure...
- Select <Design Path>\mig_v3_4\example_design\par\example_top.bit



The screenshot displays the ChipScope Pro Analyzer interface. The 'Device' menu is open, showing two options: 'DEV:0 MyDevice0 (System_ACE_CF)...' and 'DEV:1 MyDevice1 (XC6VLX240T)...'. The 'Configure...' option is selected for the second device. The 'JTAG Configuration' dialog box is open, showing the file 'example_top.bit' and the directory 'C:\ml605_mig_design\ready_for_download'. The dialog box has several options, including 'Partial Reconfiguration Bitstream', 'Clean previous project setting', 'Import Design-level CDC File', and 'Auto-create Buses'. The 'File' and 'Directory' fields are also visible.

Note: Presentation applies to the ML605

XILINX

Run MIG Example Design

- **Select File → Open Project...**
- **Select <Design Path>\ready_for_download\
ML605_SODIMM_example_design.cpj**



Run MIG Example Design

- Click on Trigger Setup to view trigger settings
- The error bit value should be set to 1

ChipScope Pro Analyzer [ML605_SODIMM_example_design]

File View JTAG Chain Device Trigger Setup Waveform Window Help

Trigger Run Mode: Single

Project: ML605_SODIMM_example_desi

JTAG Chain

- DEV:0 MyDevice0 (System_ACE_CF)
- DEV:1 MyDevice1 (XC6VLX240T)
 - System Monitor Console
 - UNIT:0 MyILA0 (ILA)
 - Trigger Setup
 - Waveform
 - Listing
 - Bus Plot
 - UNIT:1 MyVIO1 (VIO)
 - UNIT:2 MyVIO2 (VIO)
 - UNIT:3 MyVIO3 (VIO)
 - UNIT:4 MyVIO4 (VIO)

Trigger Setup - DEV:1 MyDevice1 (XC6VLX240T) UNIT:0 MyILA0 (ILA)

Match Unit	Function	Value	Radix	Counter
M0:TRIG0	==	XX1X_XXXX	Bin	disabled
/TRIG0[7]			X	
/TRIG0[6]			X	
error			1	
/dfi_init_complete			X	
/dbg_rdlvl_err[1]			X	
/dbg_rdlvl_err[0]			X	
/dbg_rdlvl_done[1]			X	
/dbg_rdlvl_done[0]			X	

Type: Window Windows: 1 Depth: 1024 Position: 512

Storage Qualification: All Data

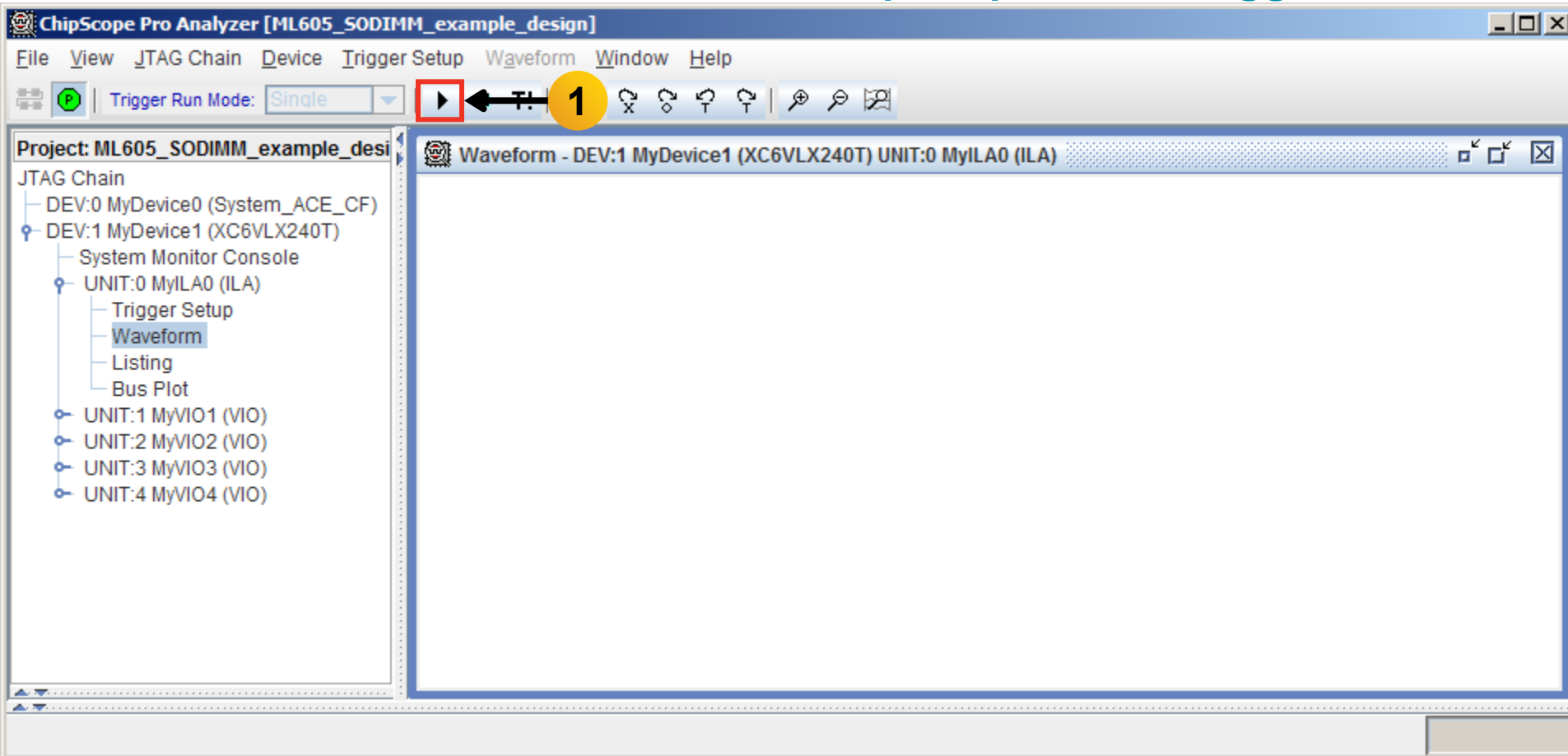
Trigger Conditions

IDLE

Reading project file: C:\ml605_mig_design\ready_for_download\ML605_SODIMM_example_design.cpj

Run MIG Example Design

- Click on Waveform; click the Arm Trigger button (1)
- Detection of an error will cause ChipScope Pro to trigger



Run MIG Example Design

- The Example Design should run error free (no trigger on error)
- To force a trigger, click the T! button (1)

ChipScope Pro Analyzer [ML605_S0DIMM_example_design]

File View JTAG Chain Device Trigger Setup Waveform Window Help

Trigger Run Mode: Single

Waveform - DEV:1 MyDevice1 (XC6VLX240T) UNIT:0 MyILA0 (ILA)

Bus/Signal	X	O	84	385	386	387	388	389
/dfi_init_complete	1	1						
/dbg_rdlvl_done	3	3				3		
/dbg_rdlvl_err	0	0				0		
error	0	0						
app_rd_data_valid	0	0						
/dbg_rddata_rise0	0092i	0092i	00092B9C0	0092B9E00092B9E0	0092BA000092BA00	0092BA200092BA20	0092B82000	
/dbg_rddata_fall0	0092i	0092i	00092B9C0	0092B9E00092B9E0	0092BA000092BA00	0092BA200092BA20	0012082000	
/dbg_rddata_rise1	0092i	0092i	00092B9C0	0092B9E00092B9E0	0092BA000092BA00	0092BA200092BA20	0000002100	
/dbg_rddata_fall1	0092i	0092i	00092B9C0	0092B9E00092B9E0	0092BA000092BA00	0092BA200092BA20	0000002100	

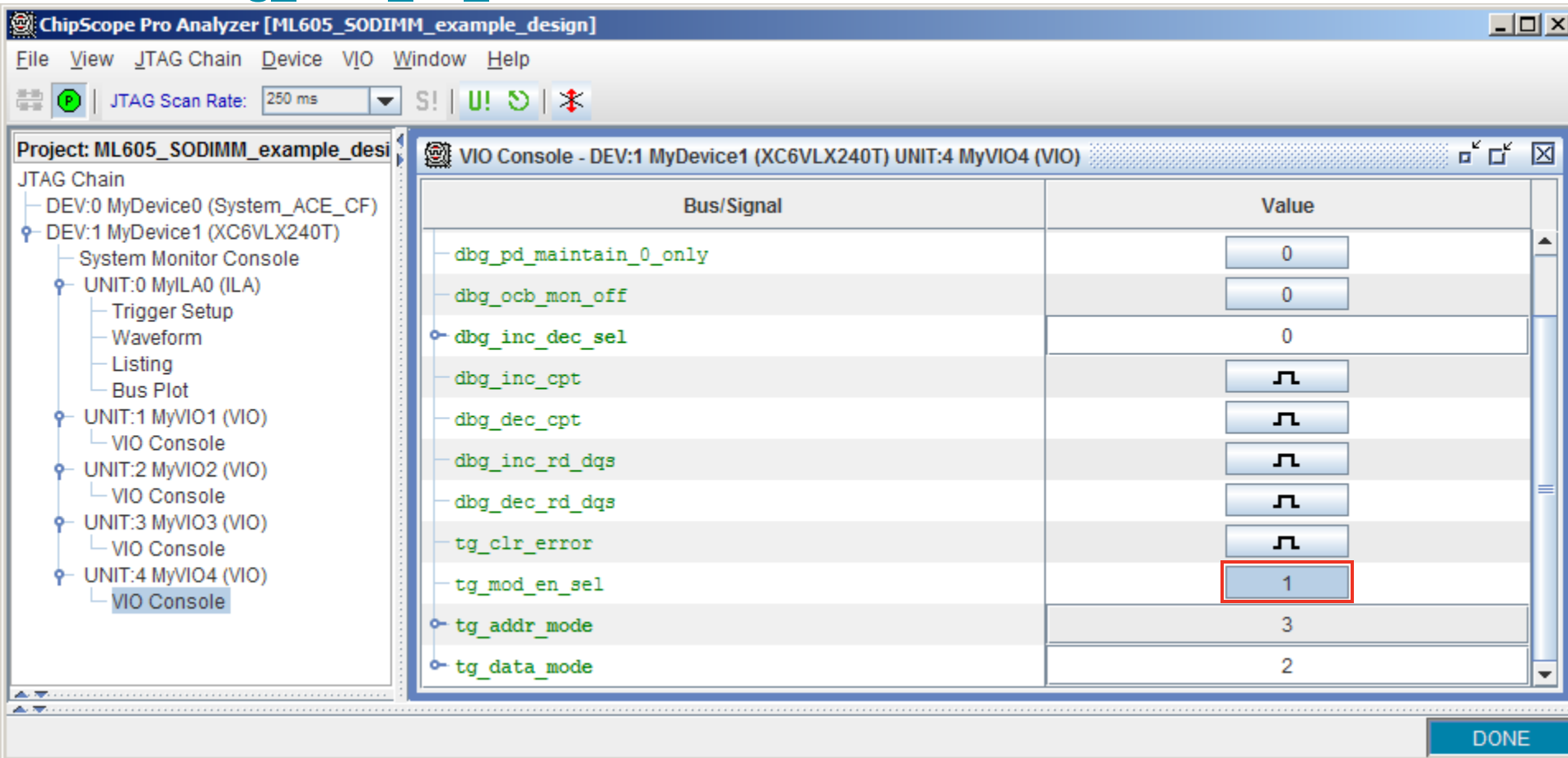
Waveform captured Apr 29, 2010 11:46:46 AM

X: 0 O: 0 $\Delta(X-O) : 0$




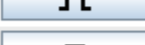
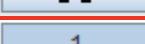
DONE

Adjust Data Pattern using VIO Console

- Select VIO Console 4
- Set `tg_mod_en_sel` to 1



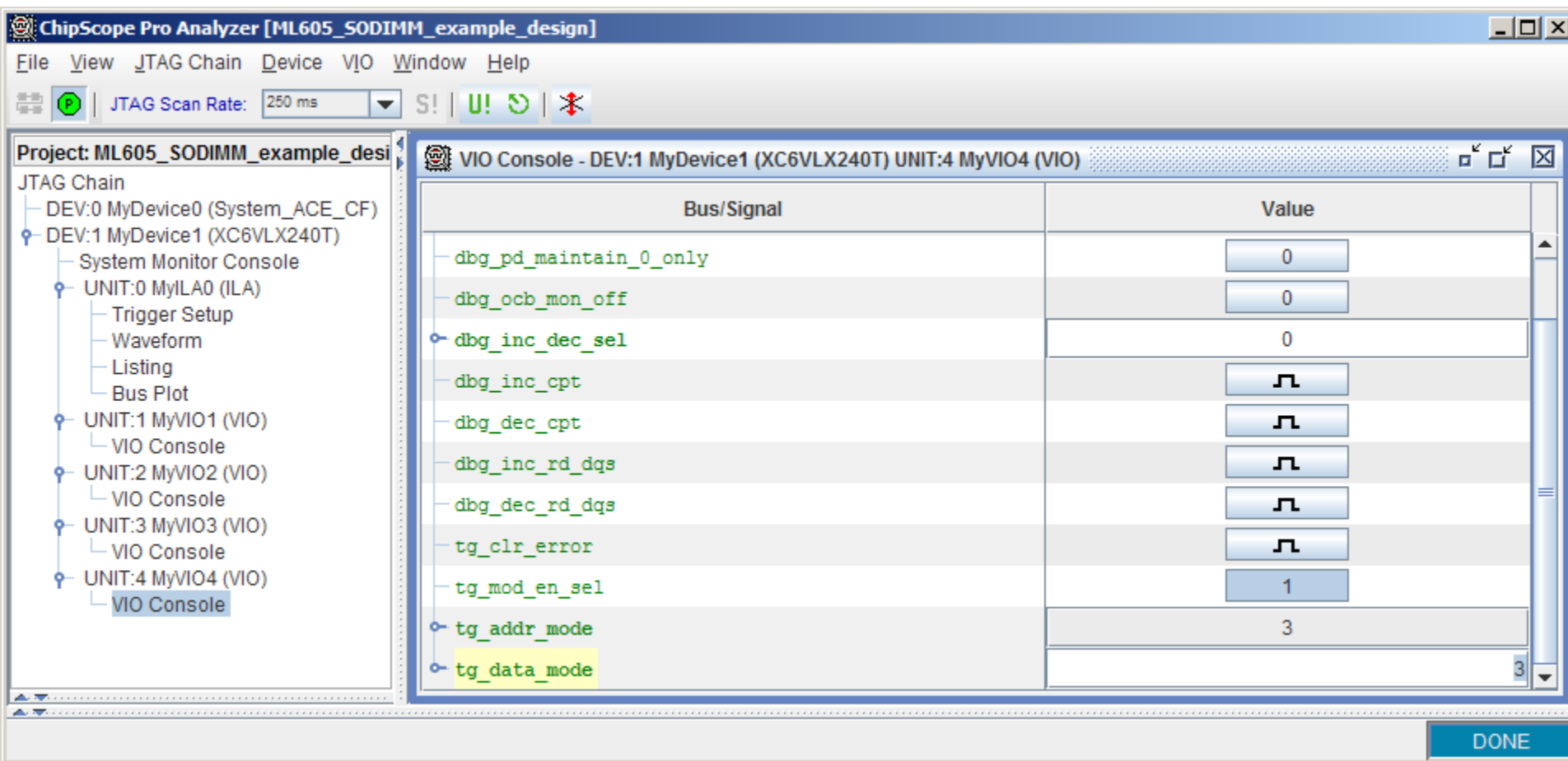
The screenshot shows the ChipScope Pro Analyzer interface. The main window displays the VIO Console for UNIT:4 MyVIO4 (VIO). The console shows a list of signals and their values. The signal `tg_mod_en_sel` is highlighted with a red box, and its value is set to 1.

Bus/Signal	Value
<code>dbg_pd_maintain_0_only</code>	0
<code>dbg_ocb_mon_off</code>	0
<code>dbg_inc_dec_sel</code>	0
<code>dbg_inc_cpt</code>	
<code>dbg_dec_cpt</code>	
<code>dbg_inc_rd_dqs</code>	
<code>dbg_dec_rd_dqs</code>	
<code>tg_clr_error</code>	
<code>tg_mod_en_sel</code>	1
<code>tg_addr_mode</code>	3
<code>tg_data_mode</code>	2

Note: Presentation applies to the ML605

Adjust Data Pattern using VIO Console

- Set `tg_data_mode` to “3” for HAMMER_DATA_MODE



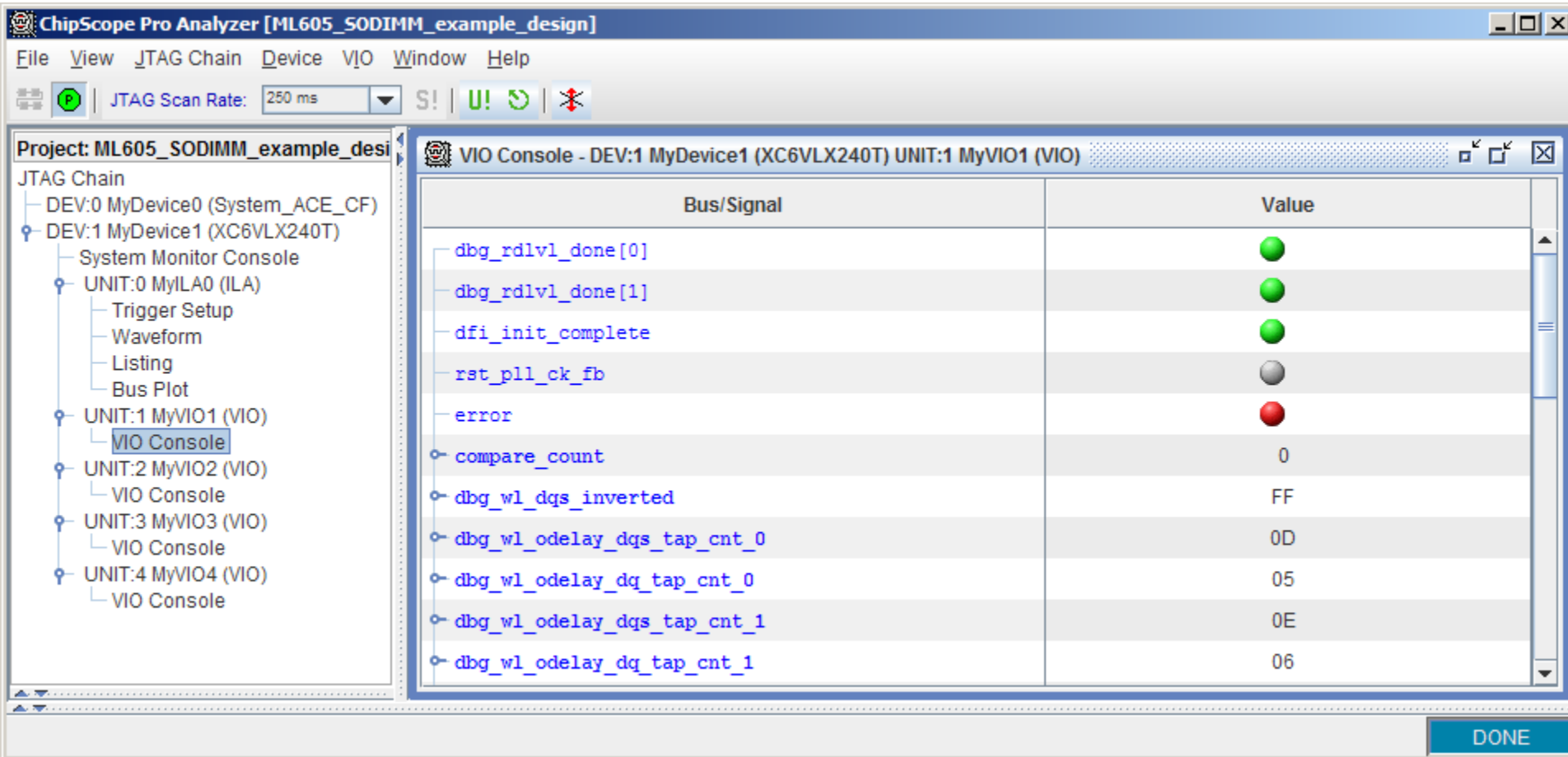
The screenshot shows the ChipScope Pro Analyzer interface for a project named "ML605_SODIMM_example_design". The VIO Console window is open, displaying a list of bus/signals and their current values. The signal `tg_data_mode` is highlighted in yellow, and its value is set to 3. The signal `tg_mod_en_sel` is set to 1, and other signals like `dbg_inc_dec_sel` and `dbg_inc_cpt` are set to 0. The VIO Console window title is "VIO Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:4 MyVIO4 (VIO)".

Bus/Signal	Value
<code>dbg_pd_maintain_0_only</code>	0
<code>dbg_ocb_mon_off</code>	0
<code>dbg_inc_dec_sel</code>	0
<code>dbg_inc_cpt</code>	0
<code>dbg_dec_cpt</code>	0
<code>dbg_inc_rd_dqs</code>	0
<code>dbg_dec_rd_dqs</code>	0
<code>tg_clr_error</code>	0
<code>tg_mod_en_sel</code>	1
<code>tg_addr_mode</code>	3
<code>tg_data_mode</code>	3

Note: Presentation applies to the ML605

Adjust Data Pattern using VIO Console

- Select VIO Console 1
- Note error is active



ChipScope Pro Analyzer [ML605_SODIMM_example_design]

File View JTAG Chain Device VIO Window Help

JTAG Scan Rate: 250 ms

Project: ML605_SODIMM_example_desi

JTAG Chain

- DEV:0 MyDevice0 (System_ACE_CF)
- DEV:1 MyDevice1 (XC6VLX240T)
 - System Monitor Console
 - UNIT:0 MyILA0 (ILA)
 - Trigger Setup
 - Waveform
 - Listing
 - Bus Plot
 - UNIT:1 MyVIO1 (VIO)
 - VIO Console
 - UNIT:2 MyVIO2 (VIO)
 - VIO Console
 - UNIT:3 MyVIO3 (VIO)
 - VIO Console
 - UNIT:4 MyVIO4 (VIO)
 - VIO Console

VIO Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:1 MyVIO1 (VIO)

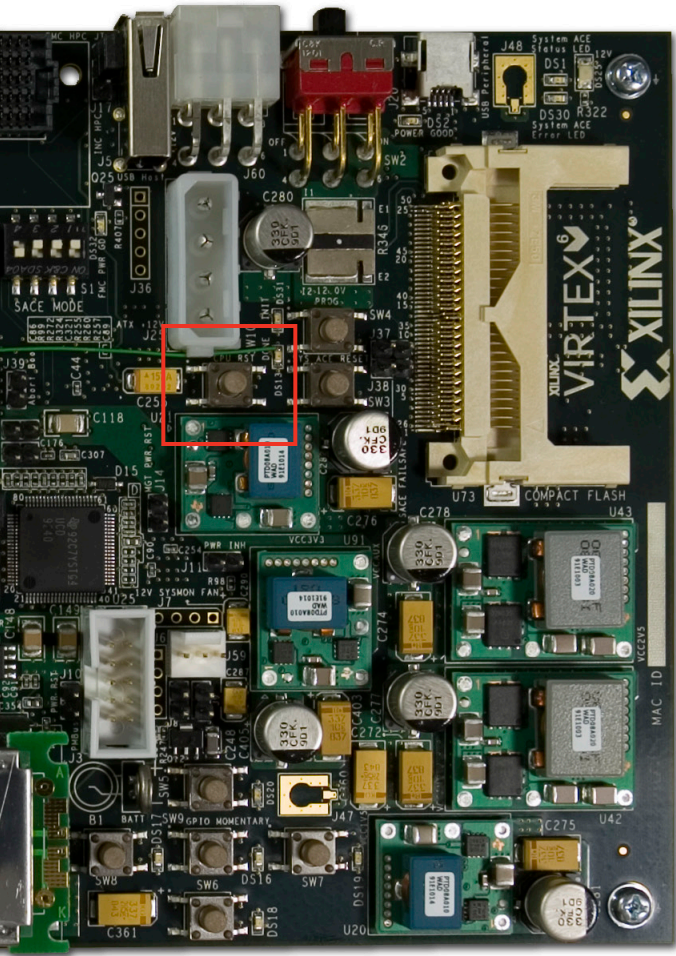
Bus/Signal	Value
dbg_rdlvl_done[0]	
dbg_rdlvl_done[1]	
dfi_init_complete	
rst_pll_ck_fb	
error	
compare_count	0
dbg_wl_dqs_inverted	FF
dbg_wl_odelay_dqs_tap_cnt_0	0D
dbg_wl_odelay_dq_tap_cnt_0	05
dbg_wl_odelay_dqs_tap_cnt_1	0E
dbg_wl_odelay_dq_tap_cnt_1	06

DONE

Note: Presentation applies to the ML605

Adjust Data Pattern using VIO Console

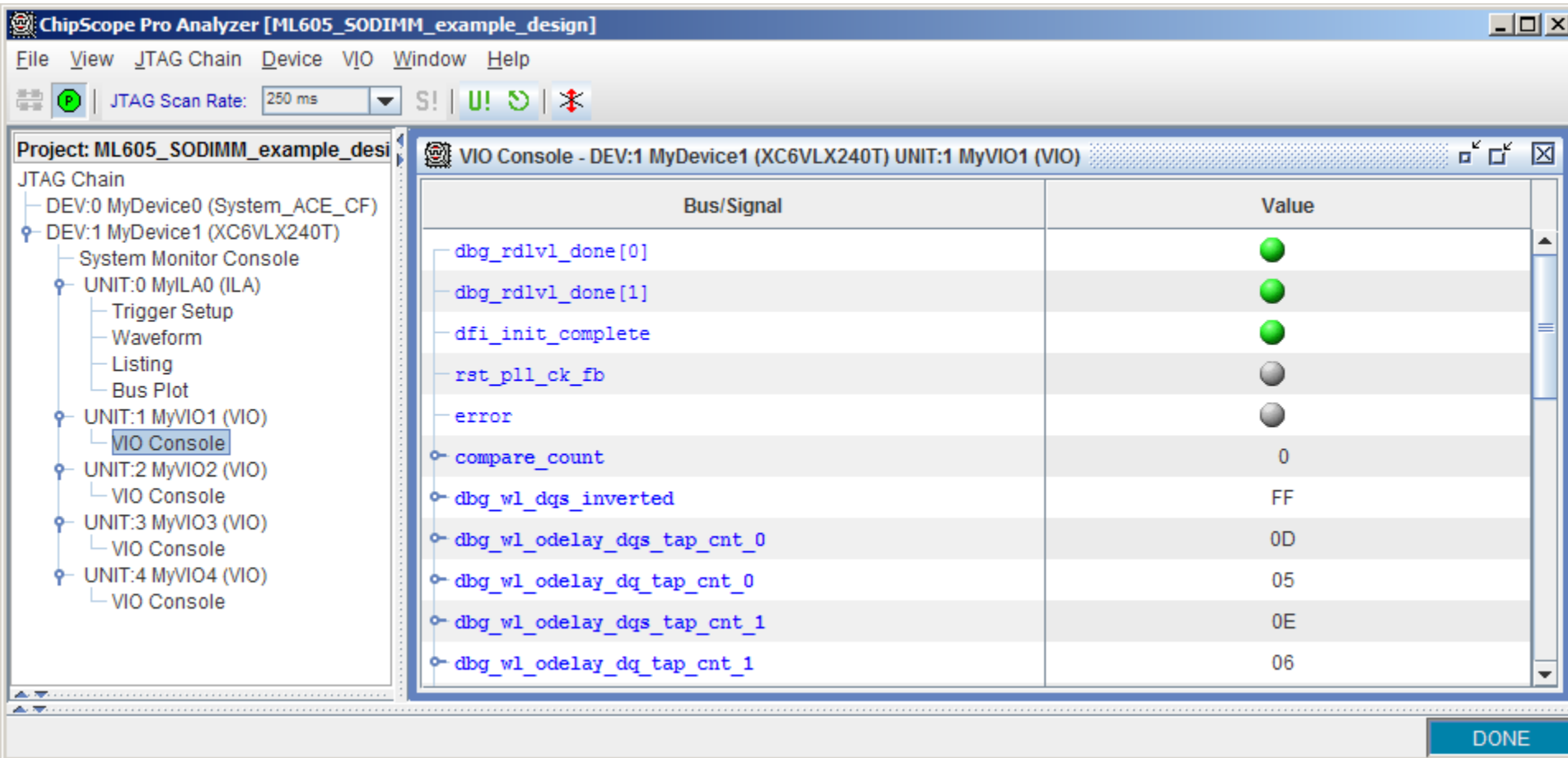
- Press and release the CPU RESET switch, SW10, after each change to `tg_mod_en_sel` or `tg_data_mode`



Note: Presentation applies to the ML605

Adjust Data Pattern using VIO Console

- Error is now cleared



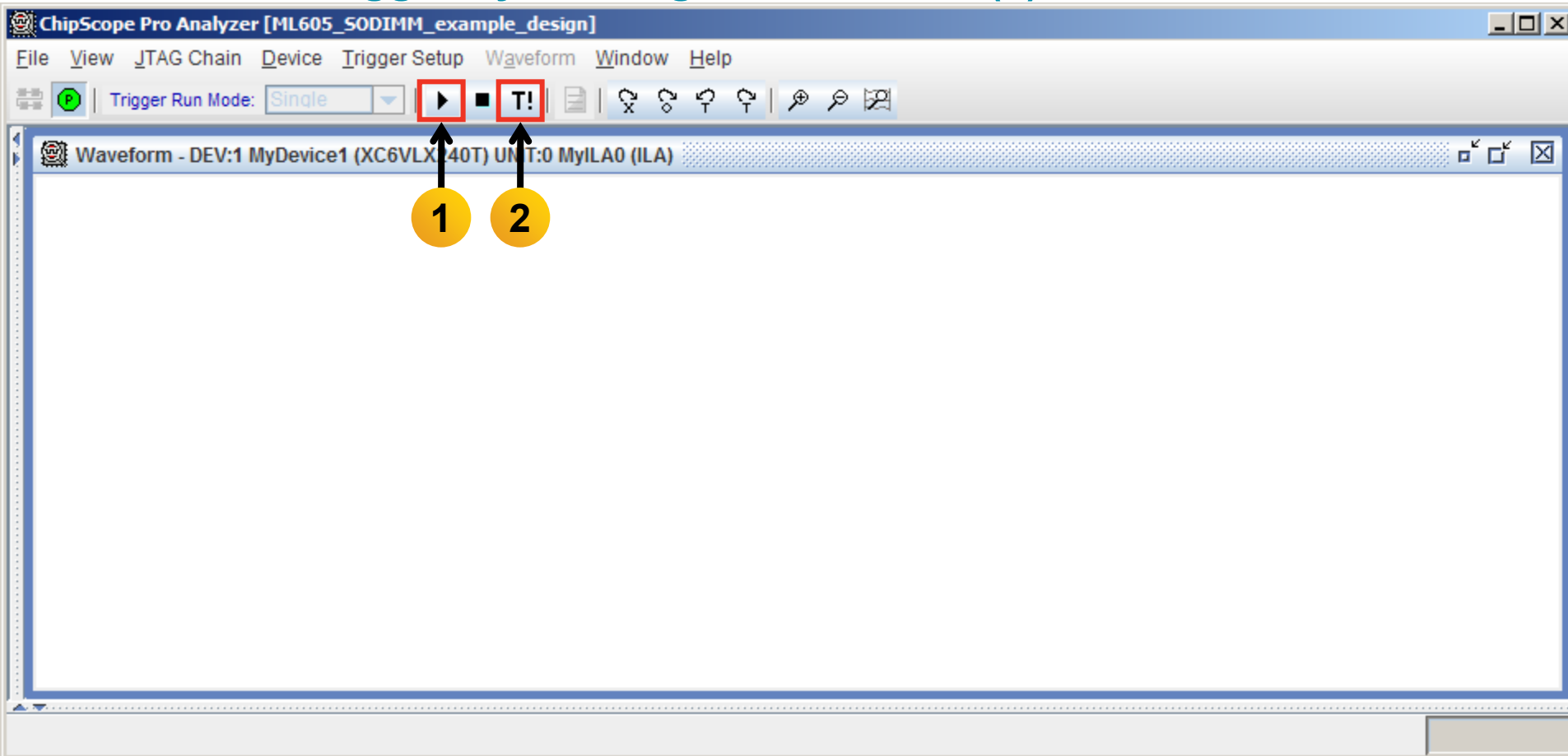
The screenshot shows the ChipScope Pro Analyzer interface for a project named 'ML605_SODIMM_example_design'. The VIO Console window is active, displaying a list of bus signals and their current values. The 'error' signal is shown as a grey circle, indicating it is cleared. Other signals like 'dbg_rdlvl_done' and 'dfi_init_complete' are shown as green circles, indicating they are active or completed. The 'compare_count' is 0, and various delay tap counts are shown in hexadecimal (FF, 0D, 05, 0E, 06).

Bus/Signal	Value
dbg_rdlvl_done[0]	
dbg_rdlvl_done[1]	
dfi_init_complete	
rst_pll_ck_fb	
error	
compare_count	0
dbg_wl_dqs_inverted	FF
dbg_wl_odelay_dqs_tap_cnt_0	0D
dbg_wl_odelay_dq_tap_cnt_0	05
dbg_wl_odelay_dqs_tap_cnt_1	0E
dbg_wl_odelay_dq_tap_cnt_1	06

DONE

Adjust Data Pattern using VIO Console

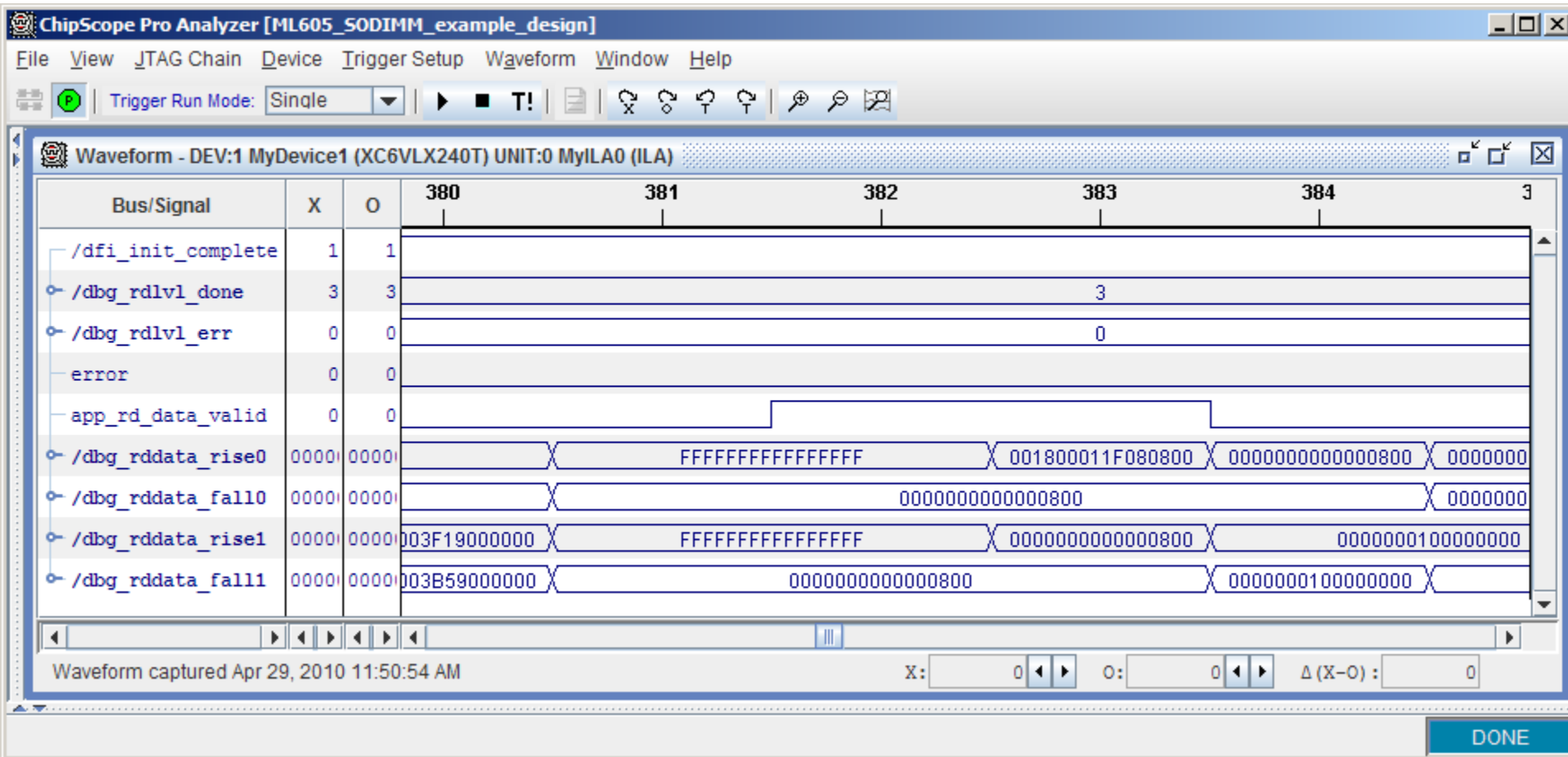
- Click on Waveform; click the Arm Trigger button (1)
- Force a trigger by clicking the T! button (2)



Adjust Data Pattern using VIO Console

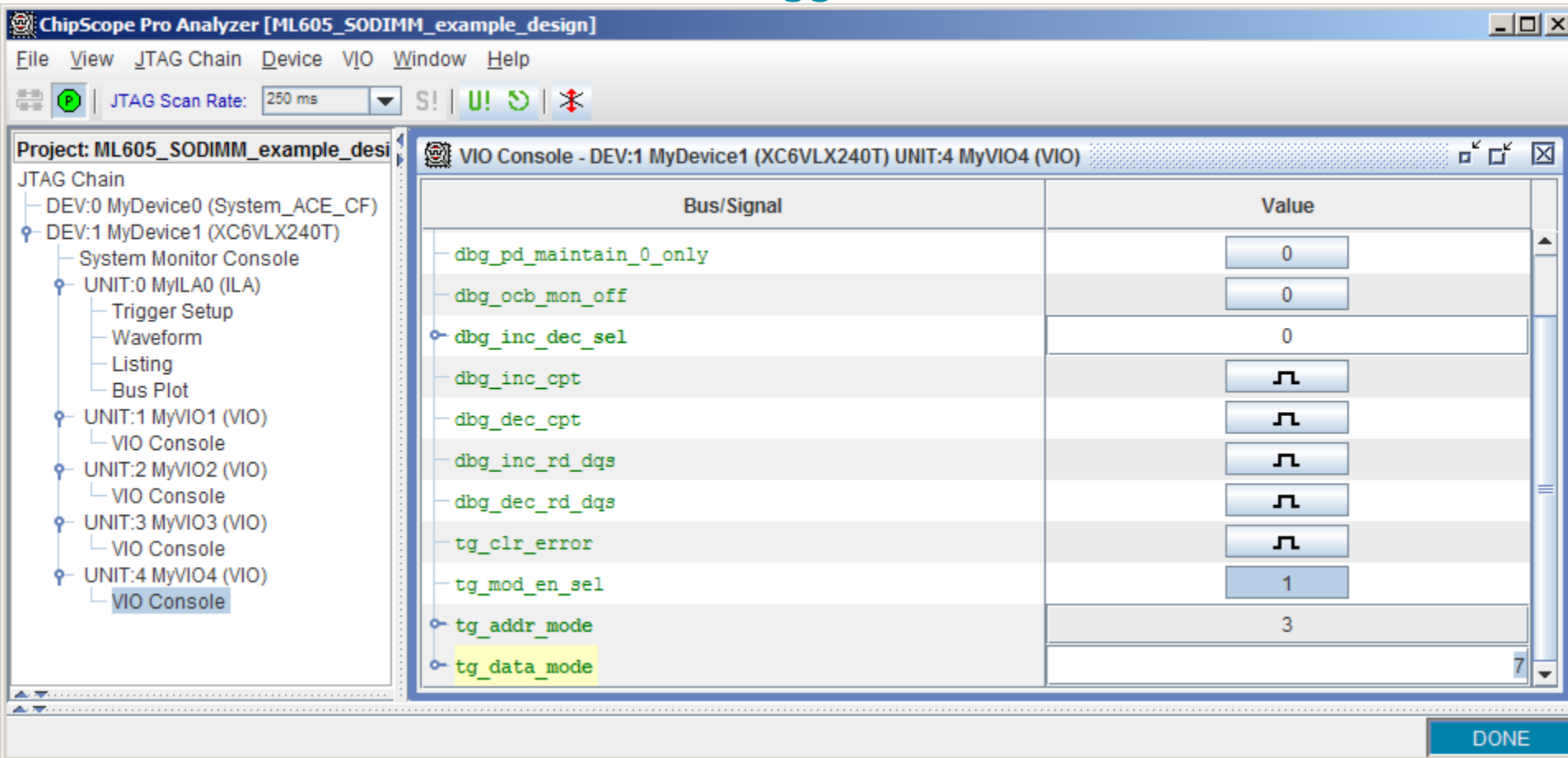
▪ Hammer PRBS Data Mode

- 64 bit DQ data bus hammer pattern



Adjust Data Pattern using VIO Console

- Set `tg_data_mode` to “7” for PRBS data pattern
- Push CPU Reset, click Arm Trigger button, click T! button



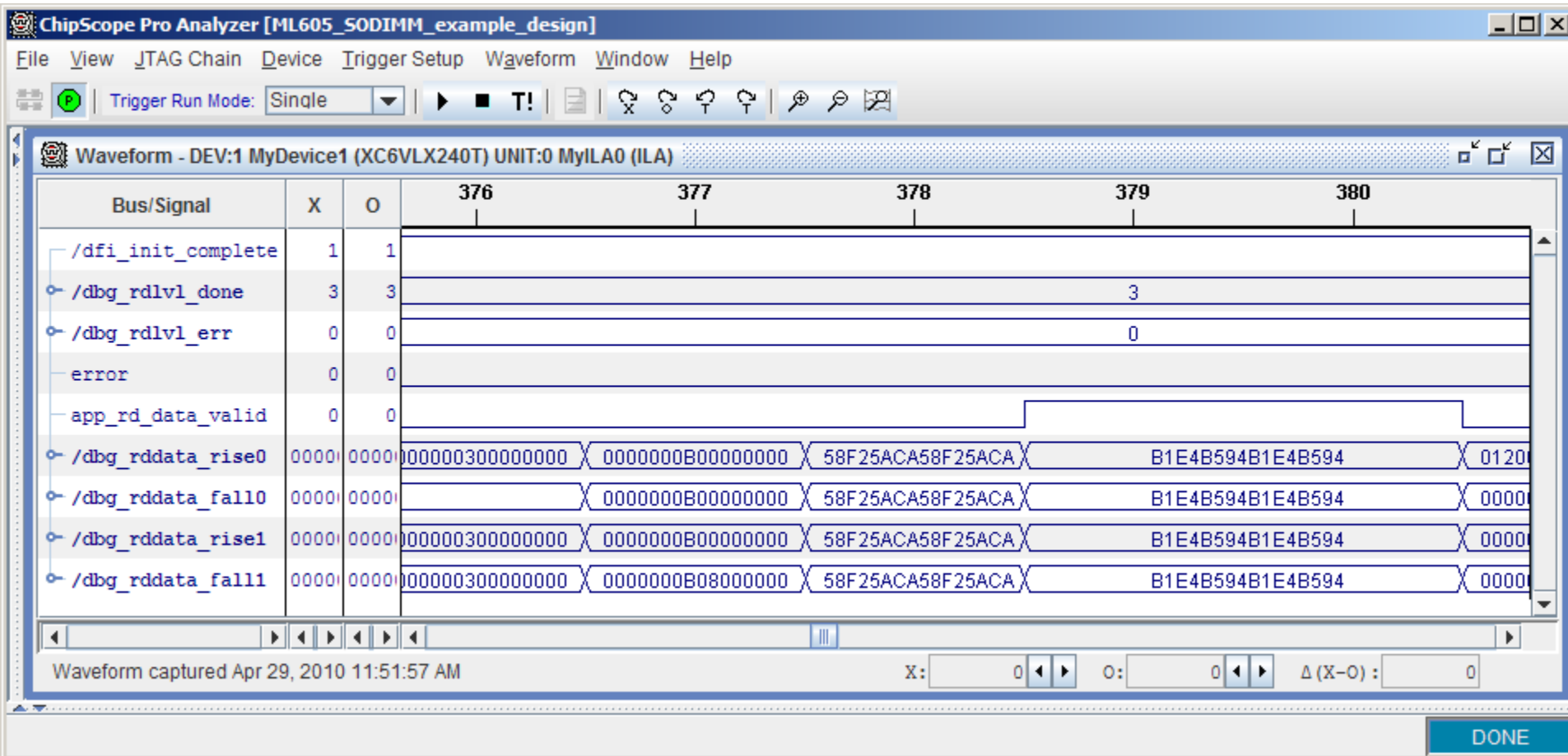
The screenshot shows the ChipScope Pro Analyzer interface. The VIO Console window is open, displaying a list of bus signals and their current values. The signal `tg_data_mode` is highlighted in yellow, and its value is set to 7. The signal `tg_mod_en_sel` is set to 1, and `tg_addr_mode` is set to 3. The other signals are set to 0 or have a square wave icon.

Bus/Signal	Value
<code>dbg_pd_maintain_0_only</code>	0
<code>dbg_ocb_mon_off</code>	0
<code>dbg_inc_dec_sel</code>	0
<code>dbg_inc_cpt</code>	⏏
<code>dbg_dec_cpt</code>	⏏
<code>dbg_inc_rd_dqs</code>	⏏
<code>dbg_dec_rd_dqs</code>	⏏
<code>tg_clr_error</code>	⏏
<code>tg_mod_en_sel</code>	1
<code>tg_addr_mode</code>	3
<code>tg_data_mode</code>	7

DONE

Adjust Data Pattern using VIO Console

▪ PRBS Data Mode



DONE

Example Design VIO Consoles

- **Useful for PHY layer logic debug and status**
- **Available if “debug” option is checked in MIG GUI**
 - Monitor PHY outputs
 - Status of write calibration
 - Status of read calibration
 - Phase detector control
 - Read data capture clock adjustment
 - Disable selected PHY features
- **Reference documentation in UG406**
 - “PHY Layer Debug Port” section
 - Table 1-25 for signal definitions and descriptions
- **VIO port assignments (4 cores) defined in “example_top.v”**

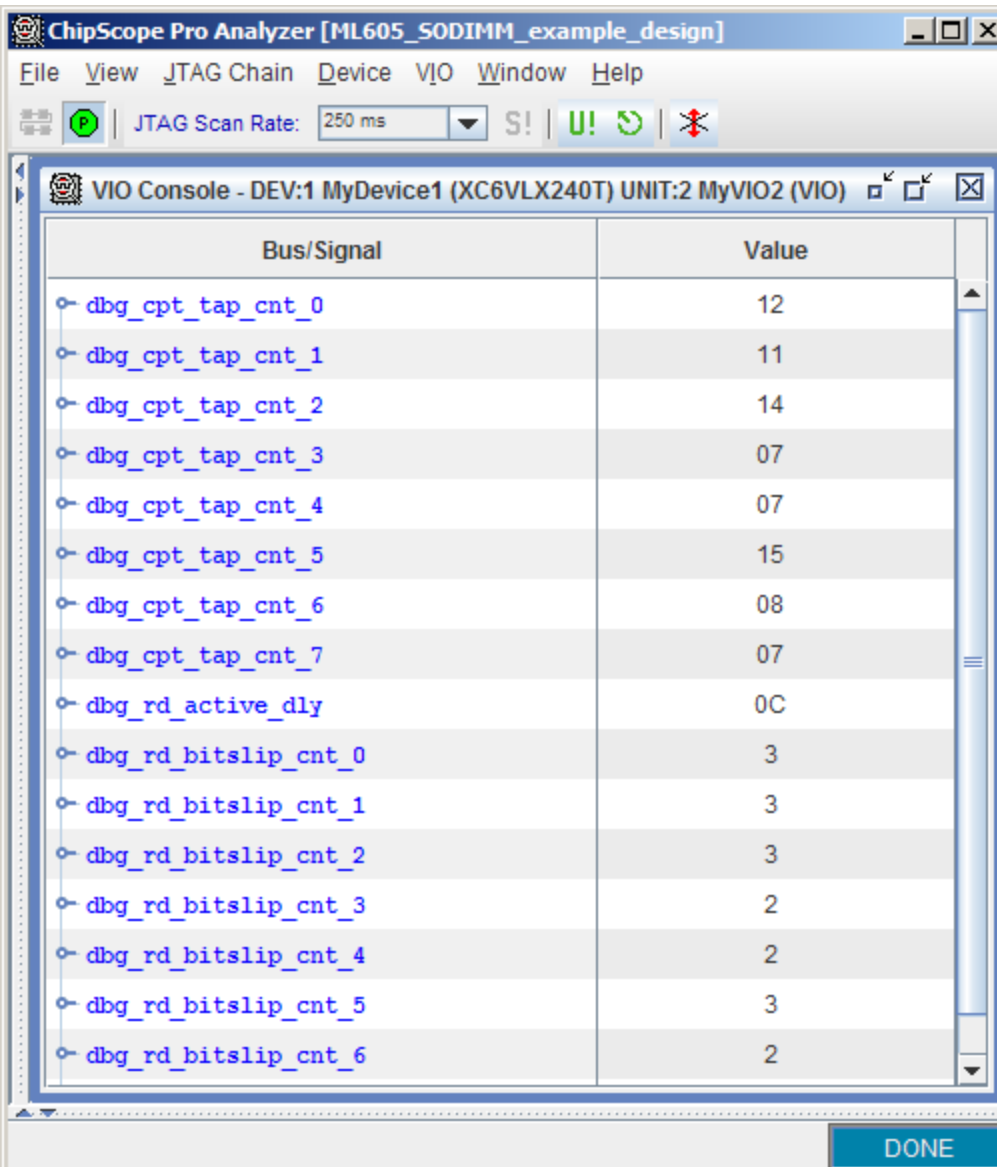
Example Design VIO Consoles

Bus/Signal	Value
dbg_rdlvl_done[0]	●
dbg_rdlvl_done[1]	●
dfi_init_complete	●
rst_pll_ck_fb	●
error	●
compare_count	0
dbg_wl_dqs_inverted	FF
dbg_wl_odelay_dqs_tap_cnt_0	0D
dbg_wl_odelay_dq_tap_cnt_0	05
dbg_wl_odelay_dqs_tap_cnt_1	0E
dbg_wl_odelay_dq_tap_cnt_1	06
dbg_wl_odelay_dqs_tap_cnt_2	0D
dbg_wl_odelay_dq_tap_cnt_2	05
dbg_wl_odelay_dqs_tap_cnt_3	0E
dbg_wl_odelay_dq_tap_cnt_3	06
dbg_wl_odelay_dqs_tap_cnt_4	0F

■ VIO Console 1

- Write Path Calibration Status
- Read Leveling Done, Read Leveling Error
- Initialization complete, PLL reset
- Note: Press CPU RESET to clear error status in this VIO console

Example Design VIO Consoles



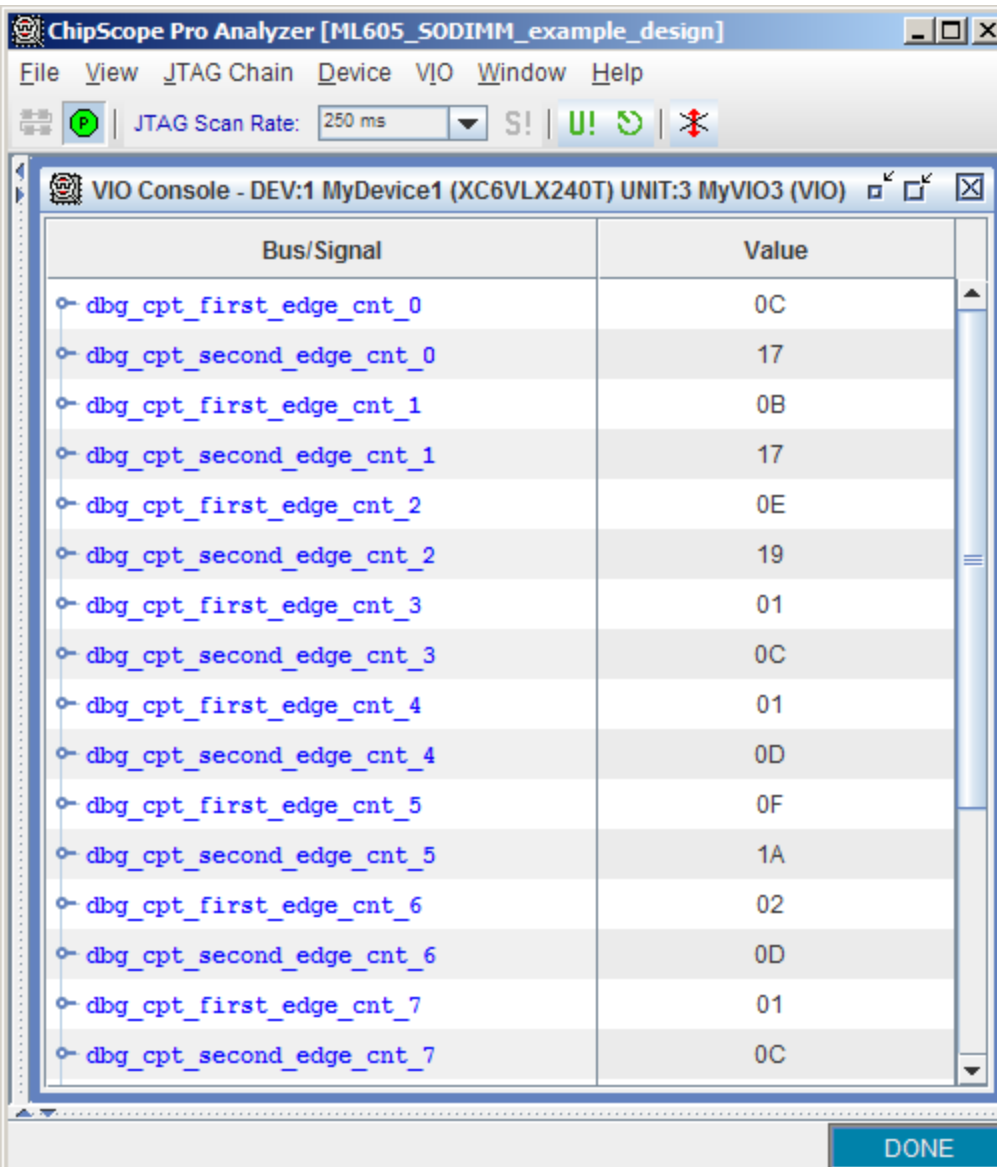
The screenshot shows the ChipScope Pro Analyzer interface. The main window is titled "VIO Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:2 MyVIO2 (VIO)". It displays a table with two columns: "Bus/Signal" and "Value". The table contains 15 rows of data, including tap counts and read path bit slips. A "DONE" button is visible at the bottom right of the console window.

Bus/Signal	Value
dbg_cpt_tap_cnt_0	12
dbg_cpt_tap_cnt_1	11
dbg_cpt_tap_cnt_2	14
dbg_cpt_tap_cnt_3	07
dbg_cpt_tap_cnt_4	07
dbg_cpt_tap_cnt_5	15
dbg_cpt_tap_cnt_6	08
dbg_cpt_tap_cnt_7	07
dbg_rd_active_dly	0C
dbg_rd_bitslip_cnt_0	3
dbg_rd_bitslip_cnt_1	3
dbg_rd_bitslip_cnt_2	3
dbg_rd_bitslip_cnt_3	2
dbg_rd_bitslip_cnt_4	2
dbg_rd_bitslip_cnt_5	3
dbg_rd_bitslip_cnt_6	2

- **VIO Console 2 & VIO Console 3**

- Read Path Calibration Status

Example Design VIO Consoles



The screenshot shows the ChipScope Pro Analyzer interface. The main window is titled "VIO Console - DEV:1 MyDevice1 (XC6VLX240T) UNIT:3 MyVIO3 (VIO)". It displays a table with two columns: "Bus/Signal" and "Value". The table contains 14 rows of data, each with a small circular icon to the left of the signal name. The values are hexadecimal numbers ranging from 0C to 0D.

Bus/Signal	Value
dbg_cpt_first_edge_cnt_0	0C
dbg_cpt_second_edge_cnt_0	17
dbg_cpt_first_edge_cnt_1	0B
dbg_cpt_second_edge_cnt_1	17
dbg_cpt_first_edge_cnt_2	0E
dbg_cpt_second_edge_cnt_2	19
dbg_cpt_first_edge_cnt_3	01
dbg_cpt_second_edge_cnt_3	0C
dbg_cpt_first_edge_cnt_4	01
dbg_cpt_second_edge_cnt_4	0D
dbg_cpt_first_edge_cnt_5	0F
dbg_cpt_second_edge_cnt_5	1A
dbg_cpt_first_edge_cnt_6	02
dbg_cpt_second_edge_cnt_6	0D
dbg_cpt_first_edge_cnt_7	01
dbg_cpt_second_edge_cnt_7	0C

A "DONE" button is visible at the bottom right of the console window.

■ VIO Console 2 & VIO Console 3

- Read Path Calibration Status

Example Design VIO Consoles

Bus/Signal	Value
dbg_pd_off	0
dbg_pd_maintain_off	0
dbg_pd_maintain_0_only	0
dbg_ocb_mon_off	0
dbg_inc_dec_sel	0
dbg_inc_cpt	
dbg_dec_cpt	
dbg_inc_rd_dqs	
dbg_dec_rd_dqs	
tg_clr_error	
tg_mod_en_sel	1
tg_addr_mode	3
tg_data_mode	7

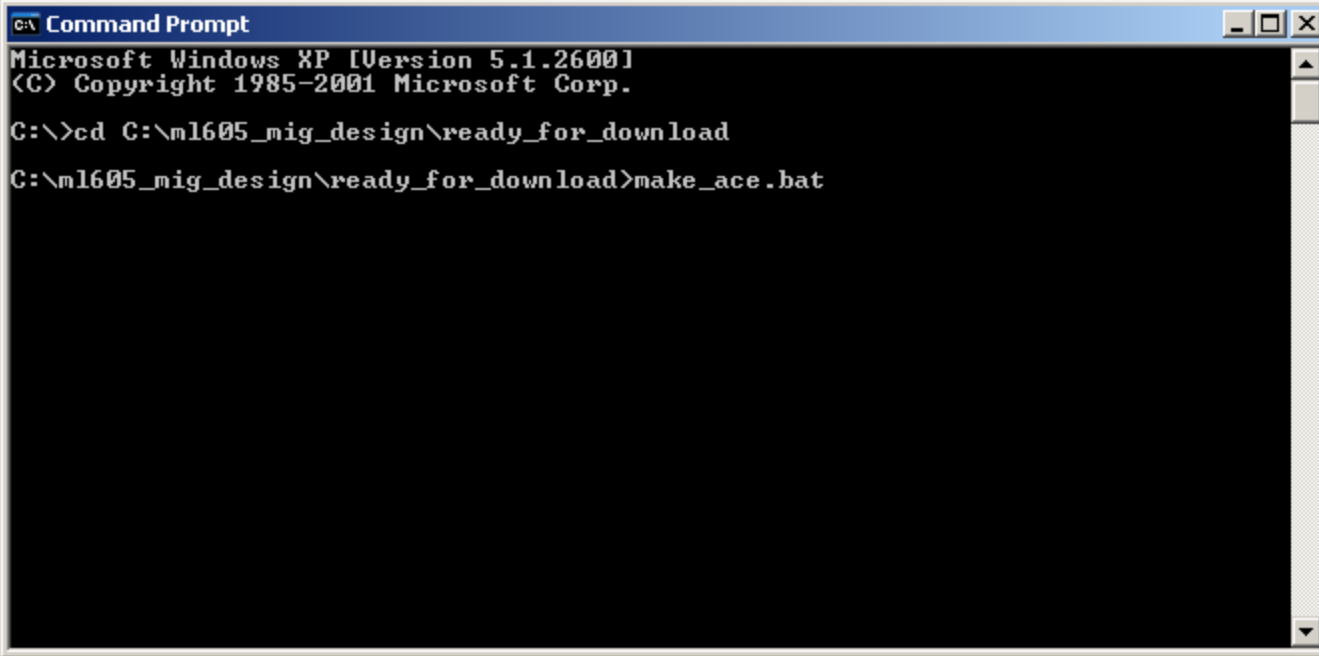
■ VIO Console 4

- Phase Detector Controls
- Read Data Capture Clock Adjustment

Generate MIG ACE File (Optional)

- Type these commands in a windows command shell:

```
cd C:\ml605_mig_design\ready_for_download  
make_ace.bat
```



```
C:\ Command Prompt  
Microsoft Windows XP [Version 5.1.2600]  
(C) Copyright 1985-2001 Microsoft Corp.  
C:\>cd C:\ml605_mig_design\ready_for_download  
C:\ml605_mig_design\ready_for_download>make_ace.bat
```

References

References

▪ Virtex-6 Memory

- Virtex-6 FPGA Memory Interface Solutions User Guide – UG406

http://www.xilinx.com/support/documentation/ip_documentation/ug406.pdf

- Virtex-6 FPGA Memory Interface Solutions – DS186

http://www.xilinx.com/support/documentation/ip_documentation/ds186.pdf

Documentation

Documentation

- **Virtex-6**

- Virtex-6 FPGA Family

<http://www.xilinx.com/products/virtex6/index.htm>

- **ML605 Documentation**

- Virtex-6 FPGA ML605 Evaluation Kit

<http://www.xilinx.com/products/devkits/EK-V6-ML605-G.htm>

- ML605 Hardware User Guide

http://www.xilinx.com/support/documentation/boards_and_kits/ug534.pdf

- ML605 Reference Design User Guide

http://www.xilinx.com/support/documentation/boards_and_kits/ug535.pdf