

SSD1322

Advance Information

480 x 128, Dot Matrix High Power OLED/PLED Segment/Common Driver with Controller

This document contains information on a new product. Specifications and information herein are subject to change without notice.

<http://www.solomon-systech.com>

SSD1322

Rev 1.2

P 1/60

Jul 2010

Copyright © 2010 Solomon Systech Limited

Appendix: IC Revision history of SSD1322 Specification

| Version | Change Items | Effective Date |
|----------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|
| 1.0 | <ol style="list-style-type: none"> 1. Changed to Advance Information 2. Revised the typo errors on commands BBh and BEh (Section 9) 3. Amended the default OSCFREQ[3:0] of command B3h from 1100b to 0101b (Section 9) 4. Updated the DC Characteristics table (Section 12) 5. Updated the AC Characteristics table (Section 13) 6. Revise Table 13-5 & Figure 13-4 (3 wire SPI) | 23-Jul-08 |
| 1.1 | <ol style="list-style-type: none"> 1. Updated the ordering P/N from SSD1322Z to SSD1322Z2 (P.7) and corresponding information (Section 5) 2. Updated the application examples (P.55, 56) 3. Added SSD1322Z2 die tray information (Section 15.2) | 10-Sep-08 |
| 1.2 | <ol style="list-style-type: none"> 1. Revise typo in Section 3 : No. of SPH from 4 to 5 (P.7) 2. Revise die thickness tolerance from $\pm 25\mu\text{m}$ to $\pm 15\mu\text{m}$ on Table 3-1 (P.7) & Fig 5-1(P.9) 3. Added +/- 0.05mm tolerance for Die Size (after sawing) and revise bump size typo in Section 5 (P.9) 4. Update Table 3-2: SSD1322Z2 Bump Die Pad Coordinates (p.10) 5. Update Power On sequence (P.30) 6. Updated P/N from SSD1322Z to SSD1322Z2 in Fig 10-6 & 10-7 (P.41) 7. Revised a typo on the command description of command ABh (P.45) 8. Add alignment mark detail of SSD1322UR1 in Fig 15-1 (P.57) 9. Revised disclaimer (P.60) | 13-Jul-10 |

CONTENTS

| | | |
|-----------|------------------------------------------------------------|-----------|
| 1 | GENERAL DESCRIPTION | 7 |
| 2 | FEATURES | 7 |
| 3 | ORDERING INFORMATION | 7 |
| 4 | BLOCK DIAGRAM | 8 |
| 5 | DIE PAD FLOOR PLAN | 9 |
| 6 | PIN ARRANGEMENT | 13 |
| 6.1 | SSD1322UR1 PIN ASSIGNMENT | 13 |
| 7 | PIN DESCRIPTIONS | 15 |
| 8 | FUNCTIONAL BLOCK DESCRIPTIONS | 18 |
| 8.1 | MCU INTERFACE | 18 |
| 8.1.1 | MCU Parallel 6800-series Interface | 18 |
| 8.1.2 | MCU Parallel 8080-series Interface | 19 |
| 8.1.3 | MCU Serial Interface (4-wire SPI) | 20 |
| 8.1.4 | MCU Serial Interface (3-wire SPI) | 21 |
| 8.2 | RESET CIRCUIT | 22 |
| 8.3 | GDDRAM | 22 |
| 8.3.1 | GDDRAM structure in Gray Scale mode | 22 |
| 8.3.2 | Data bus to RAM mapping | 22 |
| 8.4 | COMMAND DECODER | 23 |
| 8.5 | OSCILLATOR & TIMING GENERATOR | 23 |
| 8.6 | SEG/COM DRIVING BLOCK | 24 |
| 8.7 | SEG / COM DRIVER | 25 |
| 8.8 | GRAY SCALE DECODER | 29 |
| 8.9 | POWER ON AND OFF SEQUENCE | 30 |
| 8.10 | V _{DD} REGULATOR | 31 |
| 9 | COMMAND TABLE | 32 |
| 10 | COMMAND | 37 |
| 10.1.1 | Enable Gray Scale Table (00h) | 37 |
| 10.1.2 | Set Column Address (15h) | 37 |
| 10.1.3 | Write RAM Command (5Ch) | 37 |
| 10.1.4 | Read RAM Command (5Dh) | 37 |
| 10.1.5 | Set Row Address (75h) | 38 |
| 10.1.6 | Set Re-map & Dual COM Line Mode (A0h) | 39 |
| 10.1.7 | Set Display Start Line (A1h) | 42 |
| 10.1.8 | Set Display Offset (A2h) | 43 |
| 10.1.9 | Set Display Mode (A4h ~ A7h) | 44 |
| 10.1.10 | Enable Partial Display (A8h) | 45 |
| 10.1.11 | Exit Partial Display (A9h) | 45 |
| 10.1.12 | Set Function selection (ABh) | 45 |
| 10.1.13 | Set Display ON/OFF (AEh / AFh) | 45 |
| 10.1.14 | Set Phase Length (B1h) | 45 |
| 10.1.15 | Set Front Clock Divider / Oscillator Frequency (B3h) | 45 |
| 10.1.16 | Display Enhancement A (B4h) | 46 |
| 10.1.17 | Set GPIO (B5h) | 46 |
| 10.1.18 | Set Second Pre-charge period (B6h) | 46 |
| 10.1.19 | Set Gray Scale Table (B8h) | 46 |
| 10.1.20 | Select Default Linear Gray Scale Table (B9h) | 46 |
| 10.1.21 | Set Pre-charge voltage (BBh) | 46 |
| 10.1.22 | Set V _{COMH} Voltage (BEh) | 47 |
| 10.1.23 | Set Contrast Current (C1h) | 47 |

| | | |
|-----------|-------------------------------------|-----------|
| 10.1.24 | Master Current Control (C7h)..... | 47 |
| 10.1.25 | Set Multiplex Ratio (CAh)..... | 47 |
| 10.1.26 | Display Enhancement B (DIh)..... | 47 |
| 10.1.27 | Set Command Lock (FDh)..... | 47 |
| 11 | MAXIMUM RATINGS..... | 48 |
| 12 | DC CHARACTERISTICS..... | 49 |
| 13 | AC CHARACTERISTICS..... | 50 |
| 14 | APPLICATION EXAMPLES | 55 |
| 15 | PACKAGE INFORMATION..... | 57 |
| 15.1 | SSD1322UR1 DETAIL DIMENSION | 57 |
| 15.2 | SSD1322Z2 DIE TRAY INFORMATION..... | 58 |

TABLES

| | |
|-------------------------------------------------------------------------------|----|
| 4. UPDATE TABLE 3-1: SSD1322Z2 BUMP DIE PAD COORDINATES (P.10)..... | ii |
| 4. UPDATE TABLE 3-2: SSD1322Z2 BUMP DIE PAD COORDINATES (P.10)..... | 2 |
| TABLE 3-1 : ORDERING INFORMATION | 7 |
| TABLE 5-1: SSD1322Z2 BUMP DIE PAD COORDINATES..... | 10 |
| TABLE 6-1: SSD1322UR1 PIN ASSIGNMENT TABLE | 14 |
| TABLE 7-1: SSD1322 PIN DESCRIPTION | 15 |
| TABLE 7-2 : BUS INTERFACE SELECTION | 15 |
| TABLE 8-1 : MCU INTERFACE ASSIGNMENT UNDER DIFFERENT BUS INTERFACE MODE | 18 |
| TABLE 8-2 : CONTROL PINS OF 6800 INTERFACE..... | 18 |
| TABLE 8-3 : CONTROL PINS OF 8080 INTERFACE..... | 20 |
| TABLE 8-4 : CONTROL PINS OF 4-WIRE SERIAL INTERFACE..... | 20 |
| TABLE 8-5: CONTROL PINS OF 3-WIRE SERIAL INTERFACE..... | 21 |
| TABLE 8-6 : GDDRAM IN GRAY SCALE MODE (RESET) | 22 |
| TABLE 8-7 : DATA BUS USAGE | 22 |
| TABLE 9-1 : COMMAND TABLE | 32 |
| TABLE 11-1 : MAXIMUM RATINGS | 48 |
| TABLE 12-1 : DC CHARACTERISTICS | 49 |
| TABLE 13-1 : AC CHARACTERISTICS | 50 |
| TABLE 13-2 : 6800-SERIES MCU PARALLEL INTERFACE TIMING CHARACTERISTICS..... | 51 |
| TABLE 13-3 : 8080-SERIES MCU PARALLEL INTERFACE TIMING CHARACTERISTICS..... | 52 |
| TABLE 13-4 : SERIAL INTERFACE TIMING CHARACTERISTICS (4-WIRE SPI) | 53 |
| TABLE 13-5: SERIAL INTERFACE TIMING CHARACTERISTICS (3-WIRE SPI)..... | 54 |
| TABLE 15-1: SSD1322Z2 DIE TRAY DIMENSIONS | 59 |

FIGURES

| | |
|-------------------------------------------------------------------------------------------------------------------------------------|----|
| FIGURE 4-1 : SSD1322 BLOCK DIAGRAM..... | 8 |
| FIGURE 5-1: SSD1322Z2 DIE DRAWING | 9 |
| FIGURE 5-2: SSD1322Z2 ALIGNMENT MARK DIMENSION | 9 |
| FIGURE 6-1: SSD1322UR1 PIN ASSIGNMENT | 13 |
| FIGURE 8-1 : DATA READ BACK PROCEDURE - INSERTION OF DUMMY READ | 19 |
| FIGURE 8-2 : EXAMPLE OF WRITE PROCEDURE IN 8080 PARALLEL INTERFACE MODE..... | 19 |
| FIGURE 8-3 : EXAMPLE OF READ PROCEDURE IN 8080 PARALLEL INTERFACE MODE | 19 |
| FIGURE 8-4 : DISPLAY DATA READ BACK PROCEDURE - INSERTION OF DUMMY READ | 20 |
| FIGURE 8-5 : WRITE PROCEDURE IN 4-WIRE SERIAL INTERFACE MODE..... | 21 |
| FIGURE 8-6: WRITE PROCEDURE IN 3-WIRE SERIAL INTERFACE MODE..... | 21 |
| FIGURE 8-7 : OSCILLATOR CIRCUIT | 23 |
| FIGURE 8-8 : I _{REF} CURRENT SETTING BY RESISTOR VALUE | 24 |
| FIGURE 8-9 : SEGMENT AND COMMON DRIVER BLOCK DIAGRAM – SINGLE COM MODE | 25 |
| FIGURE 8-10 : SEGMENT AND COMMON DRIVER BLOCK DIAGRAM – DUAL COM MODE..... | 26 |
| FIGURE 8-11 : SEGMENT AND COMMON DRIVER SIGNAL WAVEFORM | 27 |
| FIGURE 8-12 : GRAY SCALE CONTROL BY PWM IN SEGMENT | 28 |
| FIGURE 8-13 : RELATION BETWEEN GDDRAM CONTENT AND GRAY SCALE TABLE ENTRY (UNDER COMMAND B9H ENABLE LINEAR GRAY SCALE TABLE)..... | 29 |
| FIGURE 8-14 : THE POWER ON SEQUENCE..... | 30 |
| FIGURE 8-15 : THE POWER OFF SEQUENCE..... | 30 |
| FIGURE 8-16 V _{CI} > 2.6V, V _{DD} REGULATOR ENABLE PIN CONNECTION SCHEME..... | 31 |
| FIGURE 8-17 V _{DD} REGULATOR DISABLE PIN CONNECTION SCHEME | 31 |
| FIGURE 10-110-2 : EXAMPLE OF COLUMN AND ROW ADDRESS POINTER MOVEMENT (GRAY SCALE MODE)..... | 38 |
| FIGURE 10-3 : ADDRESS POINTER MOVEMENT OF HORIZONTAL ADDRESS INCREMENT MODE | 39 |
| FIGURE 10-4: ADDRESS POINTER MOVEMENT OF VERTICAL ADDRESS INCREMENT MODE..... | 39 |
| FIGURE 10-5: GDDRAM IN GRAY SCALE MODE WITH OR WITHOUT COLUMN ADDRESS (A[1]) & NIBBLE REMAPPING (A[2]) | 40 |
| FIGURE 10-6 : COM PINS HARDWARE CONFIGURATION – 1 (MUX RATIO: 128)..... | 41 |
| FIGURE 10-7 : COM PINS HARDWARE CONFIGURATION – 2 (MUX RATIO: 64)..... | 41 |
| FIGURE 10-8 : EXAMPLE OF SET DISPLAY START LINE WITH NO REMAP | 42 |
| FIGURE 10-9 : EXAMPLE OF SET DISPLAY OFFSET WITH NO REMAP | 43 |
| FIGURE 10-10 : EXAMPLE OF NORMAL DISPLAY | 44 |
| FIGURE 10-11 : EXAMPLE OF ENTIRE DISPLAY ON | 44 |
| FIGURE 10-12 : EXAMPLE OF ENTIRE DISPLAY OFF..... | 44 |
| FIGURE 10-13 : EXAMPLE OF INVERSE DISPLAY | 44 |
| FIGURE 10-14 : EXAMPLE OF PARTIAL MODE DISPLAY | 45 |
| FIGURE 10-15 : EXAMPLE OF GAMMA CORRECTION BY GAMMA LOOK UP TABLE SETTING..... | 46 |
| FIGURE 13-1 : 6800-SERIES MCU PARALLEL INTERFACE CHARACTERISTICS..... | 51 |
| FIGURE 13-2 : 8080-SERIES MCU PARALLEL INTERFACE CHARACTERISTICS..... | 52 |
| FIGURE 13-3 : SERIAL INTERFACE CHARACTERISTICS (4-WIRE SPI)..... | 53 |
| FIGURE 13-4: SERIAL INTERFACE CHARACTERISTICS (3-WIRE SPI) | 54 |
| FIGURE 14-1 : SSD1322 APPLICATION EXAMPLE FOR 8-BIT 6800-PARALLEL INTERFACE MODE (INTERNAL REGULATED V _{DD}) | 55 |
| FIGURE 14-2 : SSD1322 APPLICATION EXAMPLE FOR 8-BIT 6800-PARALLEL INTERFACE, DUAL COM MODE (INTERNAL V _{DD}) | 56 |
| FIGURE 15-1: SSD1322UR1 DETAIL DIMENSION | 57 |
| FIGURE 15-2: SSD1322Z2 DIE TRAY DRAWING | 58 |

1 GENERAL DESCRIPTION

SSD1322 is a single-chip CMOS OLED/PLED driver with controller for organic/polymer light emitting diode dot-matrix graphic display system. It consists of 480 segments and 128 commons. This IC is designed for Common Cathode type OLED/PLED panel.

SSD1322 displays data directly from its internal 480 x 128 x 4 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from general MCU through the hardware selectable 6800-/8080-series compatible Parallel Interface or Serial Peripheral Interface. This driver IC has a 256 steps contrast control and can be widely used in many applications such as automotive and industrial control panel.

2 FEATURES

- Resolution: 480 x 128 dot matrix panel
- Power supply
 - $V_{DD} = 2.4V - 2.6V$ (Core V_{DD} power supply, can be regulated from V_{CI})
 - $V_{DDIO} = 1.65V - V_{CI}$ (MCU interface logic level)
 - $V_{CI} = 2.4V - 3.5V$ (Low voltage power supply)
 - $V_{CC} = 10.0V - 20.0V$ (Panel driving power supply)
- When V_{CI} is lower than 2.6V, V_{DD} should be supplied by external power source
- For matrix display
 - Segment maximum source current: 300uA
 - Common maximum sink current: 80mA
 - 256 step contrast brightness current control, 16 step master current control
- 16 gray scale levels supported by embedded 480 x 128 x 4 bit SRAM display buffer
- Selectable MCU Interfaces:
 - 8-bit 6800/8080-series parallel interface
 - 3/4-wire Serial Peripheral Interface
- Selectable Common current sinking mode:
 - Dual COM mode
 - Single COM mode
- 8-bit programmable Gray Scale Look Up Table
- High Power Protection
- Programmable Frame Rate and Multiplexing Ratio
- Row re-mapping and Column re-mapping
- Sleep mode current <10uA with ram data kept
- Operating temperature range -40°C to 85°C.

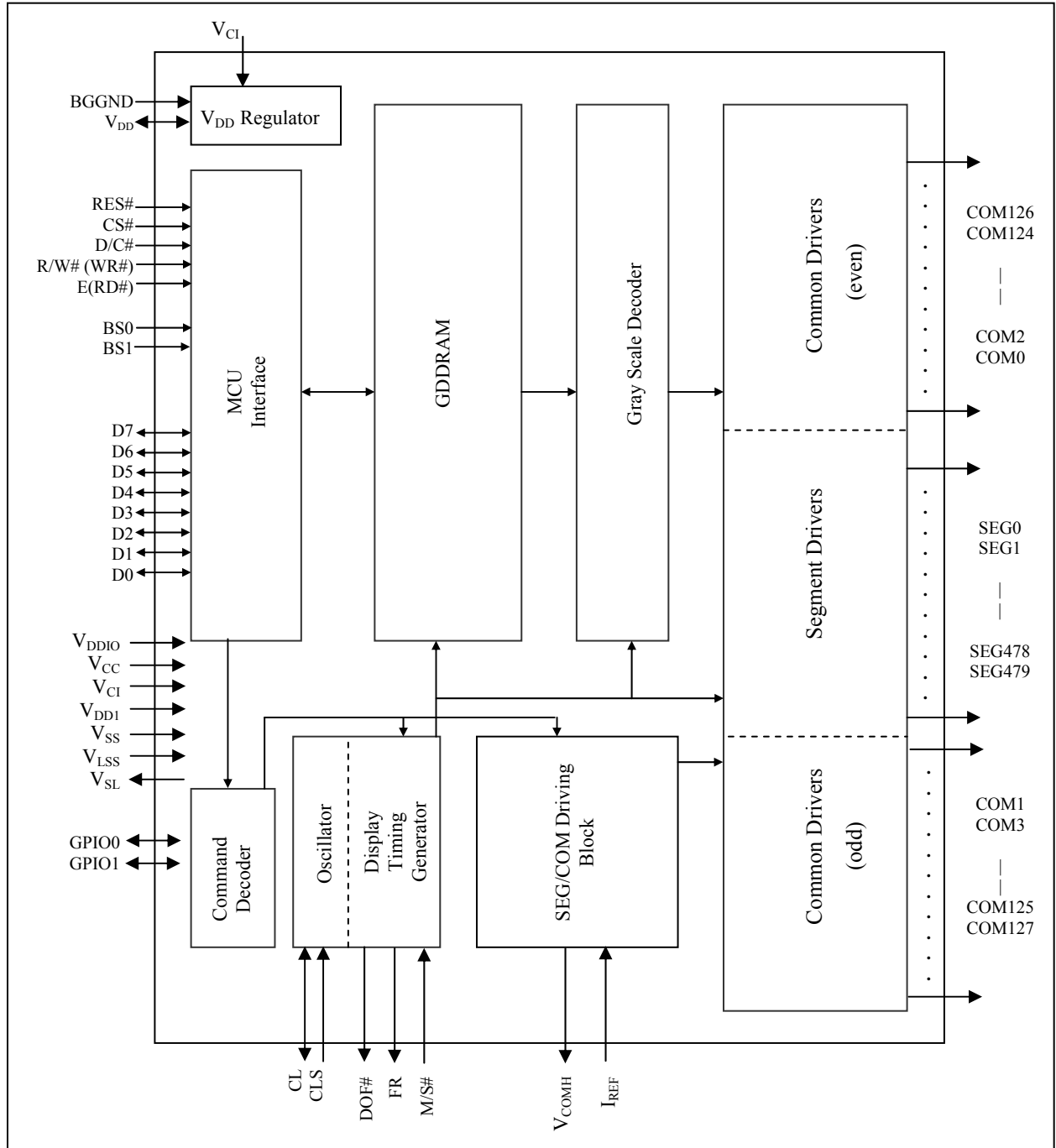
3 ORDERING INFORMATION

Table 3-1 : Ordering Information

| Ordering Part Number | SEG | COM | Package Form | Reference | Remark |
|----------------------|-----|---------------|---------------|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SSD1322Z2 | 480 | 128 | Gold bump Die | Page 9 | <ul style="list-style-type: none"> • Min SEG pitch: 25um • Min COM pitch: 35um • Die thickness: 300 +/- 15um |
| SSD1322UR1 | 256 | 64 (dual COM) | COF | Page 13, 57 | <ul style="list-style-type: none"> • 70mm film, 5 SPH • 8-bit 80/68/SPI interfaces • SEG, COM lead pitch 0.12mm x 0.999 = 0.11988mm • Also support 128 MUX (single COM) • Die thickness: 457 +/- 25um |

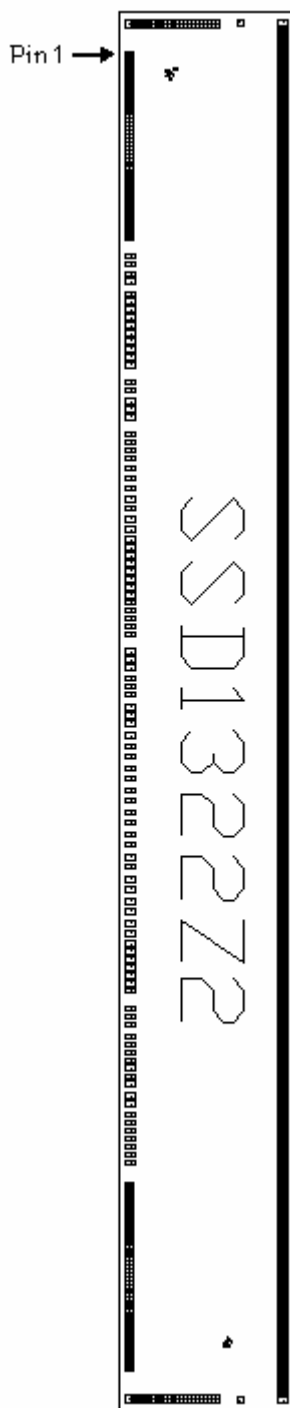
4 BLOCK DIAGRAM

Figure 4-1 : SSD1322 Block Diagram



5 DIE PAD FLOOR PLAN

Figure 5-1: SSD1322Z2 Die Drawing



| | |
|-------------------|-------------------------------------|
| Die size | 12.4 mm ± 0.05mm x 1.53 mm ± 0.05mm |
| Die thickness | 300 +/- 15um |
| Min I/O pad pitch | 70um |
| Min SEG pad pitch | 25um |
| Min COM pad pitch | 35um |
| Bump height | Nominal 15um |

| Bump size | | |
|------------------|-------|-------|
| Pad# | X[um] | Y[um] |
| 1-48, 146-193 | 26 | 60 |
| 195-216, 706-727 | 60 | 26 |
| 49-145 | 45 | 90 |
| 194, 728 | 60 | 50 |
| 217, 705 | 50 | 50 |
| 218, 704 | 50 | 96 |
| 219-703 | 16 | 96 |

| Alignment mark | Position | Size |
|----------------|--------------------|-------------|
| + shape | (5583.95,200.78) | 75um x 75um |
| + shape | (-5634.61,-309.88) | 75um x 75um |
| SSL Logo | (-5682.11,-258.98) | - |

(For details dimension please see Figure 5-2)

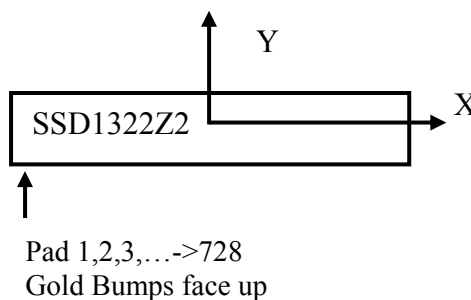


Figure 5-2: SSD1322Z2 alignment mark dimension

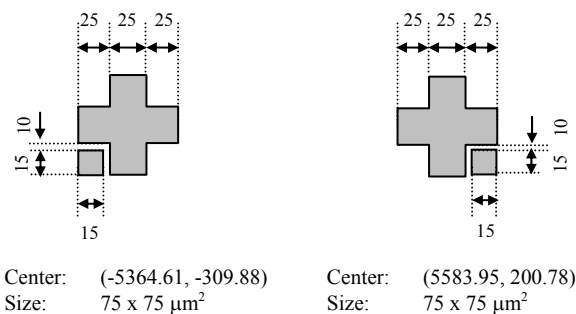


Table 5-1: SSD132Z2 Bump Die Pad Coordinates

| Pad no. | Pin name | X-pos | Y-pos | Pad no. | Pin name | X-pos | Y-pos | Pad no. | Pin name | X-pos | Y-pos | Pad no. | Pin name | X-pos | Y-pos |
|---------|----------|----------|---------|---------|-----------|----------|---------|---------|----------|---------|---------|---------|----------|-------|--------|
| 1 | VLSS | -5833.06 | -664.06 | 81 | RES# | -1381.06 | -654.15 | 161 | COM50 | 4708.06 | -664.06 | 241 | SEG22 | 5500 | 687.81 |
| 2 | VLSS | -5798.06 | -664.06 | 82 | CS# | -1311.06 | -654.15 | 162 | COM49 | 4743.06 | -664.06 | 242 | SEG23 | 5475 | 687.81 |
| 3 | COM84 | -5758.06 | -664.06 | 83 | D/C# | -1241.06 | -654.15 | 163 | COM48 | 4778.06 | -664.06 | 243 | SEG24 | 5450 | 687.81 |
| 4 | COM85 | -5723.06 | -664.06 | 84 | VSS | -1171.06 | -654.15 | 164 | COM47 | 4813.06 | -664.06 | 244 | SEG25 | 5425 | 687.81 |
| 5 | COM86 | -5688.06 | -664.06 | 85 | BS1 | -1101.06 | -654.15 | 165 | COM46 | 4848.06 | -664.06 | 245 | SEG26 | 5400 | 687.81 |
| 6 | COM87 | -5653.06 | -664.06 | 86 | VDDIO | -1031.06 | -654.15 | 166 | COM45 | 4883.06 | -664.06 | 246 | SEG27 | 5375 | 687.81 |
| 7 | COM88 | -5618.06 | -664.06 | 87 | BS0 | -961.06 | -654.15 | 167 | COM44 | 4918.06 | -664.06 | 247 | SEG28 | 5350 | 687.81 |
| 8 | COM89 | -5583.06 | -664.06 | 88 | VSS | -891.06 | -654.15 | 168 | COM43 | 4953.06 | -664.06 | 248 | SEG29 | 5325 | 687.81 |
| 9 | COM90 | -5548.06 | -664.06 | 89 | R/W#(WR#) | -821.06 | -654.15 | 169 | COM42 | 4988.06 | -664.06 | 249 | SEG30 | 5300 | 687.81 |
| 10 | COM91 | -5513.06 | -664.06 | 90 | E(RD#) | -751.06 | -654.15 | 170 | COM41 | 5023.06 | -664.06 | 250 | SEG31 | 5275 | 687.81 |
| 11 | COM92 | -5478.06 | -664.06 | 91 | VDDIO | -681.06 | -654.15 | 171 | COM40 | 5058.06 | -664.06 | 251 | SEG32 | 5250 | 687.81 |
| 12 | COM93 | -5443.06 | -664.06 | 92 | VDD1 | -528.06 | -654.15 | 172 | COM39 | 5093.06 | -664.06 | 252 | SEG33 | 5225 | 687.81 |
| 13 | COM94 | -5408.06 | -664.06 | 93 | VDD1 | -458.06 | -654.15 | 173 | COM38 | 5128.06 | -664.06 | 253 | SEG34 | 5200 | 687.81 |
| 14 | COM95 | -5373.06 | -664.06 | 94 | VDD1 | -388.06 | -654.15 | 174 | COM37 | 5163.06 | -664.06 | 254 | SEG35 | 5175 | 687.81 |
| 15 | COM96 | -5338.06 | -664.06 | 95 | VDD | -290.06 | -654.15 | 175 | COM36 | 5198.06 | -664.06 | 255 | SEG36 | 5150 | 687.81 |
| 16 | COM97 | -5303.06 | -664.06 | 96 | VDD | -220.06 | -654.15 | 176 | COM35 | 5233.06 | -664.06 | 256 | SEG37 | 5125 | 687.81 |
| 17 | COM98 | -5268.06 | -664.06 | 97 | VDD | -150.06 | -654.15 | 177 | COM34 | 5268.06 | -664.06 | 257 | SEG38 | 5100 | 687.81 |
| 18 | COM99 | -5233.06 | -664.06 | 98 | NC | -36.06 | -654.15 | 178 | COM33 | 5303.06 | -664.06 | 258 | SEG39 | 5075 | 687.81 |
| 19 | COM100 | -5198.06 | -664.06 | 99 | NC | 33.94 | -654.15 | 179 | COM32 | 5338.06 | -664.06 | 259 | SEG40 | 5050 | 687.81 |
| 20 | COM101 | -5163.06 | -664.06 | 100 | NC | 103.94 | -654.15 | 180 | COM31 | 5373.06 | -664.06 | 260 | SEG41 | 5025 | 687.81 |
| 21 | COM102 | -5128.06 | -664.06 | 101 | VCI | 217.94 | -654.15 | 181 | COM30 | 5408.06 | -664.06 | 261 | SEG42 | 5000 | 687.81 |
| 22 | COM103 | -5093.06 | -664.06 | 102 | D0 | 309.94 | -654.15 | 182 | COM29 | 5443.06 | -664.06 | 262 | SEG43 | 4975 | 687.81 |
| 23 | COM104 | -5058.06 | -664.06 | 103 | D1 | 395.94 | -654.15 | 183 | COM28 | 5478.06 | -664.06 | 263 | SEG44 | 4950 | 687.81 |
| 24 | COM105 | -5023.06 | -664.06 | 104 | D2 | 505.94 | -654.15 | 184 | COM27 | 5513.06 | -664.06 | 264 | SEG45 | 4925 | 687.81 |
| 25 | COM106 | -4988.06 | -664.06 | 105 | D3 | 591.94 | -654.15 | 185 | COM26 | 5548.06 | -664.06 | 265 | SEG46 | 4900 | 687.81 |
| 26 | COM107 | -4953.06 | -664.06 | 106 | D4 | 701.94 | -654.15 | 186 | COM25 | 5583.06 | -664.06 | 266 | SEG47 | 4875 | 687.81 |
| 27 | COM108 | -4918.06 | -664.06 | 107 | D5 | 787.94 | -654.15 | 187 | COM24 | 5618.06 | -664.06 | 267 | SEG48 | 4850 | 687.81 |
| 28 | COM109 | -4883.06 | -664.06 | 108 | D6 | 897.94 | -654.15 | 188 | COM23 | 5653.06 | -664.06 | 268 | SEG49 | 4825 | 687.81 |
| 29 | COM110 | -4848.06 | -664.06 | 109 | D7 | 983.94 | -654.15 | 189 | COM22 | 5688.06 | -664.06 | 269 | SEG50 | 4800 | 687.81 |
| 30 | COM111 | -4813.06 | -664.06 | 110 | DN0 | 1093.94 | -654.15 | 190 | COM21 | 5723.06 | -664.06 | 270 | SEG51 | 4775 | 687.81 |
| 31 | COM112 | -4778.06 | -664.06 | 111 | DN1 | 1179.94 | -654.15 | 191 | COM20 | 5758.06 | -664.06 | 271 | SEG52 | 4750 | 687.81 |
| 32 | COM113 | -4743.06 | -664.06 | 112 | DN2 | 1289.94 | -654.15 | 192 | VLSS | 5793.06 | -664.06 | 272 | SEG53 | 4725 | 687.81 |
| 33 | COM114 | -4708.06 | -664.06 | 113 | DN3 | 1375.94 | -654.15 | 193 | VLSS | 5828.06 | -664.06 | 273 | SEG54 | 4700 | 687.81 |
| 34 | COM115 | -4673.06 | -664.06 | 114 | DN4 | 1485.94 | -654.15 | 194 | VLSS | 6087.34 | -674.56 | 274 | SEG55 | 4675 | 687.81 |
| 35 | COM116 | -4638.06 | -664.06 | 115 | DN5 | 1571.94 | -654.15 | 195 | COM19 | 6087.34 | -627.06 | 275 | SEG56 | 4650 | 687.81 |
| 36 | COM117 | -4603.06 | -664.06 | 116 | DN6 | 1681.94 | -654.15 | 196 | COM18 | 6087.34 | -592.06 | 276 | SEG57 | 4625 | 687.81 |
| 37 | COM118 | -4568.06 | -664.06 | 117 | DN7 | 1767.94 | -654.15 | 197 | COM17 | 6087.34 | -557.06 | 277 | SEG58 | 4600 | 687.81 |
| 38 | COM119 | -4533.06 | -664.06 | 118 | DN8 | 1877.94 | -654.15 | 198 | COM16 | 6087.34 | -522.06 | 278 | SEG59 | 4575 | 687.81 |
| 39 | COM120 | -4498.06 | -664.06 | 119 | DN9 | 1963.94 | -654.15 | 199 | COM15 | 6087.34 | -487.06 | 279 | SEG60 | 4550 | 687.81 |
| 40 | COM121 | -4463.06 | -664.06 | 120 | VSS | 2055.94 | -654.15 | 200 | COM14 | 6087.34 | -452.06 | 280 | SEG61 | 4525 | 687.81 |
| 41 | COM122 | -4428.06 | -664.06 | 121 | BGGND | 2125.94 | -654.15 | 201 | COM13 | 6087.34 | -417.06 | 281 | SEG62 | 4500 | 687.81 |
| 42 | COM123 | -4393.06 | -664.06 | 122 | MS | 2195.94 | -654.15 | 202 | COM12 | 6087.34 | -382.06 | 282 | SEG63 | 4475 | 687.81 |
| 43 | COM124 | -4358.06 | -664.06 | 123 | CLS | 2265.94 | -654.15 | 203 | COM11 | 6087.34 | -347.06 | 283 | SEG64 | 4450 | 687.81 |
| 44 | COM125 | -4323.06 | -664.06 | 124 | VSL | 2335.94 | -654.15 | 204 | COM10 | 6087.34 | -312.06 | 284 | SEG65 | 4425 | 687.81 |
| 45 | COM126 | -4288.06 | -664.06 | 125 | VSL | 2405.94 | -654.15 | 205 | COM9 | 6087.34 | -277.06 | 285 | SEG66 | 4400 | 687.81 |
| 46 | COM127 | -4253.06 | -664.06 | 126 | VCI | 2475.94 | -654.15 | 206 | COM8 | 6087.34 | -242.06 | 286 | SEG67 | 4375 | 687.81 |
| 47 | VLSS | -4218.06 | -664.06 | 127 | VDDIO | 2628.94 | -654.15 | 207 | COM7 | 6087.34 | -207.06 | 287 | SEG68 | 4350 | 687.81 |
| 48 | VLSS | -4183.06 | -664.06 | 128 | VDDIO | 2698.94 | -654.15 | 208 | COM6 | 6087.34 | -172.06 | 288 | SEG69 | 4325 | 687.81 |
| 49 | VSS | -4033.06 | -654.15 | 129 | VDD | 2768.94 | -654.15 | 209 | COM5 | 6087.34 | -137.06 | 289 | SEG70 | 4300 | 687.81 |
| 50 | VSS | -3963.06 | -654.15 | 130 | NC | 2878.94 | -654.15 | 210 | COM4 | 6087.34 | -102.06 | 290 | SEG71 | 4275 | 687.81 |
| 51 | VCC | -3874.06 | -654.15 | 131 | VSS | 2948.94 | -654.15 | 211 | COM3 | 6087.34 | -67.06 | 291 | SEG72 | 4250 | 687.81 |
| 52 | VCC | -3804.06 | -654.15 | 132 | VSS | 3018.94 | -654.15 | 212 | COM2 | 6087.34 | -32.06 | 292 | SEG73 | 4225 | 687.81 |
| 53 | VCOMH | -3697.06 | -654.15 | 133 | VLSS | 3088.94 | -654.15 | 213 | COM1 | 6087.34 | 2.94 | 293 | SEG74 | 4200 | 687.81 |
| 54 | VCOMH | -3627.06 | -654.15 | 134 | VLSS | 3158.94 | -654.15 | 214 | COM0 | 6087.34 | 37.94 | 294 | SEG75 | 4175 | 687.81 |
| 55 | VLSS | -3557.06 | -654.15 | 135 | VCOMH | 3228.94 | -654.15 | 215 | VLSS | 6087.34 | 72.94 | 295 | SEG76 | 4150 | 687.81 |
| 56 | VLSS | -3487.06 | -654.15 | 136 | VCOMH | 3298.94 | -654.15 | 216 | VLSS | 6087.34 | 107.94 | 296 | SEG77 | 4125 | 687.81 |
| 57 | VSS | -3417.06 | -654.15 | 137 | VCC | 3405.94 | -654.15 | 217 | VSL | 6097.34 | 311.09 | 297 | SEG78 | 4100 | 687.81 |
| 58 | VSS | -3347.06 | -654.15 | 138 | VCC | 3475.94 | -654.15 | 218 | VCC | 6097.34 | 687.81 | 298 | SEG79 | 4075 | 687.81 |
| 59 | VSL | -3277.06 | -654.15 | 139 | VSS | 3572.94 | -654.15 | 219 | SEGO | 6050 | 687.81 | 299 | SEG80 | 4050 | 687.81 |
| 60 | VSL | -3207.06 | -654.15 | 140 | VSS | 3642.94 | -654.15 | 220 | SEG1 | 6025 | 687.81 | 300 | SEG81 | 4025 | 687.81 |
| 61 | VCI | -3137.06 | -654.15 | 141 | VSS | 3712.94 | -654.15 | 221 | SEG2 | 6000 | 687.81 | 301 | SEG82 | 4000 | 687.81 |
| 62 | VCI | -3067.06 | -654.15 | 142 | VSS | 3782.94 | -654.15 | 222 | SEG3 | 5975 | 687.81 | 302 | SEG83 | 3975 | 687.81 |
| 63 | VDD1 | -2914.06 | -654.15 | 143 | VSS | 3852.94 | -654.15 | 223 | SEG4 | 5950 | 687.81 | 303 | SEG84 | 3950 | 687.81 |
| 64 | VDD1 | -2844.06 | -654.15 | 144 | VSS | 3922.94 | -654.15 | 224 | SEG5 | 5925 | 687.81 | 304 | SEG85 | 3925 | 687.81 |
| 65 | VDD | -2746.06 | -654.15 | 145 | VSS | 3992.94 | -654.15 | 225 | SEG6 | 5900 | 687.81 | 305 | SEG86 | 3900 | 687.81 |
| 66 | VDD | -2676.06 | -654.15 | 146 | VLSS | 4183.06 | -664.06 | 226 | SEG7 | 5875 | 687.81 | 306 | SEG87 | 3875 | 687.81 |
| 67 | VDD | -2606.06 | -654.15 | 147 | VLSS | 4218.06 | -664.06 | 227 | SEG8 | 5850 | 687.81 | 307 | SEG88 | 3850 | 687.81 |
| 68 | VDDIO | -2453.06 | -654.15 | 148 | COM63 | 4253.06 | -664.06 | 228 | SEG9 | 5825 | 687.81 | 308 | SEG89 | 3825 | 687.81 |
| 69 | VDDIO | -2383.06 | -654.15 | 149 | COM62 | 4288.06 | -664.06 | 229 | SEG10 | 5800 | 687.81 | 309 | SEG90 | 3800 | 687.81 |
| 70 | VDD | -2313.06 | -654.15 | 150 | COM61 | 4323.06 | -664.06 | 230 | SEG11 | 5775 | 687.81 | 310 | SEG91 | 3775 | 687.81 |
| 71 | VLSS | -2243.06 | -654.15 | 151 | COM60 | 4358.06 | -664.06 | 231 | SEG12 | 5750 | 687.81 | 311 | SEG92 | 3750 | 687.81 |
| 72 | GPIO0 | -2151.06 | -654.15 | 152 | COM59 | 4393.06 | -664.06 | 232 | SEG13 | 5725 | 687.81 | 312 | SEG93 | 3725 | 687.81 |
| 73 | GPIO1 | -2065.06 | -654.15 | 153 | COM58 | 4428.06 | -664.06 | 233 | SEG14 | 5700 | 687.81 | 313 | SEG94 | 3700 | 687.81 |
| 74 | IREF | -1973.06 | -654.15 | 154 | COM57 | 4463.06 | -664.06 | 234 | SEG15 | 5675 | 687.81 | 314 | SEG95 | 3675 | 687.81 |
| 75 | FR | -1881.06 | -654.15 | 155 | COM56 | 4498.06 | -664.06 | 235 | SEG16 | 5650 | 687.81 | 315 | SEG96 | 3650 | 687.81 |
| 76 | CL | -1795.06 | -654.15 | 156 | COM55 | 4533.06 | -664.06 | 236 | SEG17 | 5625 | 687.81 | 316 | SEG97 | 3625 | 687.81 |
| 77 | VSS | -1703.06 | -654.15 | 157 | COM54 | 4568.06 | -664.06 | 237 | SEG18 | 5600 | 687.81 | 317 | SEG98 | 3600 | 687.81 |
| 78 | DOF# | -1611.06 | -654.15 | 158 | COM53 | 4603.06 | -664.06 | 238 | SEG19 | 5575 | 687.81 | 318 | SEG99 | 3575 | 687.81 |
| 79 | NC | -1521.06 | -654.15 | 159 | COM52 | 4638.06 | -664.06 | 239 | SEG20 | 5550 | 687.81 | 319 | SEG100 | 3550 | 687.81 |
| 80 | VSS | -145 | | | | | | | | | | | | | |

| Pad no. | Pin name | X-pos | Y-pos |
|---------|----------|-------|--------|
| 321 | SEG102 | 3500 | 687.81 |
| 322 | SEG103 | 3475 | 687.81 |
| 323 | SEG104 | 3450 | 687.81 |
| 324 | SEG105 | 3425 | 687.81 |
| 325 | SEG106 | 3400 | 687.81 |
| 326 | SEG107 | 3375 | 687.81 |
| 327 | SEG108 | 3350 | 687.81 |
| 328 | SEG109 | 3325 | 687.81 |
| 329 | SEG110 | 3300 | 687.81 |
| 330 | SEG111 | 3275 | 687.81 |
| 331 | SEG112 | 3250 | 687.81 |
| 332 | SEG113 | 3225 | 687.81 |
| 333 | SEG114 | 3200 | 687.81 |
| 334 | SEG115 | 3175 | 687.81 |
| 335 | SEG116 | 3150 | 687.81 |
| 336 | SEG117 | 3125 | 687.81 |
| 337 | SEG118 | 3100 | 687.81 |
| 338 | SEG119 | 3075 | 687.81 |
| 339 | SEG120 | 3050 | 687.81 |
| 340 | SEG121 | 3025 | 687.81 |
| 341 | SEG122 | 3000 | 687.81 |
| 342 | SEG123 | 2975 | 687.81 |
| 343 | SEG124 | 2950 | 687.81 |
| 344 | SEG125 | 2925 | 687.81 |
| 345 | SEG126 | 2900 | 687.81 |
| 346 | SEG127 | 2875 | 687.81 |
| 347 | SEG128 | 2850 | 687.81 |
| 348 | SEG129 | 2825 | 687.81 |
| 349 | SEG130 | 2800 | 687.81 |
| 350 | SEG131 | 2775 | 687.81 |
| 351 | SEG132 | 2750 | 687.81 |
| 352 | SEG133 | 2725 | 687.81 |
| 353 | SEG134 | 2700 | 687.81 |
| 354 | SEG135 | 2675 | 687.81 |
| 355 | SEG136 | 2650 | 687.81 |
| 356 | SEG137 | 2625 | 687.81 |
| 357 | SEG138 | 2600 | 687.81 |
| 358 | SEG139 | 2575 | 687.81 |
| 359 | SEG140 | 2550 | 687.81 |
| 360 | SEG141 | 2525 | 687.81 |
| 361 | SEG142 | 2500 | 687.81 |
| 362 | SEG143 | 2475 | 687.81 |
| 363 | SEG144 | 2450 | 687.81 |
| 364 | SEG145 | 2425 | 687.81 |
| 365 | SEG146 | 2400 | 687.81 |
| 366 | SEG147 | 2375 | 687.81 |
| 367 | SEG148 | 2350 | 687.81 |
| 368 | SEG149 | 2325 | 687.81 |
| 369 | SEG150 | 2300 | 687.81 |
| 370 | SEG151 | 2275 | 687.81 |
| 371 | SEG152 | 2250 | 687.81 |
| 372 | SEG153 | 2225 | 687.81 |
| 373 | SEG154 | 2200 | 687.81 |
| 374 | SEG155 | 2175 | 687.81 |
| 375 | SEG156 | 2150 | 687.81 |
| 376 | SEG157 | 2125 | 687.81 |
| 377 | SEG158 | 2100 | 687.81 |
| 378 | SEG159 | 2075 | 687.81 |
| 379 | SEG160 | 2050 | 687.81 |
| 380 | SEG161 | 2025 | 687.81 |
| 381 | SEG162 | 2000 | 687.81 |
| 382 | SEG163 | 1975 | 687.81 |
| 383 | SEG164 | 1950 | 687.81 |
| 384 | SEG165 | 1925 | 687.81 |
| 385 | SEG166 | 1900 | 687.81 |
| 386 | SEG167 | 1875 | 687.81 |
| 387 | SEG168 | 1850 | 687.81 |
| 388 | SEG169 | 1825 | 687.81 |
| 389 | SEG170 | 1800 | 687.81 |
| 390 | SEG171 | 1775 | 687.81 |
| 391 | SEG172 | 1750 | 687.81 |
| 392 | SEG173 | 1725 | 687.81 |
| 393 | SEG174 | 1700 | 687.81 |
| 394 | SEG175 | 1675 | 687.81 |
| 395 | SEG176 | 1650 | 687.81 |
| 396 | SEG177 | 1625 | 687.81 |
| 397 | SEG178 | 1600 | 687.81 |
| 398 | SEG179 | 1575 | 687.81 |
| 399 | SEG180 | 1550 | 687.81 |
| 400 | SEG181 | 1525 | 687.81 |

| Pad no. | Pin name | X-pos | Y-pos |
|---------|----------|-------|--------|
| 401 | SEG182 | 1500 | 687.81 |
| 402 | SEG183 | 1475 | 687.81 |
| 403 | SEG184 | 1450 | 687.81 |
| 404 | SEG185 | 1425 | 687.81 |
| 405 | SEG186 | 1400 | 687.81 |
| 406 | SEG187 | 1375 | 687.81 |
| 407 | SEG188 | 1350 | 687.81 |
| 408 | SEG189 | 1325 | 687.81 |
| 409 | SEG190 | 1300 | 687.81 |
| 410 | SEG191 | 1275 | 687.81 |
| 411 | SEG192 | 1250 | 687.81 |
| 412 | SEG193 | 1225 | 687.81 |
| 413 | SEG194 | 1200 | 687.81 |
| 414 | SEG195 | 1175 | 687.81 |
| 415 | SEG196 | 1150 | 687.81 |
| 416 | SEG197 | 1125 | 687.81 |
| 417 | SEG198 | 1100 | 687.81 |
| 418 | SEG199 | 1075 | 687.81 |
| 419 | SEG200 | 1050 | 687.81 |
| 420 | SEG201 | 1025 | 687.81 |
| 421 | SEG202 | 1000 | 687.81 |
| 422 | SEG203 | 975 | 687.81 |
| 423 | SEG204 | 950 | 687.81 |
| 424 | SEG205 | 925 | 687.81 |
| 425 | SEG206 | 900 | 687.81 |
| 426 | SEG207 | 875 | 687.81 |
| 427 | SEG208 | 850 | 687.81 |
| 428 | SEG209 | 825 | 687.81 |
| 429 | SEG210 | 800 | 687.81 |
| 430 | SEG211 | 775 | 687.81 |
| 431 | SEG212 | 750 | 687.81 |
| 432 | SEG213 | 725 | 687.81 |
| 433 | SEG214 | 700 | 687.81 |
| 434 | SEG215 | 675 | 687.81 |
| 435 | SEG216 | 650 | 687.81 |
| 436 | SEG217 | 625 | 687.81 |
| 437 | SEG218 | 600 | 687.81 |
| 438 | SEG219 | 575 | 687.81 |
| 439 | SEG220 | 550 | 687.81 |
| 440 | SEG221 | 525 | 687.81 |
| 441 | SEG222 | 500 | 687.81 |
| 442 | SEG223 | 475 | 687.81 |
| 443 | SEG224 | 450 | 687.81 |
| 444 | SEG225 | 425 | 687.81 |
| 445 | SEG226 | 400 | 687.81 |
| 446 | SEG227 | 375 | 687.81 |
| 447 | SEG228 | 350 | 687.81 |
| 448 | SEG229 | 325 | 687.81 |
| 449 | SEG230 | 300 | 687.81 |
| 450 | SEG231 | 275 | 687.81 |
| 451 | SEG232 | 250 | 687.81 |
| 452 | SEG233 | 225 | 687.81 |
| 453 | SEG234 | 200 | 687.81 |
| 454 | SEG235 | 175 | 687.81 |
| 455 | SEG236 | 150 | 687.81 |
| 456 | SEG237 | 125 | 687.81 |
| 457 | SEG238 | 100 | 687.81 |
| 458 | SEG239 | 75 | 687.81 |
| 459 | VCC | 50 | 687.81 |
| 460 | VCC | 25 | 687.81 |
| 461 | VCC | 0 | 687.81 |
| 462 | VCC | -25 | 687.81 |
| 463 | VCC | -50 | 687.81 |
| 464 | SEG240 | -75 | 687.81 |
| 465 | SEG241 | -100 | 687.81 |
| 466 | SEG242 | -125 | 687.81 |
| 467 | SEG243 | -150 | 687.81 |
| 468 | SEG244 | -175 | 687.81 |
| 469 | SEG245 | -200 | 687.81 |
| 470 | SEG246 | -225 | 687.81 |
| 471 | SEG247 | -250 | 687.81 |
| 472 | SEG248 | -275 | 687.81 |
| 473 | SEG249 | -300 | 687.81 |
| 474 | SEG250 | -325 | 687.81 |
| 475 | SEG251 | -350 | 687.81 |
| 476 | SEG252 | -375 | 687.81 |
| 477 | SEG253 | -400 | 687.81 |
| 478 | SEG254 | -425 | 687.81 |
| 479 | SEG255 | -450 | 687.81 |
| 480 | SEG256 | -475 | 687.81 |

| Pad no. | Pin name | X-pos | Y-pos |
|---------|----------|-------|--------|
| 481 | SEG257 | -500 | 687.81 |
| 482 | SEG258 | -525 | 687.81 |
| 483 | SEG259 | -550 | 687.81 |
| 484 | SEG260 | -575 | 687.81 |
| 485 | SEG261 | -600 | 687.81 |
| 486 | SEG262 | -625 | 687.81 |
| 487 | SEG263 | -650 | 687.81 |
| 488 | SEG264 | -675 | 687.81 |
| 489 | SEG265 | -700 | 687.81 |
| 490 | SEG266 | -725 | 687.81 |
| 491 | SEG267 | -750 | 687.81 |
| 492 | SEG268 | -775 | 687.81 |
| 493 | SEG269 | -800 | 687.81 |
| 494 | SEG270 | -825 | 687.81 |
| 495 | SEG271 | -850 | 687.81 |
| 496 | SEG272 | -875 | 687.81 |
| 497 | SEG273 | -900 | 687.81 |
| 498 | SEG274 | -925 | 687.81 |
| 499 | SEG275 | -950 | 687.81 |
| 500 | SEG276 | -975 | 687.81 |
| 501 | SEG277 | -1000 | 687.81 |
| 502 | SEG278 | -1025 | 687.81 |
| 503 | SEG279 | -1050 | 687.81 |
| 504 | SEG280 | -1075 | 687.81 |
| 505 | SEG281 | -1100 | 687.81 |
| 506 | SEG282 | -1125 | 687.81 |
| 507 | SEG283 | -1150 | 687.81 |
| 508 | SEG284 | -1175 | 687.81 |
| 509 | SEG285 | -1200 | 687.81 |
| 510 | SEG286 | -1225 | 687.81 |
| 511 | SEG287 | -1250 | 687.81 |
| 512 | SEG288 | -1275 | 687.81 |
| 513 | SEG289 | -1300 | 687.81 |
| 514 | SEG290 | -1325 | 687.81 |
| 515 | SEG291 | -1350 | 687.81 |
| 516 | SEG292 | -1375 | 687.81 |
| 517 | SEG293 | -1400 | 687.81 |
| 518 | SEG294 | -1425 | 687.81 |
| 519 | SEG295 | -1450 | 687.81 |
| 520 | SEG296 | -1475 | 687.81 |
| 521 | SEG297 | -1500 | 687.81 |
| 522 | SEG298 | -1525 | 687.81 |
| 523 | SEG299 | -1550 | 687.81 |
| 524 | SEG300 | -1575 | 687.81 |
| 525 | SEG301 | -1600 | 687.81 |
| 526 | SEG302 | -1625 | 687.81 |
| 527 | SEG303 | -1650 | 687.81 |
| 528 | SEG304 | -1675 | 687.81 |
| 529 | SEG305 | -1700 | 687.81 |
| 530 | SEG306 | -1725 | 687.81 |
| 531 | SEG307 | -1750 | 687.81 |
| 532 | SEG308 | -1775 | 687.81 |
| 533 | SEG309 | -1800 | 687.81 |
| 534 | SEG310 | -1825 | 687.81 |
| 535 | SEG311 | -1850 | 687.81 |
| 536 | SEG312 | -1875 | 687.81 |
| 537 | SEG313 | -1900 | 687.81 |
| 538 | SEG314 | -1925 | 687.81 |
| 539 | SEG315 | -1950 | 687.81 |
| 540 | SEG316 | -1975 | 687.81 |
| 541 | SEG317 | -2000 | 687.81 |
| 542 | SEG318 | -2025 | 687.81 |
| 543 | SEG319 | -2050 | 687.81 |
| 544 | SEG320 | -2075 | 687.81 |
| 545 | SEG321 | -2100 | 687.81 |
| 546 | SEG322 | -2125 | 687.81 |
| 547 | SEG323 | -2150 | 687.81 |
| 548 | SEG324 | -2175 | 687.81 |
| 549 | SEG325 | -2200 | 687.81 |
| 550 | SEG326 | -2225 | 687.81 |
| 551 | SEG327 | -2250 | 687.81 |
| 552 | SEG328 | -2275 | 687.81 |
| 553 | SEG329 | -2300 | 687.81 |
| 554 | SEG330 | -2325 | 687.81 |
| 555 | SEG331 | -2350 | 687.81 |
| 556 | SEG332 | -2375 | 687.81 |
| 557 | SEG333 | -2400 | 687.81 |
| 558 | SEG334 | -2425 | 687.81 |
| 559 | SEG335 | -2450 | 687.81 |
| 560 | SEG336 | -2475 | 687.81 |

| Pad no. | Pin name | X-pos | Y-pos |
|---------|----------|-------|--------|
| 561 | SEG337 | -2500 | 687.81 |
| 562 | SEG338 | -2525 | 687.81 |
| 563 | SEG339 | -2550 | 687.81 |
| 564 | SEG340 | -2575 | 687.81 |
| 565 | SEG341 | -2600 | 687.81 |
| 566 | SEG342 | -2625 | 687.81 |
| 567 | SEG343 | -2650 | 687.81 |
| 568 | SEG344 | -2675 | 687.81 |
| 569 | SEG345 | -2700 | 687.81 |
| 570 | SEG346 | -2725 | 687.81 |
| 571 | SEG347 | -2750 | 687.81 |
| 572 | SEG348 | -2775 | 687.81 |
| 573 | SEG349 | -2800 | 687.81 |
| 574 | SEG350 | -2825 | 687.81 |
| 575 | SEG351 | -2850 | 687.81 |
| 576 | SEG352 | -2875 | 687.81 |
| 577 | SEG353 | -2900 | 687.81 |
| 578 | SEG354 | -2925 | 687.81 |
| 579 | SEG355 | -2950 | 687.81 |
| 580 | SEG356 | -2975 | 687.81 |
| 581 | SEG357 | -3000 | 687.81 |
| 582 | SEG358 | -3025 | 687.81 |
| 583 | SEG359 | -3050 | 687.81 |
| 584 | SEG360 | -3075 | 687.81 |
| 585 | SEG361 | -3100 | 687.81 |
| 586 | SEG362 | -3125 | 687.81 |
| 587 | SEG363 | -3150 | 687.81 |
| 588 | SEG364 | -3175 | 687.81 |
| 589 | SEG365 | -3200 | 687.81 |
| 590 | SEG366 | -3225 | 687.81 |
| 591 | SEG367 | -3250 | 687.81 |
| 592 | SEG368 | -3275 | 687.81 |
| 593 | SEG369 | -3300 | 687.81 |
| 594 | SEG370 | -3325 | 687.81 |
| 595 | SEG371 | -3350 | 687.81 |
| 596 | SEG372 | -3375 | 687.81 |
| 597 | SEG373 | -3400 | 687.81 |
| 598 | SEG374 | -3425 | 687.81 |
| 599 | SEG375 | -3450 | 687.81 |
| 600 | SEG376 | -3475 | 687.81 |
| 601 | SEG377 | -3500 | 687.81 |
| 602 | SEG378 | -3525 | 687.81 |
| 603 | SEG379 | -3550 | 687.81 |
| 604 | SEG380 | -3575 | 687.81 |
| 605 | SEG381 | -3600 | 687.81 |
| 606 | SEG382 | -3625 | 687.81 |
| 607 | SEG383 | -3650 | 687.81 |
| 608 | SEG384 | -3675 | 687.81 |
| 609 | SEG385 | -3700 | 6 |

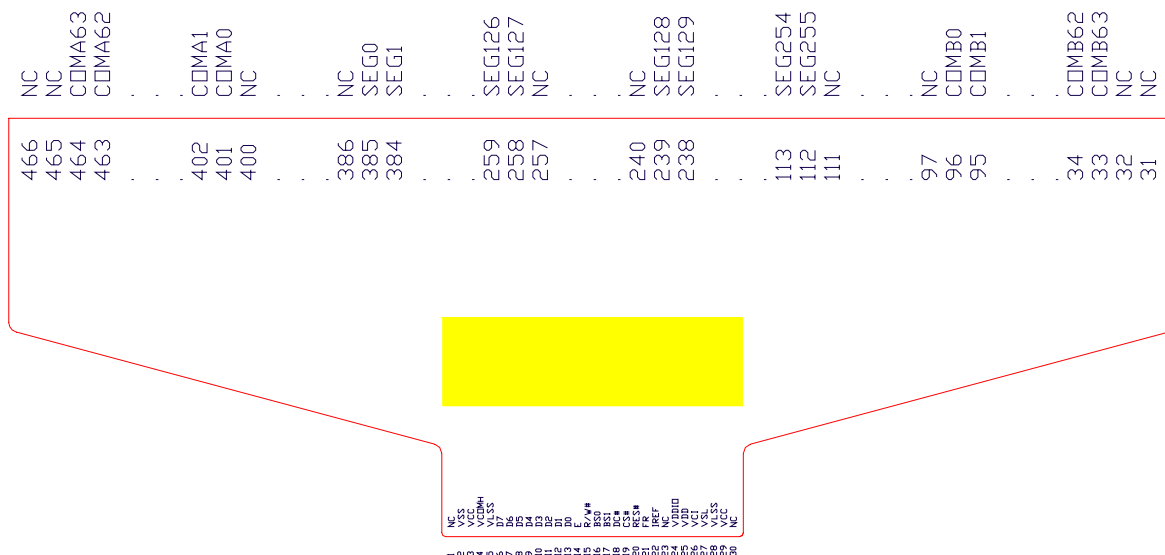
| Pad no. | Pin name | X-pos | Y-pos |
|---------|----------|----------|---------|
| 641 | SEG417 | -4500 | 687.81 |
| 642 | SEG418 | -4525 | 687.81 |
| 643 | SEG419 | -4550 | 687.81 |
| 644 | SEG420 | -4575 | 687.81 |
| 645 | SEG421 | -4600 | 687.81 |
| 646 | SEG422 | -4625 | 687.81 |
| 647 | SEG423 | -4650 | 687.81 |
| 648 | SEG424 | -4675 | 687.81 |
| 649 | SEG425 | -4700 | 687.81 |
| 650 | SEG426 | -4725 | 687.81 |
| 651 | SEG427 | -4750 | 687.81 |
| 652 | SEG428 | -4775 | 687.81 |
| 653 | SEG429 | -4800 | 687.81 |
| 654 | SEG430 | -4825 | 687.81 |
| 655 | SEG431 | -4850 | 687.81 |
| 656 | SEG432 | -4875 | 687.81 |
| 657 | SEG433 | -4900 | 687.81 |
| 658 | SEG434 | -4925 | 687.81 |
| 659 | SEG435 | -4950 | 687.81 |
| 660 | SEG436 | -4975 | 687.81 |
| 661 | SEG437 | -5000 | 687.81 |
| 662 | SEG438 | -5025 | 687.81 |
| 663 | SEG439 | -5050 | 687.81 |
| 664 | SEG440 | -5075 | 687.81 |
| 665 | SEG441 | -5100 | 687.81 |
| 666 | SEG442 | -5125 | 687.81 |
| 667 | SEG443 | -5150 | 687.81 |
| 668 | SEG444 | -5175 | 687.81 |
| 669 | SEG445 | -5200 | 687.81 |
| 670 | SEG446 | -5225 | 687.81 |
| 671 | SEG447 | -5250 | 687.81 |
| 672 | SEG448 | -5275 | 687.81 |
| 673 | SEG449 | -5300 | 687.81 |
| 674 | SEG450 | -5325 | 687.81 |
| 675 | SEG451 | -5350 | 687.81 |
| 676 | SEG452 | -5375 | 687.81 |
| 677 | SEG453 | -5400 | 687.81 |
| 678 | SEG454 | -5425 | 687.81 |
| 679 | SEG455 | -5450 | 687.81 |
| 680 | SEG456 | -5475 | 687.81 |
| 681 | SEG457 | -5500 | 687.81 |
| 682 | SEG458 | -5525 | 687.81 |
| 683 | SEG459 | -5550 | 687.81 |
| 684 | SEG460 | -5575 | 687.81 |
| 685 | SEG461 | -5600 | 687.81 |
| 686 | SEG462 | -5625 | 687.81 |
| 687 | SEG463 | -5650 | 687.81 |
| 688 | SEG464 | -5675 | 687.81 |
| 689 | SEG465 | -5700 | 687.81 |
| 690 | SEG466 | -5725 | 687.81 |
| 691 | SEG467 | -5750 | 687.81 |
| 692 | SEG468 | -5775 | 687.81 |
| 693 | SEG469 | -5800 | 687.81 |
| 694 | SEG470 | -5825 | 687.81 |
| 695 | SEG471 | -5850 | 687.81 |
| 696 | SEG472 | -5875 | 687.81 |
| 697 | SEG473 | -5900 | 687.81 |
| 698 | SEG474 | -5925 | 687.81 |
| 699 | SEG475 | -5950 | 687.81 |
| 700 | SEG476 | -5975 | 687.81 |
| 701 | SEG477 | -6000 | 687.81 |
| 702 | SEG478 | -6025 | 687.81 |
| 703 | SEG479 | -6050 | 687.81 |
| 704 | VCC | -6097.34 | 687.81 |
| 705 | VSL | -6097.34 | 311.09 |
| 706 | VLSS | -6087.34 | 107.94 |
| 707 | VLSS | -6087.34 | 72.94 |
| 708 | COM64 | -6087.34 | 37.94 |
| 709 | COM65 | -6087.34 | 2.94 |
| 710 | COM66 | -6087.34 | -32.06 |
| 711 | COM67 | -6087.34 | -67.06 |
| 712 | COM68 | -6087.34 | -102.06 |
| 713 | COM69 | -6087.34 | -137.06 |
| 714 | COM70 | -6087.34 | -172.06 |
| 715 | COM71 | -6087.34 | -207.06 |
| 716 | COM72 | -6087.34 | -242.06 |
| 717 | COM73 | -6087.34 | -277.06 |
| 718 | COM74 | -6087.34 | -312.06 |
| 719 | COM75 | -6087.34 | -347.06 |
| 720 | COM76 | -6087.34 | -382.06 |

| Pad no. | Pin name | X-pos | Y-pos |
|---------|----------|----------|---------|
| 721 | COM77 | -6087.34 | -417.06 |
| 722 | COM78 | -6087.34 | -452.06 |
| 723 | COM79 | -6087.34 | -487.06 |
| 724 | COM80 | -6087.34 | -522.06 |
| 725 | COM81 | -6087.34 | -557.06 |
| 726 | COM82 | -6087.34 | -592.06 |
| 727 | COM83 | -6087.34 | -627.06 |
| 728 | VLSS | -6087.34 | -674.56 |

6 PIN ARRANGEMENT

6.1 SSD1322UR1 pin assignment

Figure 6-1: SSD1322UR1 Pin Assignment



Note:

(1) COM sequence is listed in terms of dual COM mode; refer to Table 9-1 for details.

Table 6-1: SSD132UR1 Pin Assignment Table

| Pad no. | Pin name | Pad no. | Pin name | Pad no. | Pin name | Pad no. | Pin name | Pad no. | Pin name | Pad no. | Pin name |
|---------|----------|---------|----------|---------|----------|---------|----------|---------|----------|---------|----------|
| 1 | NC | 81 | COMB15 | 161 | SEG206 | 241 | NC | 321 | SEG64 | 401 | COMA0 |
| 2 | VSS | 82 | COMB14 | 162 | SEG205 | 242 | NC | 322 | SEG63 | 402 | COMA1 |
| 3 | VCC | 83 | COMB13 | 163 | SEG204 | 243 | NC | 323 | SEG62 | 403 | COMA2 |
| 4 | VCOMH | 84 | COMB12 | 164 | SEG203 | 244 | NC | 324 | SEG61 | 404 | COMA3 |
| 5 | VLSS | 85 | COMB11 | 165 | SEG202 | 245 | NC | 325 | SEG60 | 405 | COMA4 |
| 6 | D7 | 86 | COMB10 | 166 | SEG201 | 246 | NC | 326 | SEG59 | 406 | COMA5 |
| 7 | D6 | 87 | COMB9 | 167 | SEG200 | 247 | NC | 327 | SEG58 | 407 | COMA6 |
| 8 | D5 | 88 | COMB8 | 168 | SEG199 | 248 | NC | 328 | SEG57 | 408 | COMA7 |
| 9 | D4 | 89 | COMB7 | 169 | SEG198 | 249 | NC | 329 | SEG56 | 409 | COMA8 |
| 10 | D3 | 90 | COMB6 | 170 | SEG197 | 250 | NC | 330 | SEG55 | 410 | COMA9 |
| 11 | D2 | 91 | COMB5 | 171 | SEG196 | 251 | NC | 331 | SEG54 | 411 | COMA10 |
| 12 | D1 | 92 | COMB4 | 172 | SEG195 | 252 | NC | 332 | SEG53 | 412 | COMA11 |
| 13 | D0 | 93 | COMB3 | 173 | SEG194 | 253 | NC | 333 | SEG52 | 413 | COMA12 |
| 14 | E/RD# | 94 | COMB2 | 174 | SEG193 | 254 | NC | 334 | SEG51 | 414 | COMA13 |
| 15 | RW# | 95 | COMB1 | 175 | SEG192 | 255 | NC | 335 | SEG50 | 415 | COMA14 |
| 16 | BS0 | 96 | COMB0 | 176 | SEG191 | 256 | NC | 336 | SEG49 | 416 | COMA15 |
| 17 | BS1 | 97 | NC | 177 | SEG190 | 257 | NC | 337 | SEG48 | 417 | COMA16 |
| 18 | DC# | 98 | NC | 178 | SEG189 | 258 | SEG127 | 338 | SEG47 | 418 | COMA17 |
| 19 | CS# | 99 | NC | 179 | SEG188 | 259 | SEG126 | 339 | SEG46 | 419 | COMA18 |
| 20 | RES# | 100 | NC | 180 | SEG187 | 260 | SEG125 | 340 | SEG45 | 420 | COMA19 |
| 21 | FR | 101 | NC | 181 | SEG186 | 261 | SEG124 | 341 | SEG44 | 421 | COMA20 |
| 22 | IREF | 102 | NC | 182 | SEG185 | 262 | SEG123 | 342 | SEG43 | 422 | COMA21 |
| 23 | NC | 103 | NC | 183 | SEG184 | 263 | SEG122 | 343 | SEG42 | 423 | COMA22 |
| 24 | VDDIO | 104 | NC | 184 | SEG183 | 264 | SEG121 | 344 | SEG41 | 424 | COMA23 |
| 25 | VDD | 105 | NC | 185 | SEG182 | 265 | SEG120 | 345 | SEG40 | 425 | COMA24 |
| 26 | VCI | 106 | NC | 186 | SEG181 | 266 | SEG119 | 346 | SEG39 | 426 | COMA25 |
| 27 | VSL | 107 | NC | 187 | SEG180 | 267 | SEG118 | 347 | SEG38 | 427 | COMA26 |
| 28 | VLSS | 108 | NC | 188 | SEG179 | 268 | SEG117 | 348 | SEG37 | 428 | COMA27 |
| 29 | VCC | 109 | NC | 189 | SEG178 | 269 | SEG116 | 349 | SEG36 | 429 | COMA28 |
| 30 | NC | 110 | NC | 190 | SEG177 | 270 | SEG115 | 350 | SEG35 | 430 | COMA29 |
| 31 | NC | 111 | NC | 191 | SEG176 | 271 | SEG114 | 351 | SEG34 | 431 | COMA30 |
| 32 | NC | 112 | SEG255 | 192 | SEG175 | 272 | SEG113 | 352 | SEG33 | 432 | COMA31 |
| 33 | COMB63 | 113 | SEG254 | 193 | SEG174 | 273 | SEG112 | 353 | SEG32 | 433 | COMA32 |
| 34 | COMB62 | 114 | SEG253 | 194 | SEG173 | 274 | SEG111 | 354 | SEG31 | 434 | COMA33 |
| 35 | COMB61 | 115 | SEG252 | 195 | SEG172 | 275 | SEG110 | 355 | SEG30 | 435 | COMA34 |
| 36 | COMB60 | 116 | SEG251 | 196 | SEG171 | 276 | SEG109 | 356 | SEG29 | 436 | COMA35 |
| 37 | COMB59 | 117 | SEG250 | 197 | SEG170 | 277 | SEG108 | 357 | SEG28 | 437 | COMA36 |
| 38 | COMB58 | 118 | SEG249 | 198 | SEG169 | 278 | SEG107 | 358 | SEG27 | 438 | COMA37 |
| 39 | COMB57 | 119 | SEG248 | 199 | SEG168 | 279 | SEG106 | 359 | SEG26 | 439 | COMA38 |
| 40 | COMB56 | 120 | SEG247 | 200 | SEG167 | 280 | SEG105 | 360 | SEG25 | 440 | COMA39 |
| 41 | COMB55 | 121 | SEG246 | 201 | SEG166 | 281 | SEG104 | 361 | SEG24 | 441 | COMA40 |
| 42 | COMB54 | 122 | SEG245 | 202 | SEG165 | 282 | SEG103 | 362 | SEG23 | 442 | COMA41 |
| 43 | COMB53 | 123 | SEG244 | 203 | SEG164 | 283 | SEG102 | 363 | SEG22 | 443 | COMA42 |
| 44 | COMB52 | 124 | SEG243 | 204 | SEG163 | 284 | SEG101 | 364 | SEG21 | 444 | COMA43 |
| 45 | COMB51 | 125 | SEG242 | 205 | SEG162 | 285 | SEG100 | 365 | SEG20 | 445 | COMA44 |
| 46 | COMB50 | 126 | SEG241 | 206 | SEG161 | 286 | SEG99 | 366 | SEG19 | 446 | COMA45 |
| 47 | COMB49 | 127 | SEG240 | 207 | SEG160 | 287 | SEG98 | 367 | SEG18 | 447 | COMA46 |
| 48 | COMB48 | 128 | SEG239 | 208 | SEG159 | 288 | SEG97 | 368 | SEG17 | 448 | COMA47 |
| 49 | COMB47 | 129 | SEG238 | 209 | SEG158 | 289 | SEG96 | 369 | SEG16 | 449 | COMA48 |
| 50 | COMB46 | 130 | SEG237 | 210 | SEG157 | 290 | SEG95 | 370 | SEG15 | 450 | COMA49 |
| 51 | COMB45 | 131 | SEG236 | 211 | SEG156 | 291 | SEG94 | 371 | SEG14 | 451 | COMA50 |
| 52 | COMB44 | 132 | SEG235 | 212 | SEG155 | 292 | SEG93 | 372 | SEG13 | 452 | COMA51 |
| 53 | COMB43 | 133 | SEG234 | 213 | SEG154 | 293 | SEG92 | 373 | SEG12 | 453 | COMA52 |
| 54 | COMB42 | 134 | SEG233 | 214 | SEG153 | 294 | SEG91 | 374 | SEG11 | 454 | COMA53 |
| 55 | COMB41 | 135 | SEG232 | 215 | SEG152 | 295 | SEG90 | 375 | SEG10 | 455 | COMA54 |
| 56 | COMB40 | 136 | SEG231 | 216 | SEG151 | 296 | SEG89 | 376 | SEG9 | 456 | COMA55 |
| 57 | COMB39 | 137 | SEG230 | 217 | SEG150 | 297 | SEG88 | 377 | SEG8 | 457 | COMA56 |
| 58 | COMB38 | 138 | SEG229 | 218 | SEG149 | 298 | SEG87 | 378 | SEG7 | 458 | COMA57 |
| 59 | COMB37 | 139 | SEG228 | 219 | SEG148 | 299 | SEG86 | 379 | SEG6 | 459 | COMA58 |
| 60 | COMB36 | 140 | SEG227 | 220 | SEG147 | 300 | SEG85 | 380 | SEG5 | 460 | COMA59 |
| 61 | COMB35 | 141 | SEG226 | 221 | SEG146 | 301 | SEG84 | 381 | SEG4 | 461 | COMA60 |
| 62 | COMB34 | 142 | SEG225 | 222 | SEG145 | 302 | SEG83 | 382 | SEG3 | 462 | COMA61 |
| 63 | COMB33 | 143 | SEG224 | 223 | SEG144 | 303 | SEG82 | 383 | SEG2 | 463 | COMA62 |
| 64 | COMB32 | 144 | SEG223 | 224 | SEG143 | 304 | SEG81 | 384 | SEG1 | 464 | COMA63 |
| 65 | COMB31 | 145 | SEG222 | 225 | SEG142 | 305 | SEG80 | 385 | SEG0 | 465 | NC |
| 66 | COMB30 | 146 | SEG221 | 226 | SEG141 | 306 | SEG79 | 386 | NC | 466 | NC |
| 67 | COMB29 | 147 | SEG220 | 227 | SEG140 | 307 | SEG78 | 387 | NC | | |
| 68 | COMB28 | 148 | SEG219 | 228 | SEG139 | 308 | SEG77 | 388 | NC | | |
| 69 | COMB27 | 149 | SEG218 | 229 | SEG138 | 309 | SEG76 | 389 | NC | | |
| 70 | COMB26 | 150 | SEG217 | 230 | SEG137 | 310 | SEG75 | 390 | NC | | |
| 71 | COMB25 | 151 | SEG216 | 231 | SEG136 | 311 | SEG74 | 391 | NC | | |
| 72 | COMB24 | 152 | SEG215 | 232 | SEG135 | 312 | SEG73 | 392 | NC | | |
| 73 | COMB23 | 153 | SEG214 | 233 | SEG134 | 313 | SEG72 | 393 | NC | | |
| 74 | COMB22 | 154 | SEG213 | 234 | SEG133 | 314 | SEG71 | 394 | NC | | |
| 75 | COMB21 | 155 | SEG212 | 235 | SEG132 | 315 | SEG70 | 395 | NC | | |
| 76 | COMB20 | 156 | SEG211 | 236 | SEG131 | 316 | SEG69 | 396 | NC | | |
| 77 | COMB19 | 157 | SEG210 | 237 | SEG130 | 317 | SEG68 | 397 | NC | | |
| 78 | COMB18 | 158 | SEG209 | 238 | SEG129 | 318 | SEG67 | 398 | NC | | |
| 79 | COMB17 | 159 | SEG208 | 239 | SEG128 | 319 | SEG66 | 399 | NC | | |
| 80 | COMB16 | 160 | SEG207 | 240 | NC | 320 | SEG65 | 400 | NC | | |

7 PIN DESCRIPTIONS

Key:

| | |
|------------------------------------|----------------------------------|
| I = Input | NC = Not Connected |
| O = Output | Pull LOW= connect to Ground |
| IO = Bi-directional (input/output) | Pull HIGH= connect to V_{DDIO} |
| P = Power pin | |

Table 7-1: SSD1322 Pin Description

| Pin Name | Pin Type | Description | | | | | | | | | | |
|------------|-------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------|-------------------------|----|------------|----|------------|----|---------------------|----|---------------------|
| V_{DD} | P | Power supply pin for core logic operation. A capacitor is required to connect between this pin and V_{SS} . Refer to Section 8.10 for details. | | | | | | | | | | |
| V_{DDIO} | P | Power supply for interface logic level. It should be matched with the MCU interface voltage level. Refer to Section 8.10 for details. | | | | | | | | | | |
| V_{CI} | P | Low voltage power supply. V_{CI} must always be equal to or higher than V_{DD} and V_{DDIO} . Refer to Section 8.10 for details. | | | | | | | | | | |
| V_{CC} | P | Power supply for panel driving voltage. This is also the most positive power voltage supply pin. | | | | | | | | | | |
| V_{DD1} | P | Power supply and it should be connected to V_{DD} . | | | | | | | | | | |
| V_{SS} | P | Ground pin. | | | | | | | | | | |
| V_{LSS} | P | Analog system ground pin. | | | | | | | | | | |
| V_{COMH} | P | COM signal deselected voltage level. A capacitor should be connected between this pin and V_{SS} . | | | | | | | | | | |
| BGGND | P | It should be connected to ground. | | | | | | | | | | |
| GPIO0 | IO | This is a reserved pin. It should be kept NC. | | | | | | | | | | |
| GPIO1 | IO | This is a reserved pin. It should be kept NC. | | | | | | | | | | |
| V_{SL} | P | This is segment voltage reference pin. When external V_{SL} is used, connect with resistor and diode to ground (details depend on application). | | | | | | | | | | |
| BS[1:0] | I | MCU bus interface selection pins. Select appropriate logic setting as described in the following table. <div style="text-align: center;"> <p>Table 7-2 : Bus Interface selection</p> <table border="1"> <thead> <tr> <th>BS[1:0]</th> <th>Bus Interface Selection</th> </tr> </thead> <tbody> <tr> <td>00</td> <td>4 line SPI</td> </tr> <tr> <td>01</td> <td>3 line SPI</td> </tr> <tr> <td>10</td> <td>8-bit 8080 parallel</td> </tr> <tr> <td>11</td> <td>8-bit 6800 parallel</td> </tr> </tbody> </table> <p>Note (1) 0 is connected to V_{SS} (2) 1 is connected to V_{DDIO}</p> </div> | BS[1:0] | Bus Interface Selection | 00 | 4 line SPI | 01 | 3 line SPI | 10 | 8-bit 8080 parallel | 11 | 8-bit 6800 parallel |
| BS[1:0] | Bus Interface Selection | | | | | | | | | | | |
| 00 | 4 line SPI | | | | | | | | | | | |
| 01 | 3 line SPI | | | | | | | | | | | |
| 10 | 8-bit 8080 parallel | | | | | | | | | | | |
| 11 | 8-bit 6800 parallel | | | | | | | | | | | |

| Pin Name | Pin Type | Description |
|------------------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| I _{REF} | I | This pin is the segment output current reference pin. A resistor should be connected between this pin and V _{SS} to maintain the current around 10uA. Please refer to section 8.6 for the formula of resistor value from I _{REF} . |
| M/S# | I | This pin must be connected to V _{DDIO} to enable the chip. |
| CL | IO | External clock input pin. When internal clock is enable (i.e. pull HIGH in CLS pin), this pin is not used and should be connected to Ground. When internal clock is disable (i.e. pull LOW is CLS pin), this pin is the external clock source input pin. |
| CLS | I | Internal clock selection pin. When this pin is pulled HIGH, internal oscillator is enabled (normal operation). When this pin is pulled LOW, an external clock signal should be connected to CL. |
| CS# | I | This pin is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW. |
| RES# | I | This pin is reset signal input. When the pin is pulled LOW, initialization of the chip is executed. Keep this pin pull HIGH during normal operation. |
| D/C# | I | This pin is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the content at D[7:0] will be interpreted as data. When the pin is pulled LOW, the content at D[7:0] will be interpreted as command. |
| R/W# (WR#) | I | This pin is read / write control input pin connecting to the MCU interface. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial interface is selected, this pin R/W (WR#) must be connected to V _{SS} . |
| E (RD#) | I | This pin is MCU interface input. When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When connecting to an 8080-microprocessor, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial interface is selected, this pin E(RD#) must be connected to V _{SS} . |
| D[7:0] | IO | These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW. (Except for D2 pin in SPI mode) Refer to Section 8.1 for different bus interface connection. |
| DN[9:0] | IO | These are reserved pins and should be connected to V _{SS} . |

| Pin Name | Pin Type | Description |
|-----------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------|
| FR | O | This pin is No Connection pins. Nothing should be connected to this pin. This pin should be left open individually. |
| DOF# | O | This pin is No Connection pins. Nothing should be connected to this pin. This pin should be left open individually. |
| SEG[479:0] | O | These pins provide the OLED segment driving signals. These pins are V_{SS} state when display is OFF. |
| COM[127:0] | O | These pins provide the Common switch signals to the OLED panel. These pins are in high impedance state when display is OFF. |

8 FUNCTIONAL BLOCK DESCRIPTIONS

8.1 MCU Interface

SSD1322 MCU interface consist of 8 data pin and 5 control pins. The pin assignment at different interface mode is summarized in Table 8-1. Different MCU mode can be set by hardware selection on BS[1:0] pins (refer to Table 7-2 for BS[1:0] pins setting)

Table 8-1 : MCU interface assignment under different bus interface mode

| Pin Name Bus Interface | Data/Command Interface | | | | | | | Control Signal | | | | | |
|---------------------------|------------------------|----|----|----|----|------|------|----------------|------|---------|------|------|------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | E | R/W# | CS# | D/C# | RES# |
| 8-bit 8080 | D[7:0] | | | | | | | RD# | WR# | CS# | D/C# | RES# | |
| 8-bit 6800 | D[7:0] | | | | | | | E | R/W# | CS# | D/C# | RES# | |
| 3-wire SPI | Tie LOW | | | | NC | SDIN | SCLK | Tie LOW | CS# | Tie LOW | RES# | | |
| 4-wire SPI | Tie LOW | | | | NC | SDIN | SCLK | Tie LOW | CS# | D/C# | RES# | | |

8.1.1 MCU Parallel 6800-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), R/W#, D/C#, E and CS#.

A LOW in R/W# indicates WRITE operation and HIGH in R/W# indicates READ operation.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.

The E input serves as data latch signal while CS# is LOW. Data is latched at the falling edge of E signal.

Table 8-2 : Control pins of 6800 interface

| Function | E | R/W# | CS# | D/C# |
|---------------|---|------|-----|------|
| Write command | ↓ | L | L | L |
| Read status | ↓ | H | L | L |
| Write data | ↓ | L | L | H |
| Read data | ↓ | H | L | H |

Note

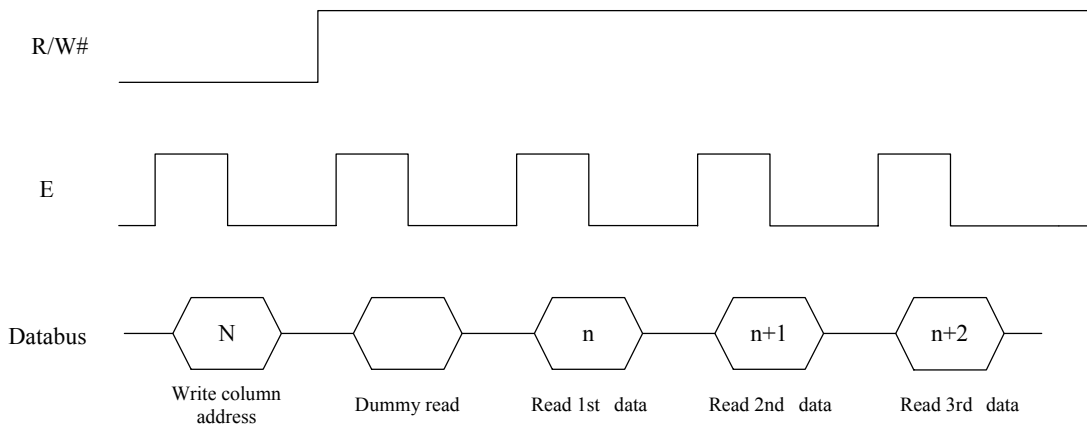
⁽¹⁾ ↓ stands for falling edge of signal

⁽²⁾ H stands for HIGH in signal

⁽³⁾ L stands for LOW in signal

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-1.

Figure 8-1 : Data read back procedure - insertion of dummy read



8.1.2 MCU Parallel 8080-series Interface

The parallel interface consists of 8 bi-directional data pins (D[7:0]), RD#, WR#, D/C# and CS#.

A LOW in D/C# indicates COMMAND read/write and HIGH in D/C# indicates DATA read/write.

A rising edge of RD# input serves as a data READ latch signal while CS# is kept LOW.

A rising edge of WR# input serves as a data/command WRITE latch signal while CS# is kept LOW.

Figure 8-2 : Example of Write procedure in 8080 parallel interface mode

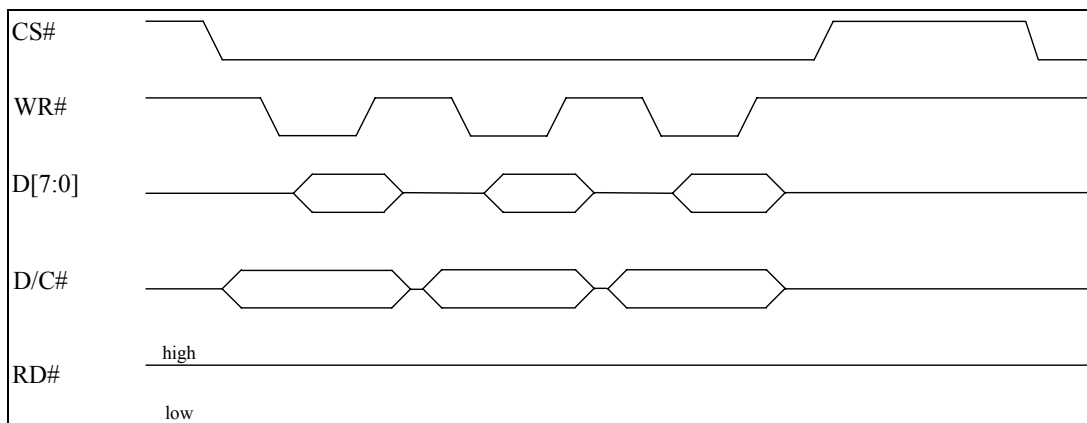


Figure 8-3 : Example of Read procedure in 8080 parallel interface mode

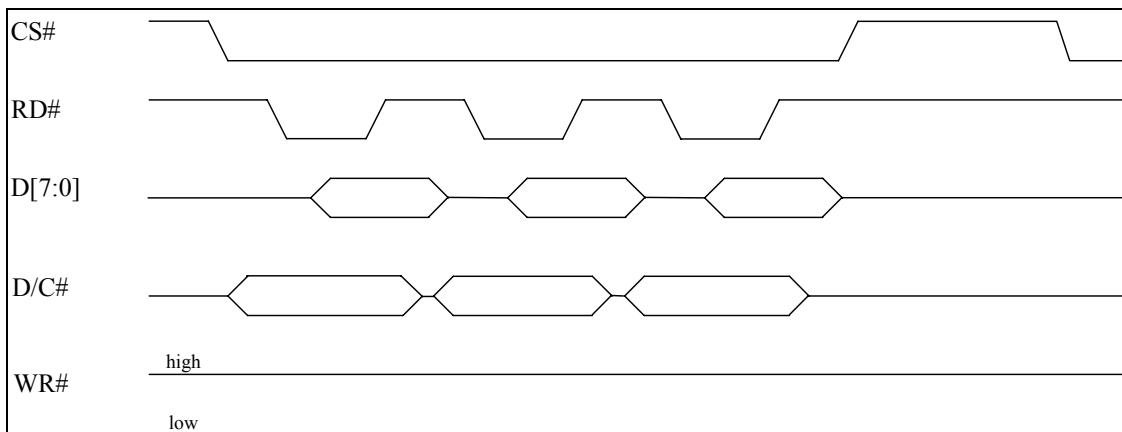


Table 8-3 : Control pins of 8080 interface

| Function | RD# | WR# | CS# | D/C# |
|---------------|-----|-----|-----|------|
| Write command | H | ↑ | L | L |
| Read status | ↑ | H | L | L |
| Write data | H | ↑ | L | H |
| Read data | ↑ | H | L | H |

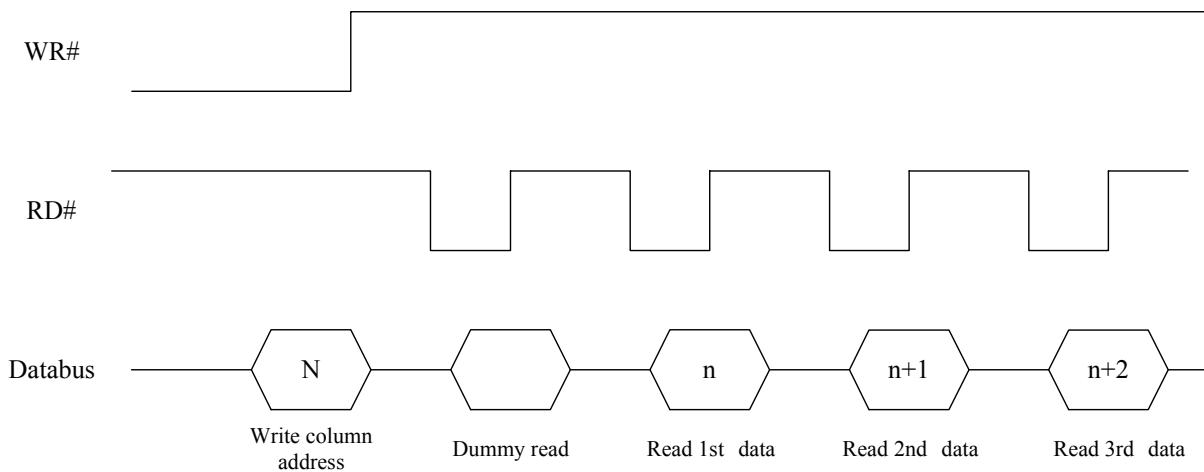
Note

- (1) ↑ stands for rising edge of signal
- (2) H stands for HIGH in signal
- (3) L stands for LOW in signal
- (4) Refer to

Figure 13-2 for Form 1 8080-Series MPU Parallel Interface Timing Characteristics

In order to match the operating frequency of display RAM with that of the microprocessor, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in Figure 8-4.

Figure 8-4 : Display data read back procedure - insertion of dummy read



8.1.3 MCU Serial Interface (4-wire SPI)

The serial interface consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, E and R/W# can be connected to an external ground.

Table 8-4 : Control pins of 4-wire Serial interface

| Function | E(RD#) | R/W#(WR#) | CS# | D/C# | D0 |
|---------------|---------|-----------|-----|------|----|
| Write command | Tie LOW | Tie LOW | L | L | ↑ |
| Write data | Tie LOW | Tie LOW | L | H | ↑ |

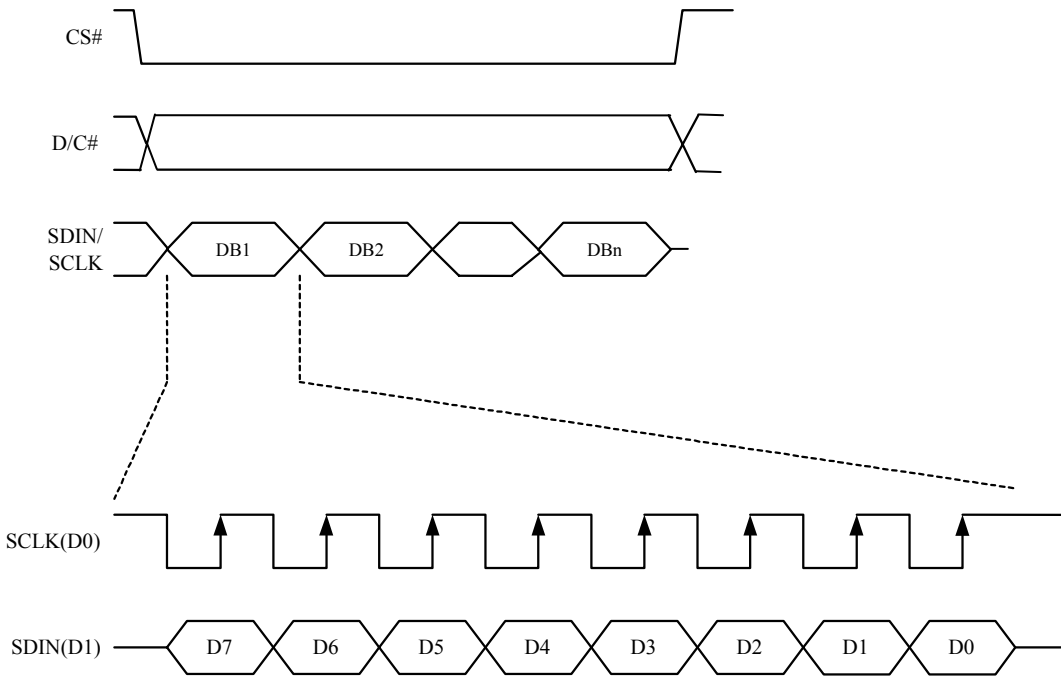
Note

- (1) H stands for HIGH in signal
- (2) L stands for LOW in signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (GDDRAM) or command register in the same clock.

Under serial mode, only write operations are allowed.

Figure 8-5 : Write procedure in 4-wire Serial interface mode



8.1.4 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data SDIN and CS#.

In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN. For the unused data pins, D2 should be left open. The pins from D3 to D7, R/W# (WR#), E(RD#) and D/C# can be connected to an external ground.

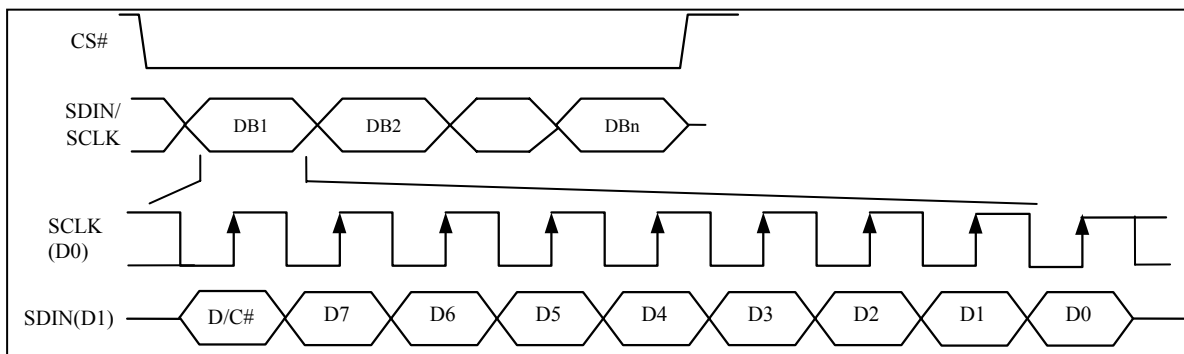
The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0). Under serial mode, only write operations are allowed.

Table 8-5: Control pins of 3-wire Serial interface

| Function | E(RD#) | R/W#(WR#) | CS# | D/C# | D0 |
|---------------|---------|-----------|-----|---------|----|
| Write command | Tie LOW | Tie LOW | L | Tie LOW | ↑ |
| Write data | Tie LOW | Tie LOW | L | Tie LOW | ↑ |

Note
(¹) L stands for LOW in signal

Figure 8-6: Write procedure in 3-wire Serial interface mode



8.2 Reset Circuit

When RES# input is pulled LOW, the chip is initialized with the following status:

1. Display is OFF
2. 128 MUX Display Mode
3. Normal segment and display data column address and row address mapping (SEG0 mapped to address 00h and COM0 mapped to address 00h)
4. Display start line is set at display RAM address 0
5. Column address counter is set at 0
6. Normal scan direction of the COM outputs
7. Contrast control register is set at 7Fh

8.3 GDDRAM

8.3.1 GDDRAM structure in Gray Scale mode

The GDDRAM address map in Table 8-6 shows the GDDRAM in Gray Scale mode. Since in Gray Scale mode, there are 16 gray levels. Therefore four bits (one nibble) are allocated for each pixel. For example D30480[3:0] in Table 8-6 corresponds to the pixel located in (COM127, SEG2). So the lower nibble and higher nibble of D0, D1, D2, ..., D30717, D30718, D30719 in Table 8-6 represent the 480x128 data nibbles in the GDDRAM.

Table 8-6 : GDDRAM in Gray Scale mode (RESET)

| | | SEG0 | SEG1 | SEG2 | SEG3 | | SEG476 | SEG477 | SEG478 | SEG479 | SEG Outputs |
|-----------------------|-------------------------|-------------|-------------|-------------|-------------|--|-------------|-------------|-------------|-------------|-----------------------------------|
| | | 00 | | 00 | | | 77 | | 77 | | RAM Column address (HEX) |
| COM0 | 00 | D1[3:0] | D1[7:4] | D0[3:0] | D0[7:4] | | D239[3:0] | D239[7:4] | D238[3:0] | D238[7:4] | |
| COM1 | 01 | D241[3:0] | D241[7:4] | D240[3:0] | D240[7:4] | | D479[3:0] | D479[7:4] | D478[3:0] | D478[7:4] | |
| | | | | | | | | | | | |
| COM126 | 7E | D30241[3:0] | D30241[7:4] | D30240[3:0] | D30240[7:4] | | D30479[3:0] | D30479[7:4] | D30478[3:0] | D30478[7:4] | |
| COM127 | 7F | D30481[3:0] | D30481[7:4] | D30480[3:0] | D30480[7:4] | | D30719[3:0] | D30719[7:4] | D30718[3:0] | D30718[7:4] | |
| RAM COM Outputs | Row Address (HEX) | | | | | | | | | | |

Corresponding to one pixel

8.3.2 Data bus to RAM mapping

Table 8-7 : Data bus usage

| Read / Write Data | | Data bus D[7:0] | | | | | | | |
|-------------------|-----------------|-----------------|----|----|----|----|----|----|----|
| Bus width | Input order | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 8 bits | 1 st | 3 | 3 | 3 | 3 | 2 | 2 | 2 | 2 |
| | 2 nd | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

Corresponding to one pixel

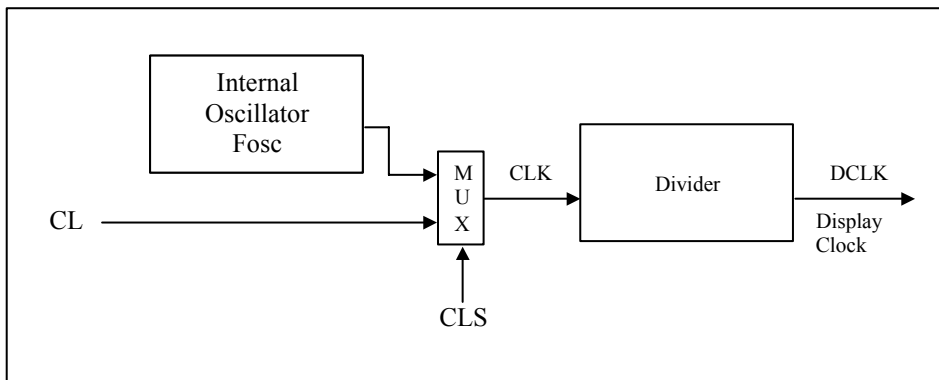
8.4 Command Decoder

This module determines whether the input should be interpreted as data or command based upon the input of the D/C# pin.

If D/C# pin is HIGH, data is written to Graphic Display Data RAM (GDDRAM). If it is LOW, the inputs at D0-D7 are interpreted as a Command and it will be decoded and be written to the corresponding command register.

8.5 Oscillator & Timing Generator

Figure 8-7 : Oscillator Circuit



This module is an On-Chip low power RC oscillator circuitry (Figure 8-7). The operation clock (CLK) can be generated either from internal oscillator or external source CL pin by CLS pin. If CLS pin is HIGH, internal oscillator is selected. If CLS pin is LOW, external clock from CL pin will be used for CLK. The frequency of internal oscillator F_{OSC} can be programmed by command B3h.

The display clock (DCLK) for the Display Timing Generator is derived from CLK. The division factor “D” can be programmed from 1 to 1024 by command B3h.

$$DCLK = F_{OSC} / D$$

The frame frequency of display is determined by the following formula:

$$F_{FRM} = \frac{F_{osc}}{D \times K \times \text{No. of Mux}}$$

where

- D stands for clock divide ratio. It is set by command B3h A[3:0]. The divide ratio has the range from 1 to 1024.
- K is the number of display clocks per row. The value is derived by
 $K = \text{Phase 1 period} + \text{Phase 2 period} + X$
 $X = \text{DCLKs in current drive period. Default } X = \text{constant} + \text{GS15} = 10 + 112 = 122$
 Default K is $9 + 7 + 122 = 138$
- Number of multiplex ratio is set by command A8h. The reset value is 127 (i.e. 128MUX).
- F_{osc} is the oscillator frequency. It can be changed by command B3h A[7:4]. The higher the register setting results in higher frequency.

If the frame frequency is set too low, flickering may occur. On the other hand, higher frame frequency leads to higher power consumption on the whole system.

8.6 SEG/COM Driving Block

This block is used to derive the incoming power sources into the different levels of internal use voltage and current.

- V_{CC} is the most positive voltage supply.
- V_{COMH} is the Common deselected level. It is internally regulated.
- V_{LSS} is the ground path of the analog and panel current.
- I_{REF} is a reference current source for segment current drivers I_{SEG} . The relationship between reference current and segment current of a color is:

$$I_{SEG} = \text{Contrast} / 256 * I_{REF} * \text{scale factor} * 2$$

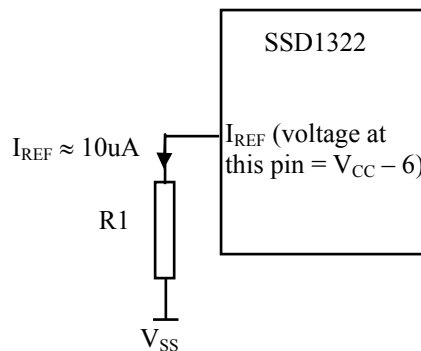
in which

the contrast (0~255) is set by Set Contrast command (C1h); and
the scale factor (1 ~ 16) is set by Master Current Control command (C7h).

For example, in order to achieve $I_{SEG} = 300\mu\text{A}$ at maximum contrast 255, I_{REF} is set to around $10\mu\text{A}$. This current value is obtained by connecting an appropriate resistor from I_{REF} pin to V_{SS} as shown in Figure 8-8.

Recommended $I_{REF} = 10\mu\text{A}$

Figure 8-8 : I_{REF} Current Setting by Resistor Value



Since the voltage at I_{REF} pin is $V_{CC} - 6\text{V}$, the value of resistor R1 can be found as below:

For $I_{REF} = 10\mu\text{A}$, $V_{CC} = 18\text{V}$:

$$\begin{aligned} R1 &= (\text{Voltage at } I_{REF} - V_{SS}) / I_{REF} \\ &= (18 - 6) / 10\mu\text{A} \\ &\approx 1.2\text{M}\Omega \end{aligned}$$

8.7 SEG / COM Driver

Segment drivers consist of 480 current sources to drive OLED panel. The driving current can be adjusted from 0 to 300uA with 8 bits, 256 steps by contrast setting command (C1h). Common drivers generate scanning voltage pulse. The block diagrams and waveforms of the segment and common driver are shown as follow.

Figure 8-9 : Segment and Common Driver Block Diagram – Single COM mode

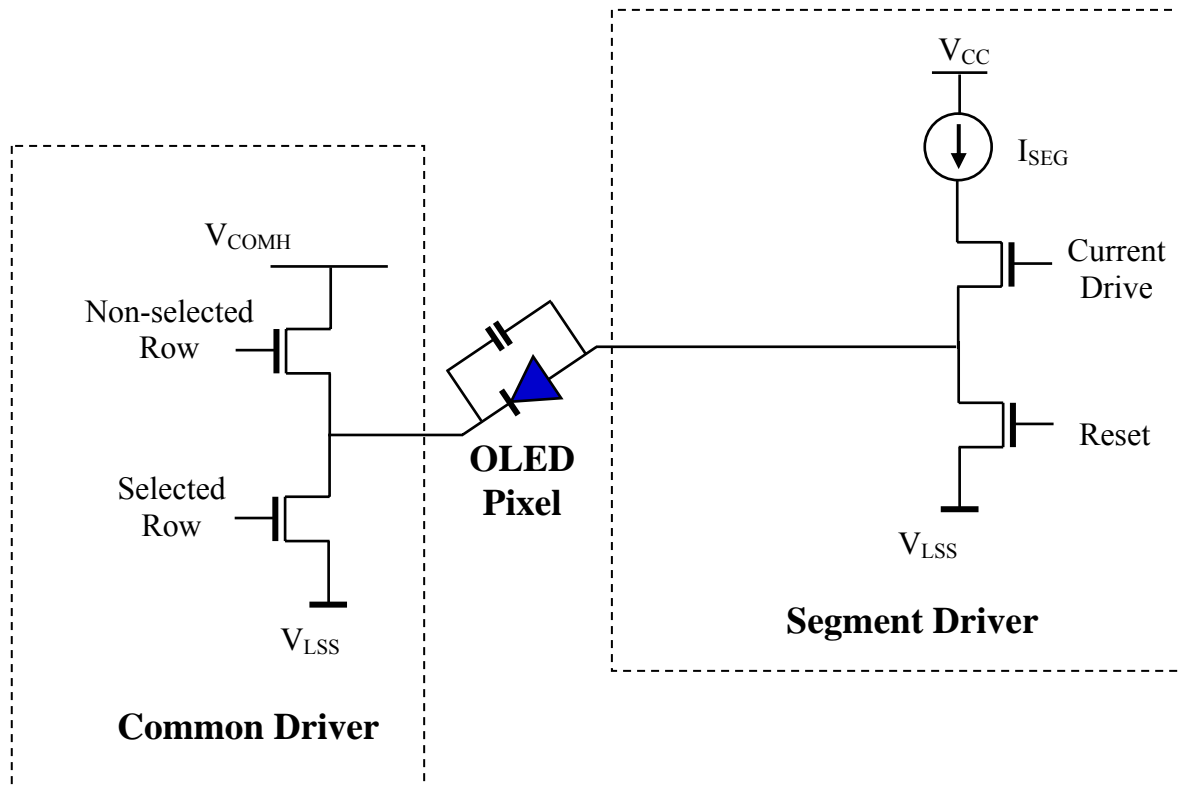
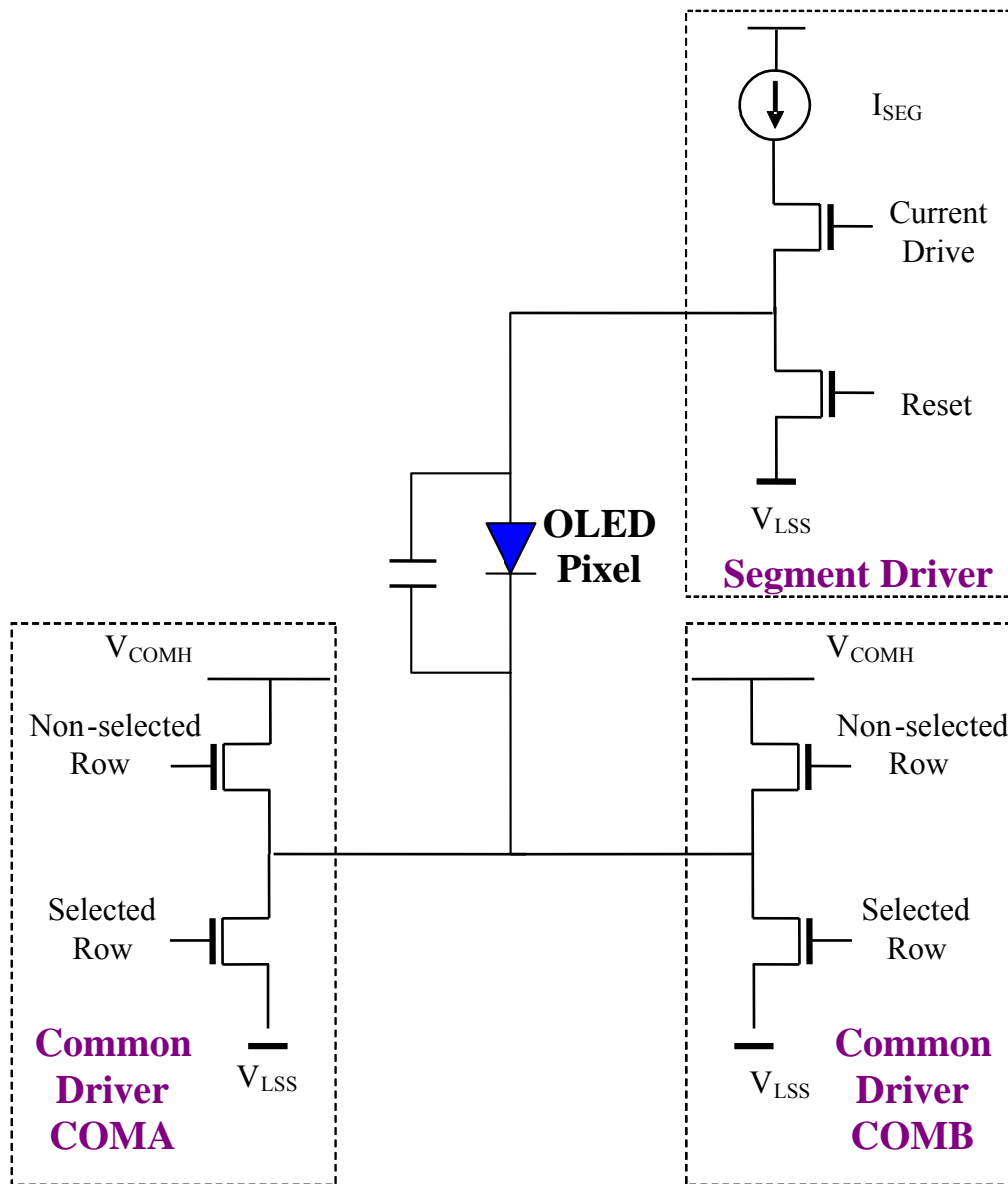


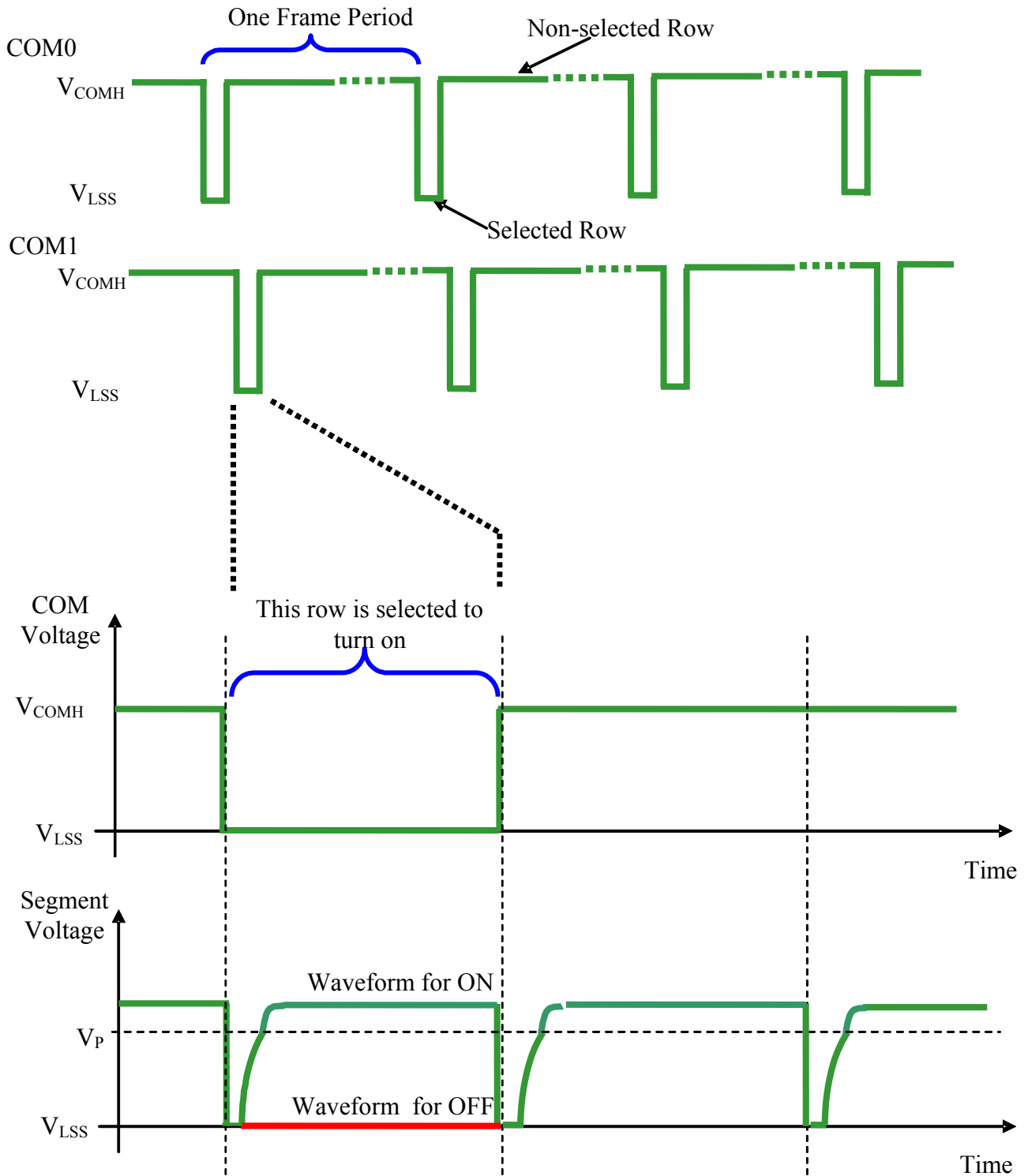
Figure 8-10 : Segment and Common Driver Block Diagram – Dual COM mode



The commons are scanned sequentially, row by row. If a row is not selected, all the pixels on the row are in reverse bias by driving those commons to voltage V_{COMH} as shown in Figure 8-11.

In the scanned row, the pixels on the row will be turned ON or OFF by sending the corresponding data signal to the segment pins. If the pixel is turned OFF, the segment current is kept at 0. On the other hand, the segment drives to I_{SEG} when the pixel is turned ON.

Figure 8-11 : Segment and Common Driver Signal Waveform



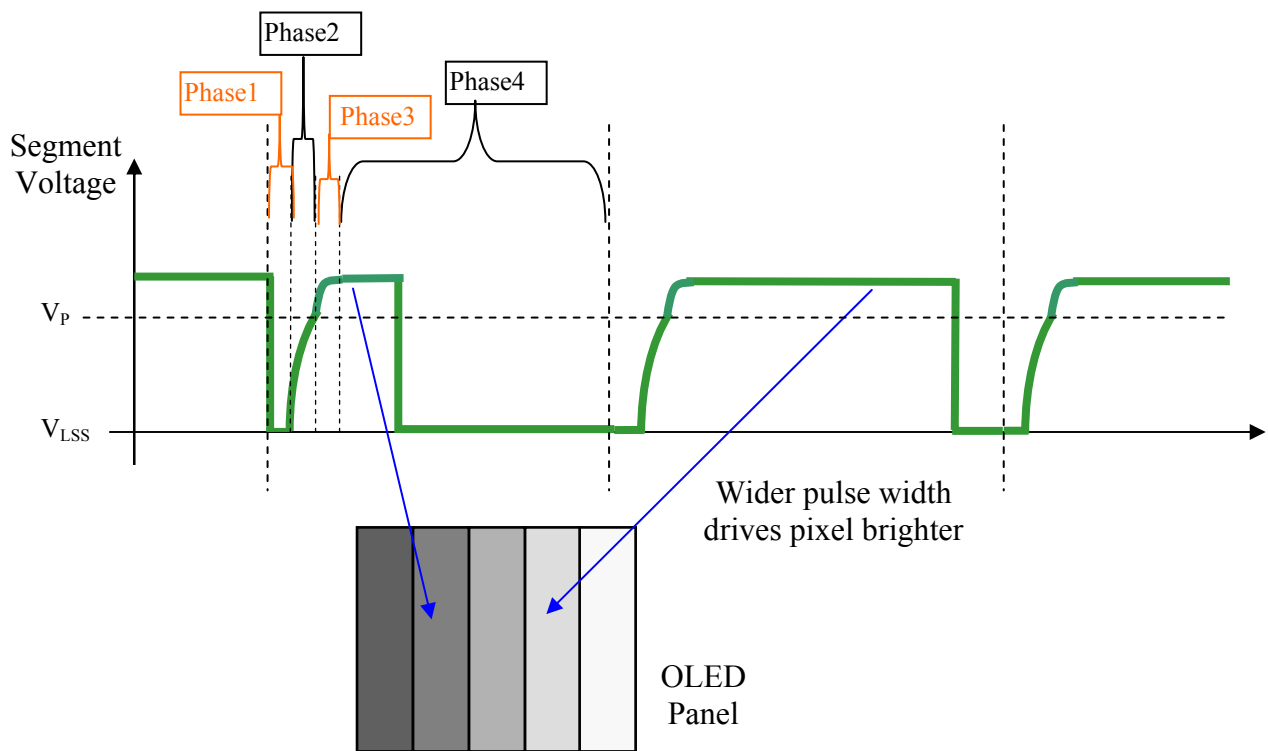
There are four phases to driving an OLED a pixel. In phase 1, the pixel is reset by the segment driver to V_{LSS} in order to discharge the previous data charge stored in the parasitic capacitance along the segment electrode. The period of phase 1 can be programmed by command B1h A[3:0]. An OLED panel with larger capacitance requires a longer period for discharging.

In phase 2, first pre-charge is performed. The pixel is driven to attain the corresponding voltage level V_P from V_{LSS} . The amplitude of V_P can be programmed by the command BBh. The period of phase 2 can be programmed by command B1h A[7:4]. If the capacitance value of the pixel of OLED panel is larger, a longer period is required to charge up the capacitor to reach the desired voltage.

In phase 3, the OLED pixel is driven to the targeted driving voltage through second pre-charge. The second pre-charge can control the speed of the charging process. The period of phase 3 can be programmed by command B6h.

Last phase (phase 4) is current drive stage. The current source in the segment driver delivers constant current to the pixel. The driver IC employs PWM (Pulse Width Modulation) method to control the gray scale of each pixel individually. The gray scale can be programmed into different Gamma settings by command B8h/B9h. The bigger gamma setting (the wider pulse widths) in the current drive stage results in brighter pixels and vice versa (details refer to Section 8.8). This is shown in the following figure.

Figure 8-12 : Gray Scale Control by PWM in Segment



After finishing phase 4, the driver IC will go back to phase 1 to display the next row image data. This four-step cycle is run continuously to refresh image display on OLED panel.

The length of phase 4 is defined by command B8h or B9h. In the table, the gray scale is defined in incremental way, with reference to the length of previous table entry.

8.8 Gray Scale Decoder

The gray scale effect is generated by controlling the pulse width (PW) of current drive phase, except GS0 there is no pre-charge (phase 2, 3) and current drive (phase 4). The driving period is controlled by the gray scale settings (setting 0 ~ setting 180). The larger the setting, the brighter the pixel will be. The Gray Scale Table stores the corresponding gray scale setting of the 16 gray scale levels (GS0~GS15) through the software commands B8h or B9h.

As shown in Figure 8-13, GDDRAM data has 4 bits, represent the 16 gray scale levels from GS0 to GS15. Note that the frame frequency is affected by GS15 setting.

Figure 8-13 : Relation between GDDRAM content and Gray Scale table entry (under command B9h Enable Linear Gray Scale Table)

| GDDRAM data (4 bits) | Gray Scale Table | Default Gamma Setting (Command B9h) |
|----------------------|--------------------|-------------------------------------|
| 0000 | GS0 | Setting 0 |
| 0001 | GS1 ⁽¹⁾ | Setting 0 |
| 0010 | GS2 | Setting 8 |
| 0011 | GS3 | Setting 16 |
| : | : | : |
| : | : | : |
| 1101 | GS13 | Setting 96 |
| 1110 | GS14 | Setting 104 |
| 1111 | GS15 | Setting 112 |

Note:

⁽¹⁾ Both GS0 and GS1 have no 2nd pre-charge (phase 3) and current drive (phase 4), however GS1 has 1st pre-charge (phase 2).

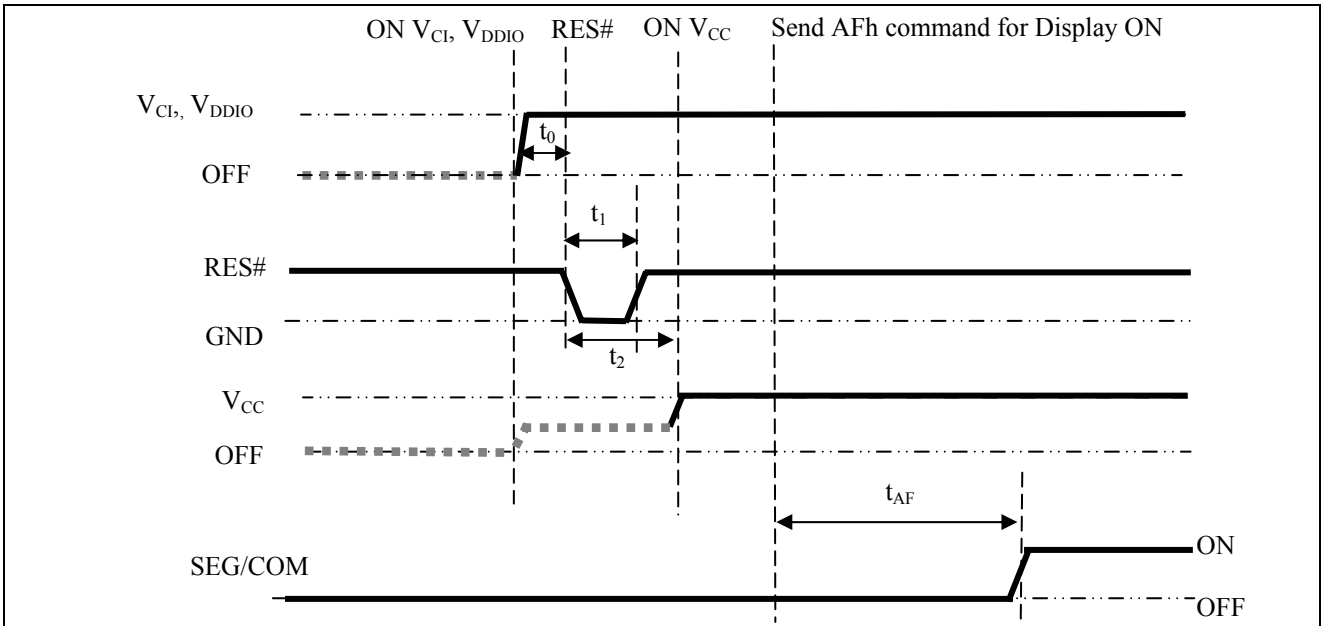
8.9 Power ON and OFF sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1322 (assume V_{CI} and V_{DDIO} are at the same voltage level and internal V_{DD} is used).

Power ON sequence:

1. Power ON V_{CI} , V_{DDIO} .
2. After V_{CI} , V_{DDIO} become stable, set wait time at least 1ms (t_0) for internal V_{DD} become stable. Then set RES# pin LOW (logic low) for at least 100us (t_1)⁽⁴⁾ and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 100us (t_2). Then Power ON V_{CC} .⁽¹⁾
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 200ms (t_{AF}).
5. After V_{CI} become stable, wait for at least 300ms to send command.

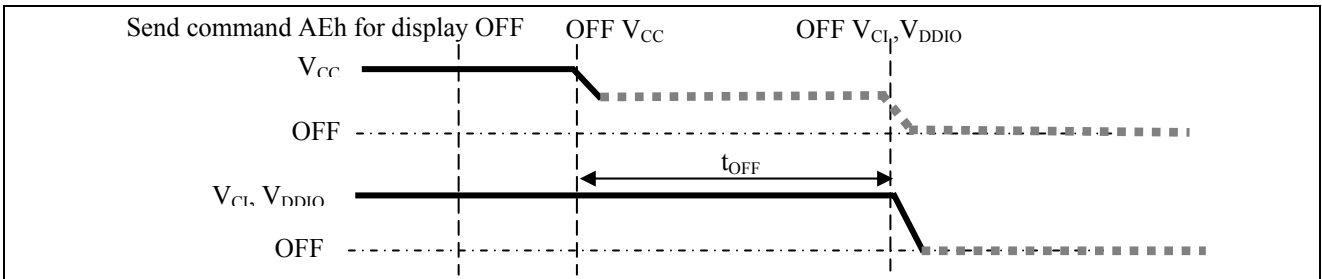
Figure 8-14 : The Power ON sequence.



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC} .^{(1), (2)}
3. Wait for t_{OFF} . Power OFF V_{CI} , V_{DDIO} . (where Minimum $t_{OFF}=0ms$ ⁽³⁾, Typical $t_{OFF}=100ms$)

Figure 8-15 : The Power OFF sequence



Note:

- (1) Since an ESD protection circuit is connected between V_{CI} , V_{DDIO} and V_{CC} , V_{CC} becomes lower than V_{CI} whenever V_{CI} , V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 8-14 and Figure 8-15.
- (2) V_{CC} should be kept float (disable) when it is OFF.
- (3) V_{CI} , V_{DDIO} should not be Power OFF before V_{CC} Power OFF.
- (4) The register values are reset after t_1 .
- (5) Power pins (V_{DD} , V_{CC}) can never be pulled to ground under any circumstance.

8.10 V_{DD} Regulator

In SSD1322, the power supply pin for core logic operation, V_{DD}, can be supplied by external source or internally regulated through the V_{DD} regulator.

The internal V_{DD} regulator is enabled by setting bit A[0] to 1b in command ABh “Function Selection”. V_{CI} should be larger than 2.6V when using the internal V_{DD} regulator. The typical regulated V_{DD} is about 2.5V

It should be notice that, no matter V_{DD} is supplied by external source or internally regulated; V_{CI} must always be set equivalent to or higher than V_{DD} and V_{DDIO}.

The following figure shows the V_{DD} regulator pin connection scheme:

Figure 8-16 V_{CI} > 2.6V, V_{DD} regulator enable pin connection scheme

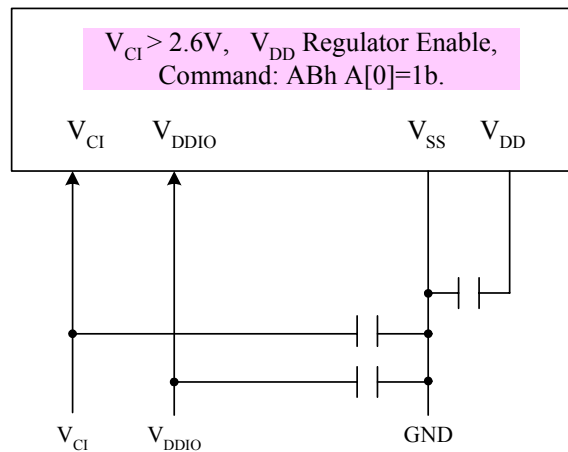
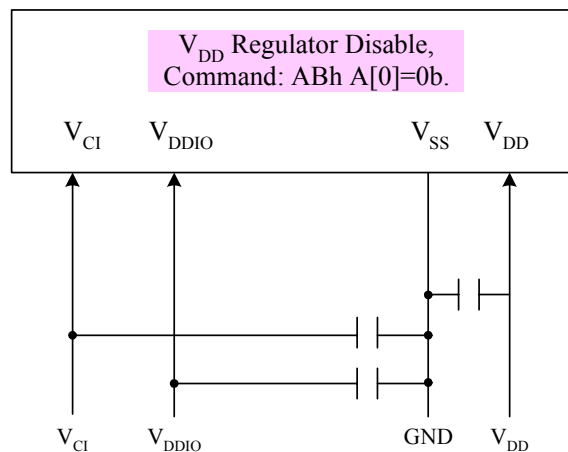


Figure 8-17 V_{DD} regulator disable pin connection scheme



9 COMMAND TABLE

Table 9-1 : Command table

(D/C#=0, R/W#(WR#) = 0, E(RD#)=1) unless specific setting is stated)

Fundamental Command Table

| D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D2 | D0 | Command | Description |
|-------------|------------------------|-------------|----------------------------------------------------|----------------------------------------------------|----------------------------------------------------|----------------------------------------------------|----------------------------------------------------|----------------------------------------------------|----------------------------------------------------|-----------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0 | 00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Enable Gray Scale table | This command is sent to enable the Gray Scale table setting (command B8h) |
| 0 1 1 | 15 A[6:0] B[6:0] | 0 * * | A ₆ A ₆ B ₆ | A ₅ A ₅ B ₅ | A ₄ A ₄ B ₄ | A ₃ A ₃ B ₃ | A ₂ A ₂ B ₂ | A ₁ A ₁ B ₁ | A ₀ A ₀ B ₀ | Set Column Address | Set Column start and end address A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=119] Range from 0 to 119 |
| 0 | 5C | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | Write RAM Command | Enable MCU to write Data into RAM |
| 0 | 5D | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | Read RAM Command | Enable MCU to read Data from RAM |
| 0 1 1 | 75 A[6:0] B[6:0] | 0 * * | A ₆ A ₆ B ₆ | A ₅ A ₅ B ₅ | A ₄ A ₄ B ₄ | A ₃ A ₃ B ₃ | A ₂ A ₂ B ₂ | A ₁ A ₁ B ₁ | A ₀ A ₀ B ₀ | Set Row Address | Set Row start and end address A[6:0]: Start Address. [reset=0] B[6:0]: End Address. [reset=127] Range from 0 to 127 |
| 0 1 1 | A0 A[7:0] B[4] | 1 0 * | 0 0 * | 1 A ₅ 0 | 0 A ₄ B ₄ | 0 0 0 | 0 A ₂ 0 | 0 A ₁ 0 | 0 A ₀ 1 | Set Re-map and Dual COM Line mode | A[0]=0b, Horizontal address increment [reset] A[0]=1b, Vertical address increment A[1]=0b, Disable Column Address Re-map [reset] A[1]=1b, Enable Column Address Re-map A[2]=0b, Disable Nibble Re-map [reset] A[2]=1b, Enable Nibble Re-map A[4]=0b, Scan from COM0 to COM[N-1] [reset] A[4]=1b, Scan from COM[N-1] to COM0, where N is the Multiplex ratio A[5]=0b, Disable COM Split Odd Even [reset] A[5]=1b, Enable COM Split Odd Even B[4], Enable / disable Dual COM Line mode 0b, Disable Dual COM mode [reset] 1b, Enable Dual COM mode (MUX ≤ 63) Note ⁽¹⁾ COM Split Odd Even mode must be disabled (A[5]=0b) when enabling the Dual COM mode (B[4]=1b) Details refer to Section 10.1.6 |
| 0 1 | A1 A[6:0] | 1 * | 0 A ₆ | 1 A ₅ | 0 A ₄ | 0 A ₃ | 0 A ₂ | 0 A ₁ | 1 A ₀ | Set Display Start Line | Set display RAM display start line register from 0-127 Display start line register is reset to 00h after RESET |

| D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D2 | D0 | Command | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------|------------------------|---------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|---------------------------------------|------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|----------------|------|---------|------|---------|------|---------|------|---------|------|-----------------|---|---|------|----------|--------|----------------|------|---------|------|---------|------|---------|------|---------|---|---|------|-----------------|---|---|------|----------|
| 0 1 | A2 A[6:0] | 1 * | 0 A ₆ | 1 A ₅ | 0 A ₄ | 0 A ₃ | 0 A ₂ | 1 A ₁ | 0 A ₀ | Set Display Offset | Set vertical scroll by COM from 0-127 The value is reset to 00H after RESET | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | A4~A7 | 1 | 0 | 1 | 0 | 0 | X ₂ | X ₁ | X ₀ | Set Display Mode | A4h = Entire Display OFF, all pixels turns OFF in GS level 0 A5h = Entire Display ON, all pixels turns ON in GS level 15 A6h = Normal Display [reset] A7h = Inverse Display (GS0 → GS15, GS1 → GS14, GS2 → GS13, ...) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 1 1 | A8 A[6:0] B[6:0] | 1 0 0 | 0 A ₆ B ₆ | 1 A ₅ B ₅ | 0 A ₄ B ₄ | 1 A ₃ B ₃ | 0 A ₂ B ₂ | 0 A ₁ B ₁ | 0 A ₀ B ₀ | Enable Partial Display | This command turns ON partial mode. The partial mode display area is defined by the following two parameters, A[6:0]: Address of start row in the display area B[6:0]: Address of end row in the display area, where B[6:0] must be ≥ A[6:0] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | A9 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | Exit Partial Display | This command is sent to exit the Partial Display mode | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 1 | AB A[0] | 1 0 | 0 0 | 1 0 | 0 0 | 1 0 | 0 0 | 1 0 | 1 A ₀ | Function Selection | A[0]=0b, Select external V _{DD} A[0]=1b, Enable internal V _{DD} regulator [reset] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | AE~AF | 1 | 0 | 1 | 0 | 1 | 1 | 1 | X ₀ | Set Sleep mode ON/OFF | AEh = Sleep mode ON (Display OFF) AFh = Sleep mode OFF (Display ON) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 1 | B1 A[7:0] | 1 A ₇ | 0 A ₆ | 1 A ₅ | 1 A ₄ | 0 A ₃ | 0 A ₂ | 0 A ₁ | 1 A ₀ | Set Phase Length | A[3:0] Phase 1 period (reset phase length) of 5~31 DCLK(s) clocks as follow: <table border="1" data-bbox="1023 1274 1426 1532"> <thead> <tr> <th>A[3:0]</th> <th>Phase 1 period</th> </tr> </thead> <tbody> <tr><td>0000</td><td>invalid</td></tr> <tr><td>0001</td><td>invalid</td></tr> <tr><td>0010</td><td>5 DCLKs</td></tr> <tr><td>0011</td><td>7 DCLKs</td></tr> <tr><td>0100</td><td>9 DCLKs [reset]</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>1111</td><td>31 DCLKs</td></tr> </tbody> </table> A[7:4] Phase 2 period (first pre-charge phase length) of 3~15 DCLK(s) clocks as follow: <table border="1" data-bbox="1031 1684 1418 1973"> <thead> <tr> <th>A[7:4]</th> <th>Phase 2 period</th> </tr> </thead> <tbody> <tr><td>0000</td><td>invalid</td></tr> <tr><td>0001</td><td>invalid</td></tr> <tr><td>0010</td><td>invalid</td></tr> <tr><td>0011</td><td>3 DCLKs</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>0111</td><td>7 DCLKs [reset]</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>1111</td><td>15 DCLKs</td></tr> </tbody> </table> | A[3:0] | Phase 1 period | 0000 | invalid | 0001 | invalid | 0010 | 5 DCLKs | 0011 | 7 DCLKs | 0100 | 9 DCLKs [reset] | : | : | 1111 | 31 DCLKs | A[7:4] | Phase 2 period | 0000 | invalid | 0001 | invalid | 0010 | invalid | 0011 | 3 DCLKs | : | : | 0111 | 7 DCLKs [reset] | : | : | 1111 | 15 DCLKs |
| A[3:0] | Phase 1 period | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0000 | invalid | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0001 | invalid | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0010 | 5 DCLKs | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0011 | 7 DCLKs | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0100 | 9 DCLKs [reset] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| : | : | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1111 | 31 DCLKs | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| A[7:4] | Phase 2 period | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0000 | invalid | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0001 | invalid | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0010 | invalid | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0011 | 3 DCLKs | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| : | : | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0111 | 7 DCLKs [reset] | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| : | : | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1111 | 15 DCLKs | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

| D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D2 | D0 | Command | Description | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------|------------------------|--------------------------|--------------------------|--------------------------|--------------------------|--------------------------|---------------------|--------------------------|--------------------------|---------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|--------|------|-------------|------|-------------|------|-------------|------|-------------|------|--------------|------|--------------|------|--------------|------|---------------|------|---------------|------|---------------|------|----------------|--------|---------|
| 0 1 | B3 A[7:0] | 1 A ₇ | 0 A ₆ | 1 A ₅ | 1 A ₄ | 0 A ₃ | 0 A ₂ | 1 A ₁ | 1 A ₀ | Set Front Clock Divider / Oscillator Frequency | <p>A[3:0] [reset=0], divide by DIVSET where</p> <table border="1"> <thead> <tr> <th>A[3:0]</th> <th>DIVSET</th> </tr> </thead> <tbody> <tr><td>0000</td><td>divide by 1</td></tr> <tr><td>0001</td><td>divide by 2</td></tr> <tr><td>0010</td><td>divide by 4</td></tr> <tr><td>0011</td><td>divide by 8</td></tr> <tr><td>0100</td><td>divide by 16</td></tr> <tr><td>0101</td><td>divide by 32</td></tr> <tr><td>0110</td><td>divide by 64</td></tr> <tr><td>0111</td><td>divide by 128</td></tr> <tr><td>1000</td><td>divide by 256</td></tr> <tr><td>1001</td><td>divide by 512</td></tr> <tr><td>1010</td><td>divide by 1024</td></tr> <tr><td>>=1011</td><td>invalid</td></tr> </tbody> </table> <p>A[7:4] Oscillator frequency, frequency increases as level increases [reset=0101b]</p> | A[3:0] | DIVSET | 0000 | divide by 1 | 0001 | divide by 2 | 0010 | divide by 4 | 0011 | divide by 8 | 0100 | divide by 16 | 0101 | divide by 32 | 0110 | divide by 64 | 0111 | divide by 128 | 1000 | divide by 256 | 1001 | divide by 512 | 1010 | divide by 1024 | >=1011 | invalid |
| A[3:0] | DIVSET | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0000 | divide by 1 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0001 | divide by 2 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0010 | divide by 4 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0011 | divide by 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0100 | divide by 16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0101 | divide by 32 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0110 | divide by 64 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0111 | divide by 128 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1000 | divide by 256 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1001 | divide by 512 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1010 | divide by 1024 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| >=1011 | invalid | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 1 1 | B4 A[1:0] B[7:3] | 1 1 B ₇ | 0 0 B ₆ | 1 1 B ₅ | 1 0 B ₄ | 0 0 B ₃ | 1 0 1 | 0 A ₁ 0 | 0 A ₀ 1 | Display Enhancement A | <p>A[1:0] = 00b: Enable external VSL A[1:0] = 10b: Internal VSL [reset]</p> <p>B[7:3] = 1111b: Enhanced low GS display quality B[7:3] = 10110b: Normal [reset]</p> | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 1 | B5 A[3:0] | 1 * | 0 * | 1 * | 1 * | 0 A ₃ | 1 A ₂ | 0 A ₁ | 1 A ₀ | Set GPIO | <p>A[1:0] GPIO0: 00 pin HiZ, Input disabled 01 pin HiZ, Input enabled 10 pin output LOW [reset] 11 pin output HIGH</p> <p>A[3:2] GPIO1: 00 pin HiZ, Input disabled 01 pin HiZ, Input enabled 10 pin output LOW [reset] 11 pin output HIGH</p> | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 1 | B6 A[3:0] | 1 * | 0 * | 1 * | 1 * | 0 A ₃ | 1 A ₂ | 1 A ₁ | 0 A ₀ | Set Second Precharge Period | <p>A[3:0] Second Pre-charge period 0000b 0 dclk 0001b 1 dclk 1000b 8 dclks [reset] 1111b 15 dclks</p> | | | | | | | | | | | | | | | | | | | | | | | | | | |

| D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D2 | D0 | Command | Description | | | | | | | | | | | | | | | | | | |
|--------|----------|--------------------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|----------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------|----------|--------------------|------|-----|------------------------|---|---|---|------|-----|--------------------------------|---|---|---|-----|-----|------------------------|
| 0 | B8 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | Set Gray Scale Table | <p>The next 15 data bytes define Gray Scale (GS) Table by setting the gray scale pulse width in unit of DCLK's (ranges from 0d ~ 180d)</p> <p>A1[7:0]: Gamma Setting for GS1, A2[7:0]: Gamma Setting for GS2, : A14[7:0]: Gamma Setting for GS14, A15[7:0]: Gamma Setting for GS15</p> <p>Note (1) $0 \leq \text{Setting of GS1} < \text{Setting of GS2} < \text{Setting of GS3} \dots < \text{Setting of GS14} < \text{Setting of GS15}$</p> <p>Refer to Section 8.8 for details</p> <p>(2) The setting must be followed by the Enable Gray Scale Table command (00h)</p> | | | | | | | | | | | | | | | | | | |
| 1 | A1[7:0] | A1 ₇ | A1 ₆ | A1 ₅ | A1 ₄ | A1 ₃ | A1 ₂ | A1 ₁ | A1 ₀ | | | | | | | | | | | | | | | | | | | | |
| 1 | A2[7:0] | A2 ₇ | A2 ₆ | A2 ₅ | A2 ₄ | A2 ₃ | A2 ₂ | A2 ₁ | A2 ₀ | | | | | | | | | | | | | | | | | | | | |
| 1 | . | . | . | . | . | . | . | . | . | | | | | | | | | | | | | | | | | | | | |
| 1 | . | . | . | . | . | . | . | . | . | | | | | | | | | | | | | | | | | | | | |
| 1 | . | . | . | . | . | . | . | . | . | | | | | | | | | | | | | | | | | | | | |
| 1 | A14[7:0] | A14 ₇ | A14 ₆ | A14 ₅ | A14 ₄ | A14 ₃ | A14 ₂ | A14 ₁ | A14 ₀ | | | | | | | | | | | | | | | | | | | | |
| 1 | A15[7:0] | A15 ₇ | A15 ₆ | A15 ₅ | A15 ₄ | A15 ₃ | A15 ₂ | A15 ₁ | A15 ₀ | | | | | | | | | | | | | | | | | | | | |
| 0 | B9 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | Select Default Linear Gray Scale table | <p>The default Linear Gray Scale table is set in unit of DCLK's as follow</p> <p>GS0 level pulse width = 0; GS1 level pulse width = 0; GS2 level pulse width = 8; GS3 level pulse width = 16; : : GS14 level pulse width = 104; GS15 level pulse width = 112</p> <p>Refer to Section 8.8 for details</p> | | | | | | | | | | | | | | | | | | |
| 0 | BB | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | Set Pre-charge voltage | <p>Set pre-charge voltage level.[reset = 17h]</p> <table border="1"> <thead> <tr> <th>A[4:0]</th> <th>Hex code</th> <th>pre-charge voltage</th> </tr> </thead> <tbody> <tr> <td>0000</td> <td>00h</td> <td>0.20 x V_{CC}</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>1111</td> <td>1Fh</td> <td>0.60 x V_{CC}</td> </tr> </tbody> </table> | A[4:0] | Hex code | pre-charge voltage | 0000 | 00h | 0.20 x V _{CC} | : | : | : | 1111 | 1Fh | 0.60 x V _{CC} | | | | | | |
| A[4:0] | Hex code | pre-charge voltage | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0000 | 00h | 0.20 x V _{CC} | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| : | : | : | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1111 | 1Fh | 0.60 x V _{CC} | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | A[4:0] | * | * | * | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | BE | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | Set V _{COMH} | <p>Set COM deselect voltage level [reset = 04h]</p> <table border="1"> <thead> <tr> <th>A[2:0]</th> <th>Hex code</th> <th>V_{COMH}</th> </tr> </thead> <tbody> <tr> <td>000</td> <td>00h</td> <td>0.72 x V_{CC}</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>100</td> <td>04h</td> <td>0.80 x V_{CC} [reset]</td> </tr> <tr> <td>:</td> <td>:</td> <td>:</td> </tr> <tr> <td>111</td> <td>07h</td> <td>0.86 x V_{CC}</td> </tr> </tbody> </table> | A[2:0] | Hex code | V _{COMH} | 000 | 00h | 0.72 x V _{CC} | : | : | : | 100 | 04h | 0.80 x V _{CC} [reset] | : | : | : | 111 | 07h | 0.86 x V _{CC} |
| A[2:0] | Hex code | V _{COMH} | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 000 | 00h | 0.72 x V _{CC} | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| : | : | : | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 100 | 04h | 0.80 x V _{CC} [reset] | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| : | : | : | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 111 | 07h | 0.86 x V _{CC} | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | A[2:0] | * | * | * | * | 0 | A ₂ | A ₁ | A ₀ | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | C1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | Set Contrast Current | <p>A[7:0]: Contrast current value, range:00h~FFh, i.e. 256 steps for I_{SEG} current [reset = 7Fh]</p> | | | | | | | | | | | | | | | | | | |
| 1 | A[7:0] | A ₇ | A ₆ | A ₅ | A ₄ | A ₃ | A ₂ | A ₁ | A ₀ | | | | | | | | | | | | | | | | | | | | |

| D/C# | Hex | D7 | D6 | D5 | D4 | D3 | D2 | D2 | D0 | Command | Description |
|-------------|--------------------|-------------|---------------------|--------------------------|--------------------------|---------------------|---------------------|---------------------|---------------------|------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0 1 | C7 A[3:0] | 1 * | 1 * | 0 * | 0 * | 0 A ₃ | 1 A ₂ | 1 A ₁ | 1 A ₀ | Master Contrast Current Control | A[3:0] = 0000b, reduce output currents for all colors to 1/16 0001b, reduce output currents for all colors to 2/16 : 1110b, reduce output currents for all colors to 15/16 1111b, no change [reset] |
| 0 1 | CA A[6:0] | 1 * | 1 A ₆ | 0 A ₅ | 0 A ₄ | 1 A ₃ | 0 A ₂ | 1 A ₁ | 0 A ₀ | Set MUX Ratio | A[6:0]: Set MUX ratio from 16MUX ~ 128MUX A[6:0] = 15d represents 16MUX : A[6:0] = 127d represents 128MUX [reset] |
| 0 1 1 | D1 A[5:4] 20 | 1 1 0 | 1 0 0 | 0 A ₅ 1 | 1 A ₄ 0 | 0 0 0 | 0 0 0 | 0 1 0 | 1 0 0 | Display Enhancement B | A[5:4] = 00b: Reserved A[5:4] = 10b: Normal [reset] |
| 0 1 | FD A[2] | 1 0 | 1 0 | 1 0 | 1 1 | 1 0 | 1 A ₂ | 0 1 | 1 0 | Set Command Lock | A[2]: MCU protection status [reset = 12h] A[2] = 0b, Unlock OLED driver IC MCU interface from entering command [reset] A[2] = 1b, Lock OLED driver IC MCU interface from entering command Note (1) The locked OLED driver IC MCU interface prohibits all commands and memory access except the FDh command |

Note

(1) “*” stands for “Don’t care”.

10 COMMAND

10.1.1 Enable Gray Scale Table (00h)

This command is sent to enable the Gray Scale Table setting (command B8h).

10.1.2 Set Column Address (15h)

This triple byte command specifies column start address and end address of the display data RAM. This command also sets the column address pointer to column start address. This pointer is used to define the current read/write column address in graphic display data RAM. If horizontal address increment mode is enabled by command A0h, after finishing read/write one column data, it is incremented automatically to the next column address. Whenever the column address pointer finishes accessing the end column address, it is reset back to start column address and the row address is incremented to the next row.

10.1.3 Write RAM Command (5Ch)

After entering this single byte command, data entries will be written into the display RAM until another command is written. Address pointer is increased accordingly. This command must be sent before write data into RAM.

10.1.4 Read RAM Command (5Dh)

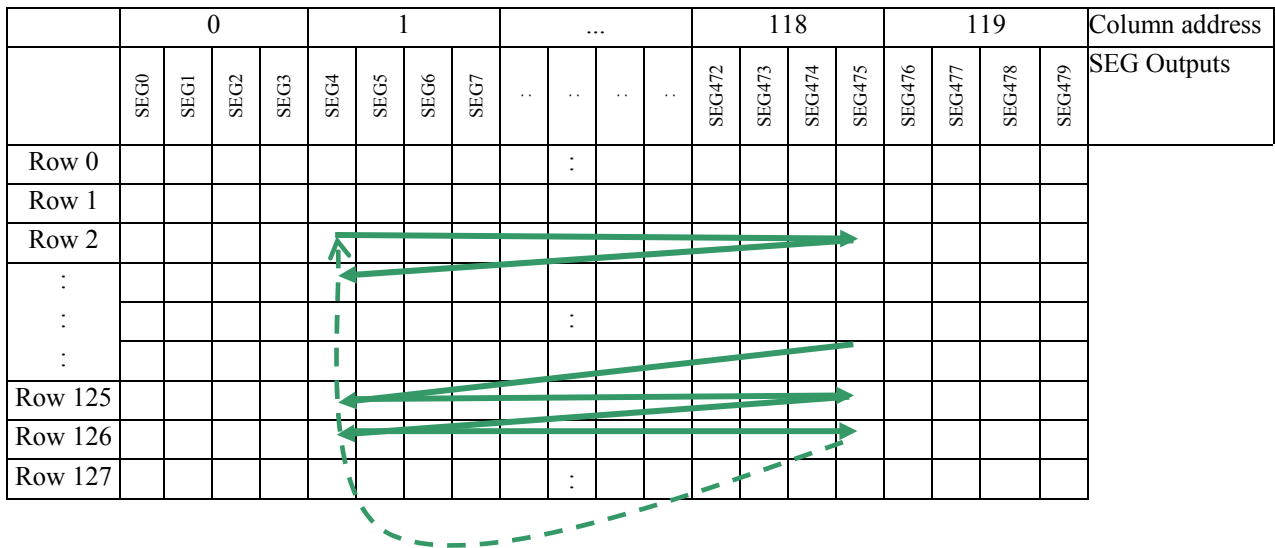
After entering this single byte command, data is read from display RAM until another command is written. Address pointer is increased accordingly. This command must be sent before read data from RAM.

10.1.5 Set Row Address (75h)

This triple byte command specifies row start address and end address of the display data RAM. This command also sets the row address pointer to row start address. This pointer is used to define the current read/write row address in graphic display data RAM. If vertical address increment mode is enabled by command A0h, after finishing read/write one row data, it is incremented automatically to the next row address. Whenever the row address pointer finishes accessing the end row address, it is reset back to start row address.

The diagram below shows the way of column and row address pointer movement through the example: column start address is set to 1 and column end address is set to 118, row start address is set to 2 and row end address is set to 126. Horizontal address increment mode is enabled by command A0h. In this case, the graphic display data RAM column accessible range is from column 1 to column 118 and from row 1 to row 126 only. In addition, the column and row address pointers are set to 1 and 2, respectively. After finishing read/write four pixels of data, the column address is increased automatically by 1 to access the next RAM location for next read/write operation (*solid line in Figure 10-1*). Whenever the column address pointer finishes accessing the end column 118, it is reset back to column 1 and row address is automatically increased by 1 (*solid line in Figure 10-1*). While the end row 126 and end column 118 RAM location is accessed, the row address is reset back to 2 and the column address is reset back to 1 (*dotted line in Figure 10-1*).

Figure 10-110-2 : Example of Column and Row Address Pointer Movement (Gray Scale Mode)

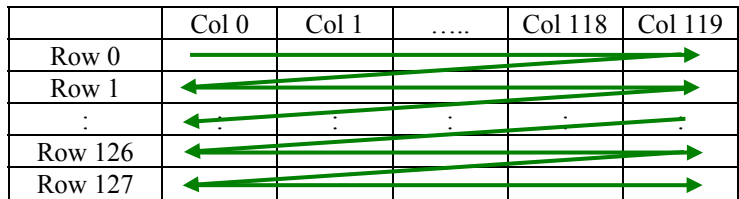


10.1.6 Set Re-map & Dual COM Line Mode (A0h)

This command has multiple configurations and each bit setting is described as follows:

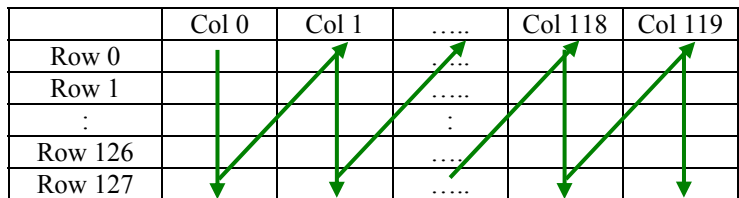
- Address increment mode (A[0])
When A[0] is set to 0, the driver is set as horizontal address increment mode. After the display RAM is read / written, the column address pointer is increased automatically by 1. If the column address pointer reaches column end address, the column address pointer is reset to column start address and row address pointer is increased by 1. The sequence of movement of the row and column address point for horizontal address increment mode is shown in Figure 10-3.

Figure 10-3 : Address Pointer Movement of Horizontal Address Increment Mode



When A[0] is set to 1, the driver is set to vertical address increment mode. After the display RAM is read / written, the row address pointer is increased automatically by 1. If the row address pointer reaches the row end address, the row address pointer is reset to row start address and column address pointer is increased by 1. The sequence of movement of the row and column address point for vertical address increment mode is shown in Figure 10-4.

Figure 10-4: Address Pointer Movement of Vertical Address Increment Mode



- Column Address Remap (A[1])
This command bit is made for increasing the layout flexibility of segment signals in OLED module with segment arranged from left to right (when A[1] is set to 0) or vice versa (when A[1] is set to 1), as demonstrated in Figure 10-5.
A[1] = 0 (reset): RAM Column 0 ~ 119 maps to SEG0-SEG3 ~ SEG476-SEG479
A[1] = 1: RAM Column 0 ~ 119 maps to SEG476-SEG479 ~ SEG0-SEG3
- Nibble Remap (A[2])
A[2] = 0 (reset): Data bits direct mapping is performed
A[2] = 1: The four nibbles of the data bus for RAM access are re-mapped
The effects are demonstrated in Figure 10-5.

Figure 10-5: GDDRAM in Gray Scale mode with or without Column Address (A[1]) & Nibble remapping (A[2])

| | | | SEG0 | SEG1 | SEG2 | SEG3 | SEG4 | SEG5 | SEG6 | SEG7 | : | : | : | : | SEG472 | SEG473 | SEG474 | SEG475 | SEG476 | SEG477 | SEG478 | SEG479 | SEG Outputs |
|------------------|-----------------|-------------------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-----|---|---|---|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|----------------------------|
| | | | SEG479 | SEG478 | SEG477 | SEG476 | SEG475 | SEG474 | SEG473 | SEG472 | : | : | : | : | SEG7 | SEG6 | SEG5 | SEG4 | SEG3 | SEG2 | SEG1 | SEG0 | |
| | | | SEG3 | SEG2 | SEG1 | SEG0 | SEG7 | SEG6 | SEG5 | SEG4 | : | : | : | : | SEG475 | SEG474 | SEG473 | SEG472 | SEG479 | SEG478 | SEG477 | SEG476 | |
| | | | SEG476 | SEG477 | SEG478 | SEG479 | SEG472 | SEG473 | SEG474 | SEG475 | : | : | : | : | SEG4 | SEG5 | SEG6 | SEG7 | SEG0 | SEG1 | SEG2 | SEG3 | |
| | | | 0 | | | | 1 | | | | ... | | | | 76 | | | | 77 | | | | RAM / Column address (HEX) |
| Normal, A[4] = 0 | Remap, A[4] = 1 | | | | | | | | | | | | | | | | | | | | | | |
| COM0 | COM127 | 0 | D1[3:0] | D1[7:4] | D0[3:0] | D0[7:4] | D3[3:0] | D3[7:4] | D2[3:0] | D2[7:4] | : | : | : | : | D237[3:0] | D237[7:4] | D236[3:0] | D236[7:4] | D239[3:0] | D239[7:4] | D238[3:0] | D238[7:4] | |
| COM1 | COM126 | 1 | D241[3:0] | D241[7:4] | D240[3:0] | D240[7:4] | D243[3:0] | D243[7:4] | D242[3:0] | D242[7:4] | : | : | : | : | D477[3:0] | D477[7:4] | D476[3:0] | D476[7:4] | D479[3:0] | D479[7:4] | D478[3:0] | D478[7:4] | |
| : | : | : | | | | | | | | | | | | | | | | | | | | | |
| COM126 | COM1 | 7E | D30241[3:0] | D30241[7:4] | D30240[3:0] | D30240[7:4] | D30243[3:0] | D30243[7:4] | D30242[3:0] | D30242[7:4] | : | : | : | : | D30477[3:0] | D30477[7:4] | D30476[3:0] | D30476[7:4] | D30479[3:0] | D30479[7:4] | D30478[3:0] | D30478[7:4] | |
| COM127 | COM0 | 7F | D30481[3:0] | D30481[7:4] | D30480[3:0] | D30480[7:4] | D30483[3:0] | D30483[7:4] | D30482[3:0] | D30482[7:4] | : | : | : | : | D30717[3:0] | D30717[7:4] | D30716[3:0] | D30716[7:4] | D30719[3:0] | D30719[7:4] | D30718[3:0] | D30718[7:4] | |
| COM Outputs | | RAM / Row address (HEX) | | | | | | | | | | | | | | | | | | | | | |

Corresponding to one pixel

- COM scan direction Remap (A[4])**
 This command bit determines the scanning direction of the common for flexible layout of common signals in OLED module either from up to down or vice versa.
 A[1] = 0 (reset): Scan from up to down
 A[1] = 1: Scan from bottom to up
 Details of pin arrangement can be found in Figure 10-5.
- Odd even split of COM pins (A[5])**
 This command bit can set the odd even arrangement of COM pins.
 A[5] = 0 (reset): Disable COM split odd even, pin assignment of common is in sequential as
 COM127 COM126...COM 65 COM64...SEG479...SEG0...COM0 COM1...COM62 COM63
 A[5] = 1: Enable COM split odd even, pin assignment of common is in odd even split as
 COM127 COM125...COM3 COM1...SEG479...SEG0...COM0 COM2...COM124 COM126
 Details of pin arrangement can be found in Figure 10-6.

- Set Dual COM mode (B[4])
 This command bit can set the dual COM mode.
 B[4] = 0 (reset): Disable the dual COM mode, as shown on Figure 10-6
 B[4] = 1: Enable the dual COM mode, details of pin arrangement can be found in Figure 10-7
 Notice that Odd even split of COM pins must be disabled (A[5]=0) and MUX must be set equating to or smaller than 63 (MUX≤63) when dual COM mode is enabled (B[4]=1).

Figure 10-6 : COM Pins Hardware Configuration – 1 (MUX ratio: 128)

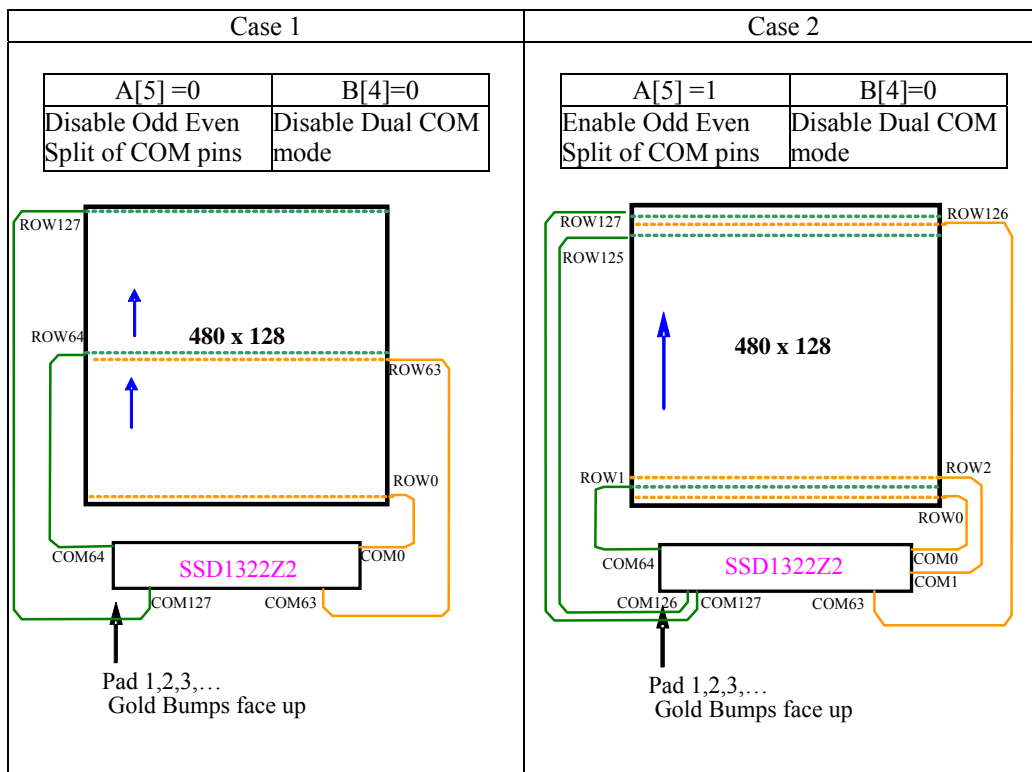
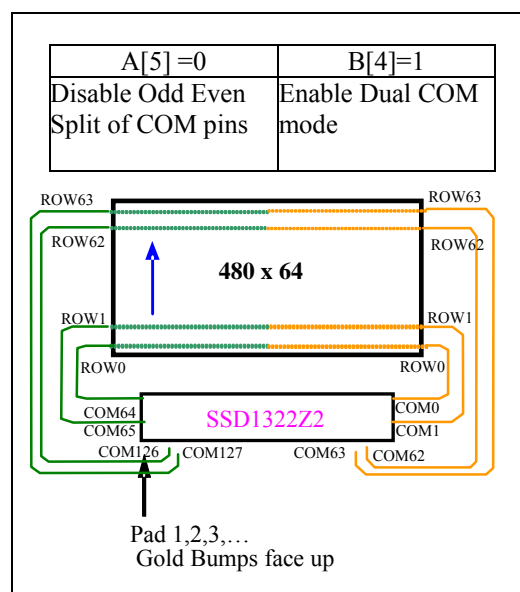






Figure 10-7 : COM Pins Hardware Configuration – 2 (MUX ratio: 64)



10.1.7 Set Display Start Line (A1h)

This command is used to set Display Start Line register to determine starting address of display RAM to be displayed by selecting a value from 0 to 127. Figure 10-8 shows an example of using this command when MUX ratio = 128 and MUX ratio = 90 and Display Start Line = 40. In there, “Row” means the graphic display data RAM row.





Figure 10-8 : Example of Set Display Start Line with no Remap

| | MUX ratio (CAh) = 128 | MUX ratio (CAh) = 128 | MUX ratio (CAh) = 90 | MUX ratio (CAh) = 90 |
|-----------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| COM Pin | Display Start Line (A1h) = 0 | Display Start Line (A1h) = 40 | Display Start Line (A1h) = 0 | Display Start Line (A1h) = 40 |
| COM0 | ROW0 | ROW40 | ROW0 | ROW40 |
| COM1 | ROW1 | ROW41 | ROW1 | ROW41 |
| COM2 | ROW2 | ROW42 | ROW2 | ROW42 |
| COM3 | ROW3 | ROW43 | ROW3 | ROW43 |
| : | : | : | : | : |
| : | : | : | : | : |
| COM48 | ROW48 | ROW88 | ROW48 | ROW88 |
| COM49 | ROW49 | ROW89 | ROW49 | ROW89 |
| COM50 | ROW50 | ROW90 | ROW50 | ROW90 |
| COM51 | ROW51 | ROW91 | ROW51 | ROW91 |
| : | : | : | : | : |
| : | : | : | : | : |
| COM86 | ROW86 | ROW126 | ROW86 | ROW126 |
| COM87 | ROW87 | ROW127 | ROW87 | ROW127 |
| COM88 | ROW88 | ROW0 | ROW88 | ROW0 |
| COM89 | ROW89 | ROW1 | ROW89 | ROW1 |
| COM90 | ROW90 | ROW2 | - | - |
| COM91 | ROW91 | ROW3 | - | - |
| : | : | : | : | : |
| : | : | : | : | : |
| COM124 | ROW124 | ROW36 | - | - |
| COM125 | ROW125 | ROW37 | - | - |
| COM126 | ROW126 | ROW38 | - | - |
| COM127 | ROW127 | ROW39 | - | - |
| Display Example |  |  |  |  |

10.1.8 Set Display Offset (A2h)

This command specifies the mapping of display start line (it is assumed that COM0 is the display start line, display start line register equals to 0) to one of COM0-127. For example, to move the COM39 towards the COM0 direction for 40 lines, the 7-bit data in the second command should be given by 0101000. The figure below shows an example of this command. In there, “Row” means the graphic display data RAM row.

Figure 10-9 : Example of Set Display Offset with no Remap

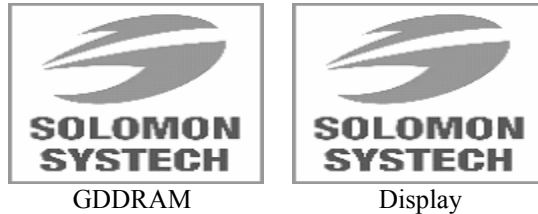
| | MUX ratio (CAh) = 128 | MUX ratio (CAh) = 128 | MUX ratio (CAh) = 90 | MUX ratio (CAh) = 90 |
|-----------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| COM Pin | Display Offset (A2h)=0 | Display Offset (A2h)=40 | Display Offset (A2h)=0 | Display Offset (A2h)=40 |
| COM0 | ROW0 | ROW40 | ROW0 | ROW40 |
| COM1 | ROW1 | ROW41 | ROW1 | ROW41 |
| COM2 | ROW2 | ROW42 | ROW2 | ROW42 |
| COM3 | ROW3 | ROW43 | ROW3 | ROW43 |
| . | . | . | . | . |
| . | . | . | . | . |
| COM48 | ROW48 | ROW88 | ROW48 | ROW88 |
| COM49 | ROW49 | ROW89 | ROW49 | ROW89 |
| COM50 | ROW50 | ROW90 | ROW50 | - |
| COM51 | ROW51 | ROW91 | ROW51 | - |
| . | . | . | . | . |
| . | . | . | . | . |
| COM86 | ROW86 | ROW126 | ROW86 | - |
| COM87 | ROW87 | ROW127 | ROW87 | - |
| COM88 | ROW88 | ROW0 | ROW88 | ROW0 |
| COM89 | ROW89 | ROW1 | ROW89 | ROW1 |
| COM90 | ROW90 | ROW2 | - | ROW2 |
| COM91 | ROW91 | ROW3 | - | ROW3 |
| . | . | . | . | . |
| . | . | . | . | . |
| COM124 | ROW124 | ROW36 | - | ROW36 |
| COM125 | ROW125 | ROW37 | - | ROW37 |
| COM126 | ROW126 | ROW38 | - | ROW38 |
| COM127 | ROW127 | ROW39 | - | ROW39 |
| Display Example |  |  |  |  |

10.1.9 Set Display Mode (A4h ~ A7h)

These are single byte command and they are used to set Normal Display, Entire Display ON, Entire Display OFF and Inverse Display.

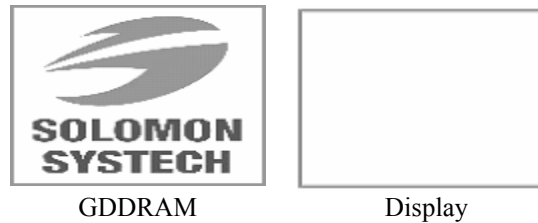
- Normal Display (A4h)
Reset the above effect and turn the data to ON at the corresponding gray level. Figure 10-10 shows an example of Normal Display.

Figure 10-10 : Example of Normal Display



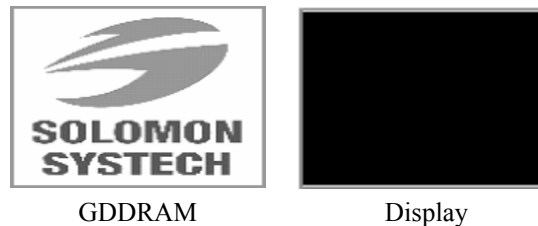
- Set Entire Display ON (A5h)
Force the entire display to be at gray scale “GS15” regardless of the contents of the display data RAM as shown in Figure 10-11.

Figure 10-11 : Example of Entire Display ON



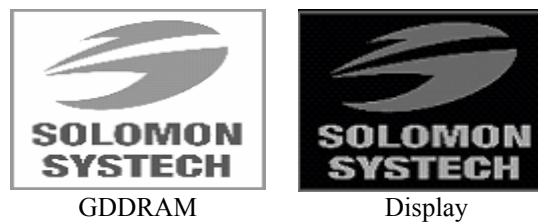
- Set Entire Display OFF (A6h)
Force the entire display to be at gray scale level “GS0” regardless of the contents of the display data RAM as shown in Figure.

Figure 10-12 : Example of Entire Display OFF



- Inverse Display (A7h)
The gray level of display data are swapped such that “GS0” ↔ “GS15”, “GS1” ↔ “GS14”, ...
Figure 10-13 shows an example of inverse display.

Figure 10-13 : Example of Inverse Display



10.1.10 Enable Partial Display (A8h)

The partial mode display area is defined this triple byte command. Figure 10-14 shows an example of enabling the partial mode display with start row address A[6:0] = 20h and end start row address B[6:0] = 5Fh at MUX ratio = 128.

Figure 10-14 : Example of Partial Mode Display



10.1.11 Exit Partial Display (A9h)

This single byte command is sent to exit the partial mode display area (command A8h).

10.1.12 Set Function selection (ABh)

This double byte command is used to enable or disable the V_{DD} regulator.

Internal V_{DD} regulator is selected when the bit A[0] is set to 1b, while external V_{DD} is selected when A[0] is set to 0b.

10.1.13 Set Display ON/OFF (AEh / AFh)

These single byte commands are used to turn the OLED panel display ON or OFF.

When the display is ON (command AFh), the selected circuits by Set Master Configuration command will be turned ON. When the display is OFF (command AEh), those circuits will be turned off, the segment is in V_{SS} state and common is in high impedance state.

10.1.14 Set Phase Length (B1h)

This double byte command sets the length of phase 1 and 2 of segment waveform of the driver.

- Phase 1 (A[3:0]): Set the period from 5 to 31 in the unit of 2 DCLKs. A larger capacitance of the OLED pixel may require longer period to discharge the previous data charge completely.
- Phase 2 (A[7:4]): Set the period from 3 to 15 in the unit of DCLKs. A longer period is needed to charge up a larger capacitance of the OLED pixel to the target voltage V_P .

10.1.15 Set Front Clock Divider / Oscillator Frequency (B3h)

This double byte command consists of two functions:

- Front Clock Divide Ratio (A[3:0])
Set the divide ratio to generate DCLK (Display Clock) from CLK. The divide ratio is from 1 to 16, with reset value = 1. Please refer to Section 8.5 for the detail relationship of DCLK and CLK.
- Oscillator Frequency (A[7:4])
Program the oscillator frequency F_{osc} which is the source of CLK if CLS pin is pulled HIGH. The 4-bit value results in 16 different frequency settings being available.

10.1.16 Display Enhancement A (B4h)

This triple byte command is sent to enhance the display performance. Setting A[1:0] to 00b enables the external VSL, while the low GS display quality would be improved by setting B[7:3] to 11111b.

10.1.17 Set GPIO (B5h)

This double byte command is used to set the states of GPIO0 and GPIO1 pins. Refer to Table 9-1 for details.

10.1.18 Set Second Pre-charge period (B6h)

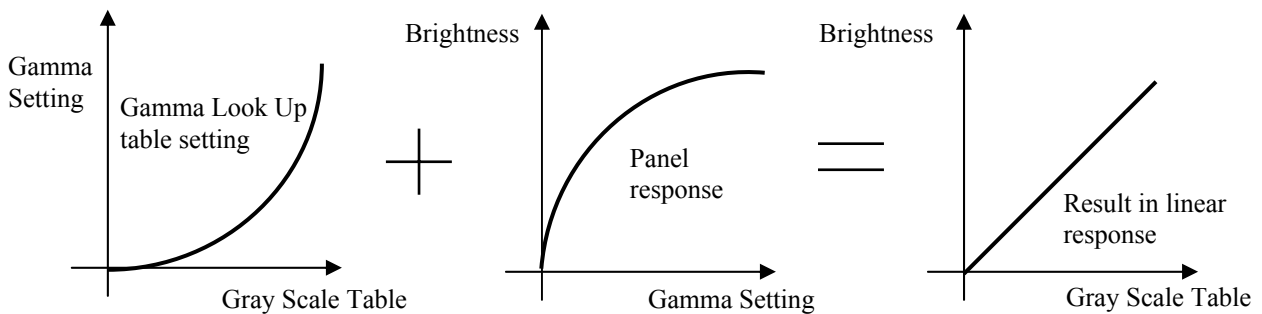
This double byte command is used to set the phase 3 second pre-charge period. The period of phase 3 can be programmed by command B6h and it is ranged from 0 to 15 DCLK's. Please refer to Table 9-1 for the detail information.

10.1.19 Set Gray Scale Table (B8h)

This command is used to set each individual gray scale level for the display. Except gray scale levels GS0 that has no pre-charge and current drive, each gray scale level is programmed in the length of current drive stage pulse width with unit of DCLK. The longer the length of the pulse width, the brighter the OLED pixel when it's turned ON. Following the command B8h, the user has to set the gray scale setting for GS1, GS2, ..., GS14, GS15 one by one in sequence. Refer to Section 8.8 for details.

The setting of gray scale table entry can perform gamma correction on OLED panel display. Since the perception of the brightness scale shall match the image data value in display data RAM, appropriate gray scale table setting like the example shown below (Figure 10-15) can compensate this effect.

Figure 10-15 : Example of Gamma correction by Gamma Look Up table setting



10.1.20 Select Default Linear Gray Scale Table (B9h)

This single byte command reloads the preset linear Gray Scale table as GS0 = Gamma Setting 0, GS1 = Gamma Setting 0, GS2 = Gamma Setting 2, ... GS14 = Gamma Setting 104, GS14 = Gamma Setting 112. Refer to Section 8.8 for details.

10.1.21 Set Pre-charge voltage (BBh)

This double byte command sets the first pre-charge voltage (phase 2) level of segment pins. The level of pre-charge voltage is programmed with reference to V_{CC} . Refer to Table 9-1 for details.

10.1.22 Set V_{COMH} Voltage (BEh)

This double byte command sets the high voltage level of common pins, V_{COMH} . The level of V_{COMH} is programmed with reference to V_{CC} . Refer to Table 9-1 for details.

10.1.23 Set Contrast Current (C1h)

This double byte command is used to set Contrast Setting of the display. The chip has 256 contrast steps from 00h to FFh. The segment output current I_{SEG} increases linearly with the contrast step, which results in brighter display.

10.1.24 Master Current Control (C7h)

This double byte command is to control the segment output current by a scaling factor. The chip has 16 master control steps, with the factor ranges from 1 [0000b] to 16 [1111b – default]. The smaller the master current value, the dimmer the OLED panel display is set.

For example, if original segment output current is 160uA at scale factor = 16, setting scale factor to 8 would reduce the current to 80uA.

10.1.25 Set Multiplex Ratio (CAh)

This double byte command switches default 1:128 multiplex mode to any multiplex mode from 16 to 128. For example, when multiplex ratio is set to 16, only 16 common pins are enabled. The starting and the ending of the enabled common pins are depended on the setting of “Display Offset” register programmed by command A2h. Figure 10-8 and Figure 10-9 show examples of setting the multiplex ratio through command CAh.

10.1.26 Display Enhancement B (D1h)

This triple byte command is sent to enhance the display performance. User is recommended to set A[5:4] to 00b.

10.1.27 Set Command Lock (FDh)

This command is used to lock the OLED driver IC from accepting any command except itself. After entering FDh 16h (A[2]=1b), the OLED driver IC will not respond to any newly-entered command (except FDh 12h A[2]=0b) and there will be no memory access. This is call “Lock” state. That means the OLED driver IC ignore all the commands (except FDh 12h A[2]=0b) during the “Lock” state.

Entering FDh 12h (A[2]=0b) can unlock the OLED driver IC. That means the driver IC resume from the “Lock” state. And the driver IC will then respond to the command and memory access.

11 MAXIMUM RATINGS

Table 11-1 : Maximum Ratings

(Voltage Reference to V_{SS})

| Symbol | Parameter | Value | Unit |
|------------|---------------------------|--------------------------------|------|
| V_{DD} | Supply Voltage | -0.5 to 2.75 | V |
| V_{CC} | | -0.5 to 21.0 | V |
| V_{DDIO} | | -0.5 to V_{CI} | V |
| V_{CI} | | -0.3 to 4.0 | V |
| V_{SEG} | SEG output voltage | 0 to V_{CC} | V |
| V_{COM} | COM output voltage | 0 to $0.9 \cdot V_{CC}$ | V |
| V_{in} | Input voltage | $V_{SS}-0.3$ to $V_{DDIO}+0.3$ | V |
| T_A | Operating Temperature | -40 to +85 | °C |
| T_{stg} | Storage Temperature Range | -65 to +150 | °C |

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description.

*This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

12 DC CHARACTERISTICS

Conditions (Unless otherwise specified):

Voltage referenced to V_{SS}

$V_{DD} = 2.4$ to $2.6V$

$V_{CI} = 2.4$ to $3.5V$ (V_{CI} must be larger than or equal to V_{DD})

$T_A = 25^\circ C$

Table 12-1 : DC Characteristics

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit | |
|------------------|------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------|------|------------------|---------|---------|
| V_{CC} | Operating Voltage | - | 10 | - | 20 | V | |
| V_{DD} | Logic Supply Voltage | - | 2.4 | - | 2.6 | V | |
| V_{CI} | Low voltage power supply | - | 2.4 | - | 3.5 | V | |
| V_{DDIO} | Power Supply for I/O pins | - | 1.65 | - | V_{CI} | V | |
| V_{OH} | High Logic Output Level | $I_{out} = 100\mu A$ | $0.9 * V_{DDIO}$ | - | V_{DDIO} | V | |
| V_{OL} | Low Logic Output Level | $I_{out} = 100\mu A$ | 0 | - | $0.1 * V_{DDIO}$ | V | |
| V_{IH} | High Logic Input Level | - | $0.8 * V_{DDIO}$ | - | V_{DDIO} | V | |
| V_{IL} | Low Logic Input Level | - | 0 | - | $0.2 * V_{DDIO}$ | V | |
| I_{SLP_VDD} | V_{DD} Sleep mode Current | $V_{CI} = V_{DDIO} = 2.8V$, $V_{CC} = OFF$ $V_{DD}(external) = 2.5V$, Display OFF, No panel attached | - | - | 10 | μA | |
| I_{SLP_VDDIO} | V_{DDIO} Sleep mode Current | $V_{CI} = V_{DDIO} = 2.8V$, $V_{CC} = OFF$ Display OFF, No panel attached | External $V_{DD} = 2.5V$ | - | - | 10 | μA |
| | | | Internal V_{DD} | - | - | 10 | μA |
| I_{SLP_VCI} | V_{CI} Sleep mode Current | $V_{CI} = V_{DDIO} = 2.8V$, $V_{CC} = OFF$ Display OFF, No panel attached | External $V_{DD} = 2.5V$ | - | - | 10 | μA |
| | | | Enable Internal V_{DD} during Sleep mode | - | - | 50 | μA |
| | | | Disable Internal V_{DD} during Sleep mode | - | - | 10 | μA |
| I_{DD} | V_{DD} Supply Current | $V_{CI} = 2.8V$, $V_{CC} = 18V$, $V_{DDIO} = 2.8V$, External $V_{DD} = 2.5V$, Display ON, No panel attached, contrast = FF | - | 100 | 130 | μA | |
| I_{DDIO} | V_{DDIO} Supply Current | $V_{CI} = 2.8V$, $V_{CC} = 18V$, $V_{DDIO} = 2.8V$, Display ON, No panel attached, contrast = FF | External $V_{DD} = 2.5V$ | - | 40 | 50 | μA |
| | | | Internal $V_{DD} = 2.5V$ | - | 40 | 50 | μA |
| I_{CI} | V_{CI} Supply Current | $V_{CI} = 2.8V$, $V_{CC} = 18V$, $V_{DDIO} = 2.8V$, Display ON, No panel attached, contrast = FF | External $V_{DD} = 2.5V$ | - | 35 | 45 | μA |
| | | | Internal $V_{DD} = 2.5V$ | - | 170 | 220 | μA |
| I_{CC} | V_{CC} Supply Current | $V_{CI} = 2.8V$, $V_{CC} = 18V$, $V_{DDIO} = 2.8V$, Display ON, No panel attached, contrast = FF | External $V_{DD} = 2.5V$ | - | 2.2 | 2.6 | mA |
| | | | Internal $V_{DD} = 2.5V$ | - | 2.2 | 2.6 | mA |
| I_{SEG} | Segment Output Current Setting $V_{CC} = 20V$, $I_{REF} = 10\mu A$ | Contrast = FF | 310 | 340 | 370 | μA | |
| | | Contrast = 7F | - | 170 | - | μA | |
| | | Contrast = 3F | - | 85 | - | μA | |
| Dev | Segment output current uniformity | $Dev = (I_{SEG} - I_{MID}) / I_{MID}$ $I_{MID} = (I_{MAX} + I_{MIN}) / 2$ $I_{SEG} =$ Segment current at contrast FF | -3 | - | 3 | % | |
| Adj. Dev | Adjacent pin output current uniformity (contrast = FF) | $Adj\ Dev = (I[n] - I[n+1]) / (I[n] + I[n+1])$ | -2 | - | 2 | % | |

13 AC CHARACTERISTICS

Conditions:

Voltage referenced to V_{SS}

V_{DD} = 2.4 to 2.6V

V_{CI} = 2.4 to 3.5V (V_{CI} must be larger than or equal to V_{DD})

T_A = 25°C

Table 13-1 : AC Characteristics

| Symbol | Parameter | Test Condition | Min. | Typ. | Max. | Unit |
|---------------------------------|---------------------------------------------------|-----------------------------------------------------------------------|------|-----------------------------------------------------|------|------|
| F _{OSC} ⁽¹⁾ | Oscillation Frequency of Display Timing Generator | V _{CI} = 2.8V | 1.75 | 1.94 | 2.13 | MHz |
| F _{FRM} | Frame Frequency for 128 MUX Mode | 480x128 Graphic Display Mode, Display ON, Internal Oscillator Enabled | - | F _{OSC} * 1 / (D * K * 128) ⁽²⁾ | - | Hz |
| t _{RES} | Reset low pulse width (RES#) | - | 3 | - | - | us |

Note

⁽¹⁾ F_{OSC} stands for the frequency value of the internal oscillator and the value is measured when command B3h A[7:4] is in default value.

⁽²⁾ D: divide ratio

K: Phase 1 period + Phase 2 period + X

X: DCLKs in current drive period.

Default K is 9 + 7 + 122 = 138

Table 13-2 : 6800-Series MCU Parallel Interface Timing Characteristics

($V_{DD} - V_{SS} = 2.4$ to $2.6V$, $V_{DDIO} = 1.6V$, $V_{CI} = 3.3V$, $T_A = 25^\circ C$)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|--------------------------------------|-----|-----|-----|------|
| t_{cycle} | Clock Cycle Time | 300 | - | - | ns |
| t_{AS} | Address Setup Time | 10 | - | - | ns |
| t_{AH} | Address Hold Time | 0 | - | - | ns |
| t_{DSW} | Write Data Setup Time | 40 | - | - | ns |
| t_{DHW} | Write Data Hold Time | 7 | - | - | ns |
| t_{DHR} | Read Data Hold Time | 20 | - | - | ns |
| t_{OH} | Output Disable Time | - | - | 70 | ns |
| t_{ACC} | Access Time | - | - | 140 | ns |
| PW_{CSL} | Chip Select Low Pulse Width (read) | 120 | - | - | ns |
| | Chip Select Low Pulse Width (write) | 60 | - | - | ns |
| PW_{CSH} | Chip Select High Pulse Width (read) | 60 | - | - | ns |
| | Chip Select High Pulse Width (write) | 60 | - | - | ns |
| t_R | Rise Time | - | - | 15 | ns |
| t_F | Fall Time | - | - | 15 | ns |

Figure 13-1 : 6800-series MCU parallel interface characteristics

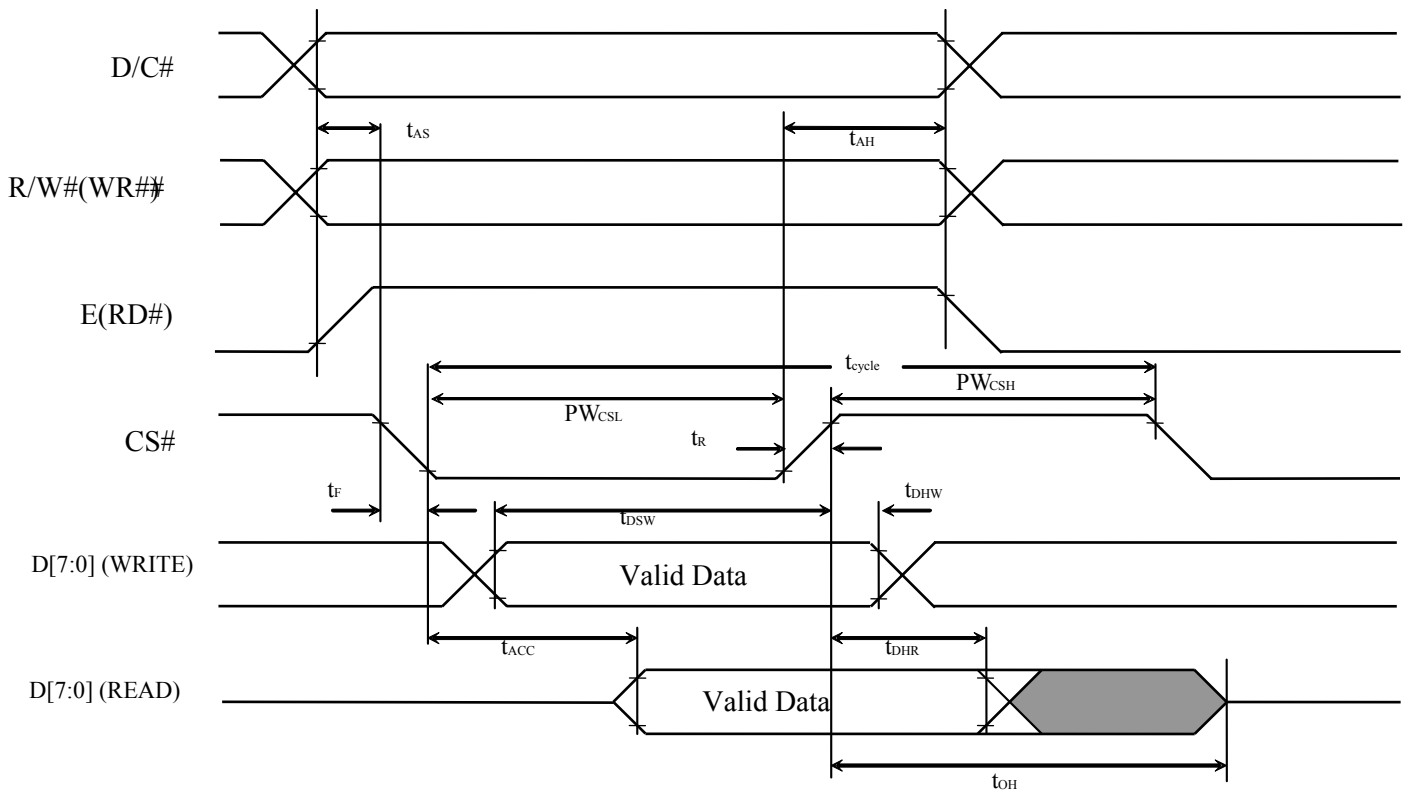


Table 13-3 : 8080-Series MCU Parallel Interface Timing Characteristics

($V_{DD} - V_{SS} = 2.4$ to $2.6V$, $V_{DDIO} = 1.6V$, $V_{CI} = 3.3V$, $T_A = 25^\circ C$)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|--------------------------------------|-----|-----|-----|------|
| t_{cycle} | Clock Cycle Time | 300 | - | - | ns |
| t_{AS} | Address Setup Time | 10 | - | - | ns |
| t_{AH} | Address Hold Time | 0 | - | - | ns |
| t_{DSW} | Write Data Setup Time | 40 | - | - | ns |
| t_{DHW} | Write Data Hold Time | 7 | - | - | ns |
| t_{DHR} | Read Data Hold Time | 20 | - | - | ns |
| t_{OH} | Output Disable Time | - | - | 70 | ns |
| t_{ACC} | Access Time | - | - | 140 | ns |
| t_{PWLR} | Read Low Time | 150 | - | - | ns |
| t_{PWLW} | Write Low Time | 60 | - | - | ns |
| t_{PWHR} | Read High Time | 60 | - | - | ns |
| t_{PWHW} | Write High Time | 60 | - | - | ns |
| t_R | Rise Time | - | - | 15 | ns |
| t_F | Fall Time | - | - | 15 | ns |
| t_{CS} | Chip select setup time | 0 | - | - | ns |
| t_{CSH} | Chip select hold time to read signal | 0 | - | - | ns |
| t_{CSF} | Chip select hold time | 20 | - | - | ns |

Figure 13-2 : 8080-series MCU parallel interface characteristics

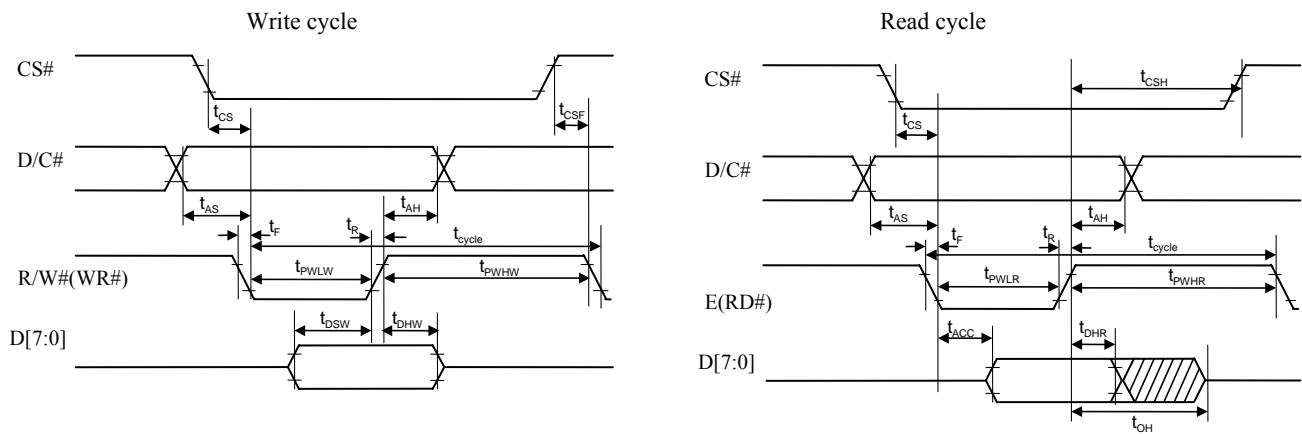


Table 13-4 : Serial Interface Timing Characteristics (4-wire SPI)

($V_{DD} - V_{SS} = 2.4$ to $2.6V$, $V_{DDIO} = 1.6V$, $V_{CI} = 3.3V$, $T_A = 25^\circ C$)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|------------------------|-----|-----|-----|------|
| t_{cycle} | Clock Cycle Time | 100 | - | - | ns |
| t_{AS} | Address Setup Time | 15 | - | - | ns |
| t_{AH} | Address Hold Time | 15 | - | - | ns |
| t_{CSS} | Chip Select Setup Time | 20 | - | - | ns |
| t_{CSH} | Chip Select Hold Time | 10 | - | - | ns |
| t_{DSW} | Write Data Setup Time | 15 | - | - | ns |
| t_{DHW} | Write Data Hold Time | 15 | - | - | ns |
| t_{CLKL} | Clock Low Time | 20 | - | - | ns |
| t_{CLKH} | Clock High Time | 20 | - | - | ns |
| t_R | Rise Time | - | - | 15 | ns |
| t_F | Fall Time | - | - | 15 | ns |

Figure 13-3 : Serial interface characteristics (4-wire SPI)

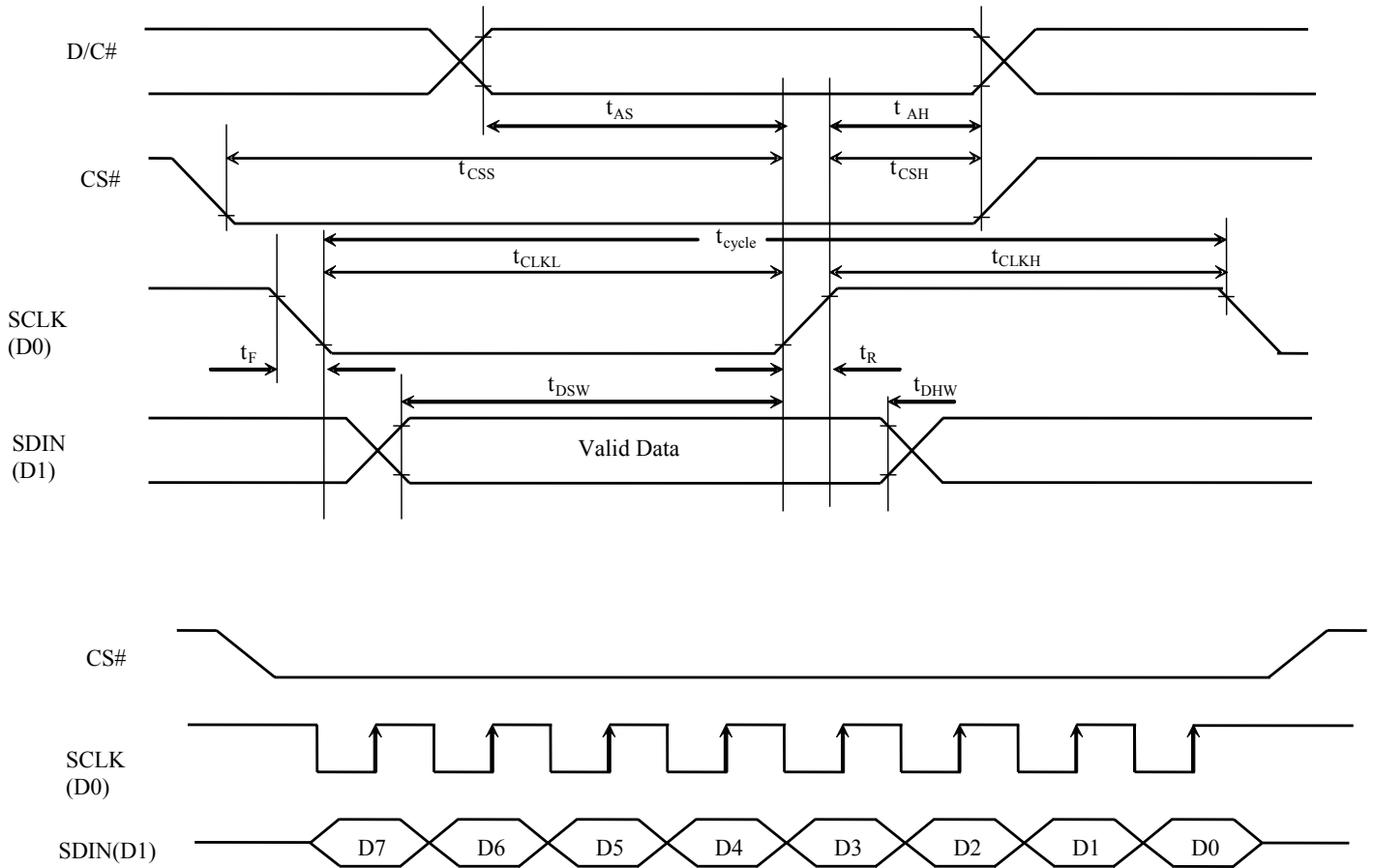
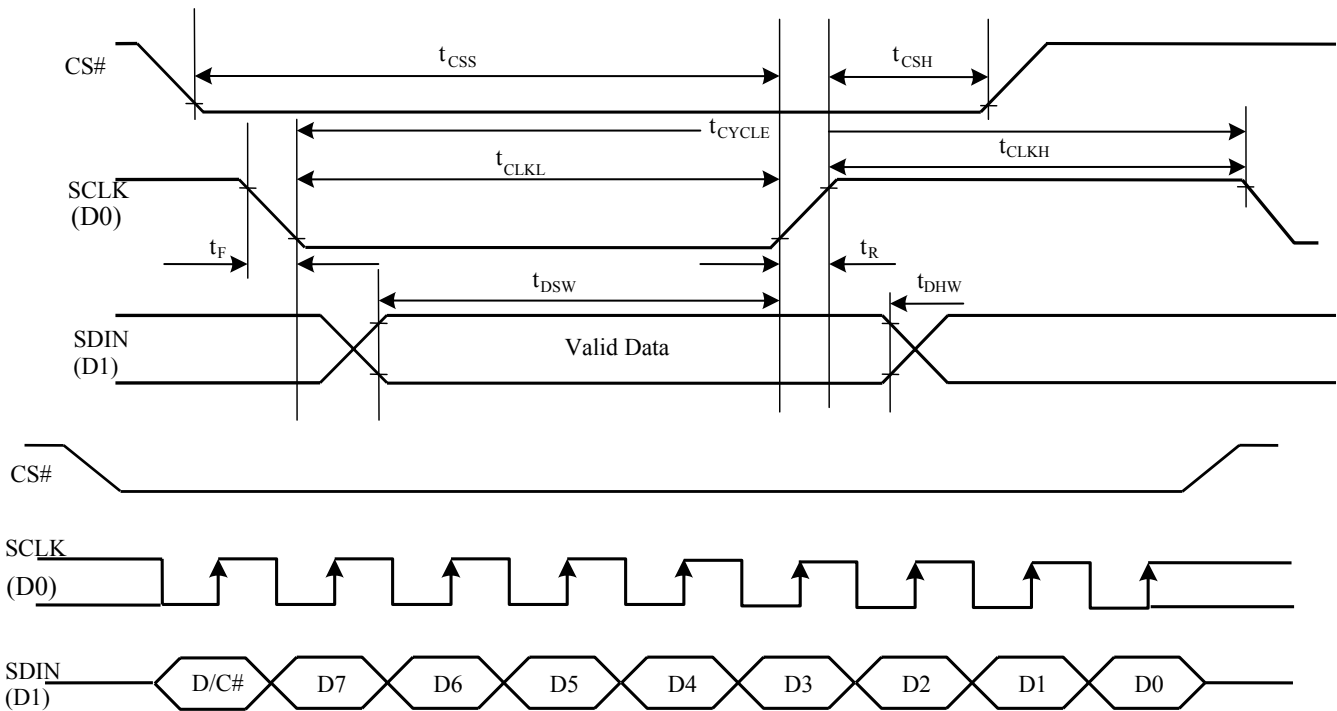


Table 13-5: Serial Interface Timing Characteristics (3-wire SPI)

($V_{DD} - V_{SS} = 2.4$ to $2.6V$, $V_{DDIO} = 1.6V$, $V_{CI} = 3.3V$, $T_A = 25^\circ C$)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------|------------------------|-----|-----|-----|------|
| t_{cycle} | Clock Cycle Time | 100 | - | - | ns |
| t_{CSS} | Chip Select Setup Time | 20 | - | - | ns |
| t_{CSH} | Chip Select Hold Time | 10 | - | - | ns |
| t_{DSW} | Write Data Setup Time | 15 | - | - | ns |
| t_{DHW} | Write Data Hold Time | 15 | - | - | ns |
| t_{CLKL} | Clock Low Time | 20 | - | - | ns |
| t_{CLKH} | Clock High Time | 20 | - | - | ns |
| t_R | Rise Time | - | - | 15 | ns |
| t_F | Fall Time | - | - | 15 | ns |

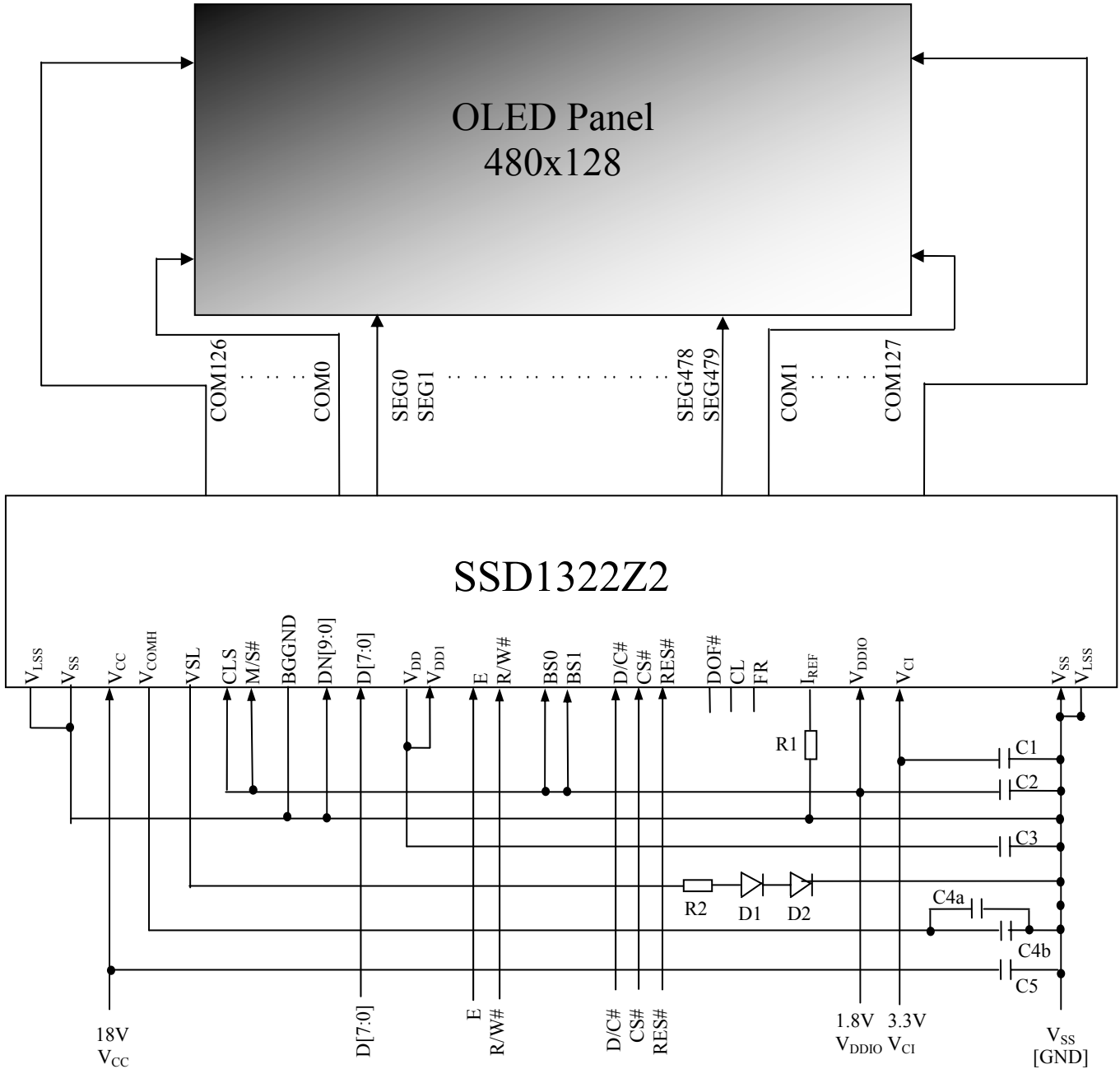
Figure 13-4: Serial interface characteristics (3-wire SPI)



14 APPLICATION EXAMPLES

Figure 14-1 : SSD1322 application example for 8-bit 6800-parallel interface mode (Internal regulated V_{DD})

The configuration for 8-bit 6800-parallel interface mode, externally V_{CC} is shown in the following diagram:
(V_{CI} = 3.3V (V_{CI} must be > 2.6V), Internal regulated V_{DD} = 2.5V, V_{DDIO} = 1.8V, external V_{CC} = 18V, I_{REF} = 10uA)



Voltage at I_{REF} = V_{CC} - 6V. For V_{CC} = 18V, I_{REF} = 10uA:

$$R1 = (\text{Voltage at } I_{REF} - V_{SS}) / I_{REF}$$

$$= (18 - 6) / 10\mu$$

$$= 1.2M\Omega$$

$$R2 = 50\Omega, 1/8W^{(1)}$$

$$D1 - D2 = V_{th} = 0.7V, 1N4148^{(1)}$$

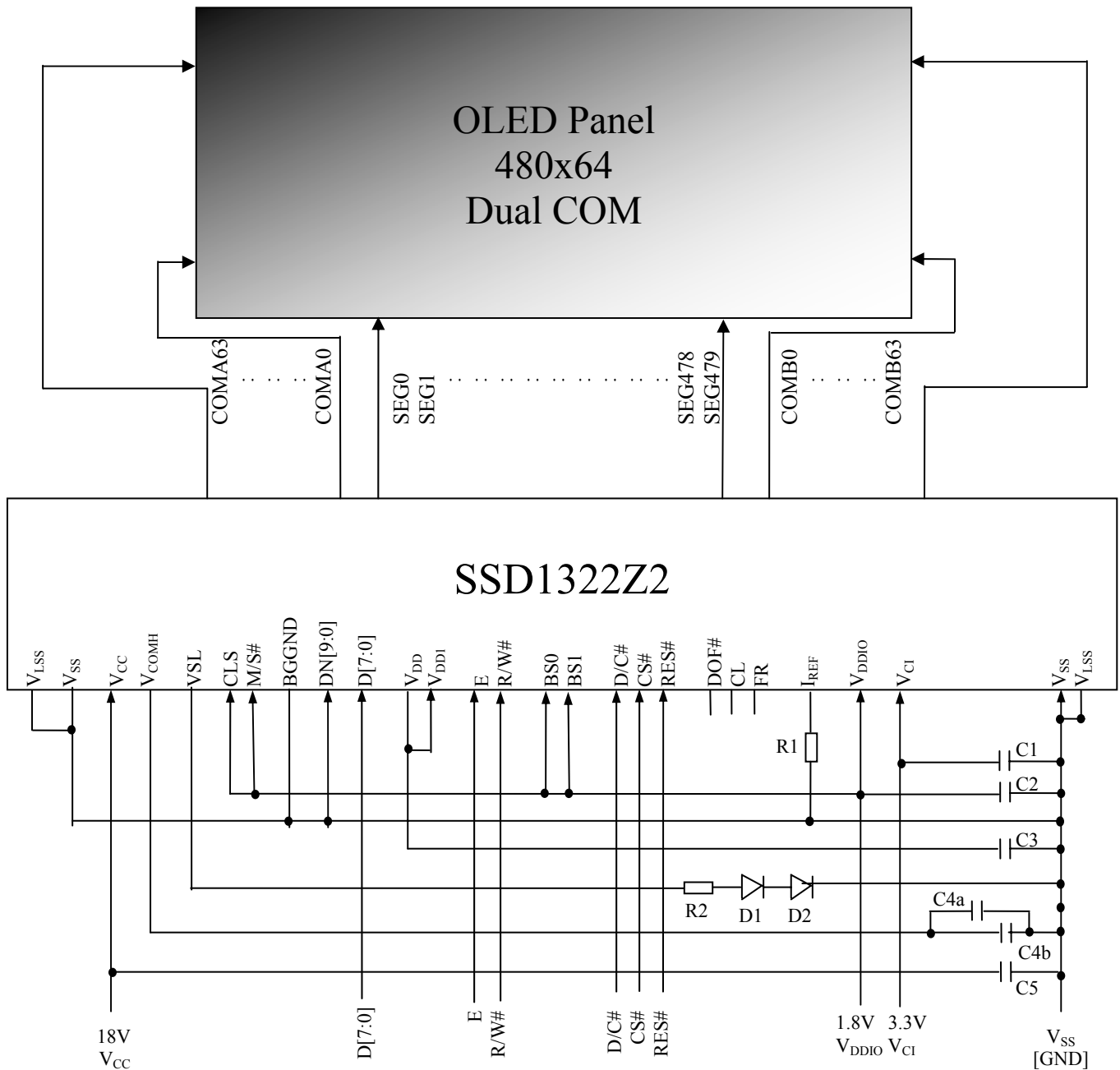
$$C1 \sim C3: 1\mu F, C4a \text{ and } C5: 4.7\mu F, C4b: 0.1\mu F$$

Note

⁽¹⁾ The value is recommended value. Select appropriate value against module application.

Figure 14-2 : SSD1322 application example for 8-bit 6800-parallel interface, dual COM mode (Internal V_{DD})

The configuration for 8-bit 6800-parallel interface mode, externally V_{CC} is shown in the following diagram:
 (V_{CI} = 3.3V (V_{CI} must be > 2.6V), Internal regulated V_{DD} = 2.5V, V_{DDIO} = 1.8V, external V_{CC} = 18V, I_{REF} = 10uA)



Voltage at I_{REF} = V_{CC} - 6V. For V_{CC} = 18V, I_{REF} = 10uA:

$$R1 = (\text{Voltage at } I_{REF} - V_{SS}) / I_{REF}$$

$$= (18 - 6) / 10\mu$$

$$= 1.2M\Omega$$

R2 = 50Ω, 1/8W⁽¹⁾

D1 - D2 = V_{th} = 0.7V, 1N4148⁽¹⁾

C1 ~ C3: 1uF, C4a and C5: 4.7uF, C4b: 0.1uF

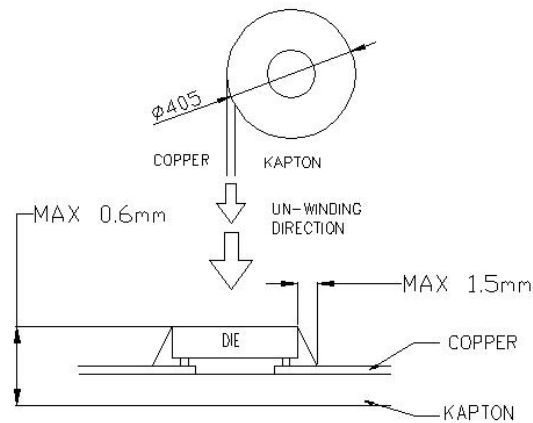
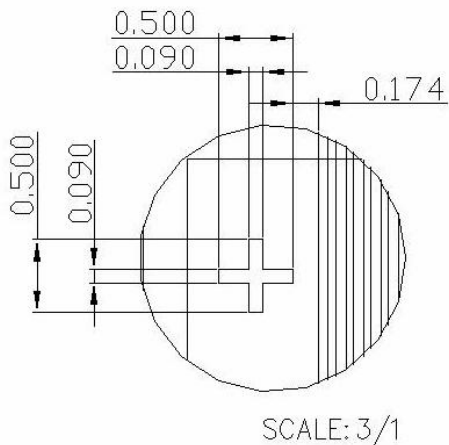
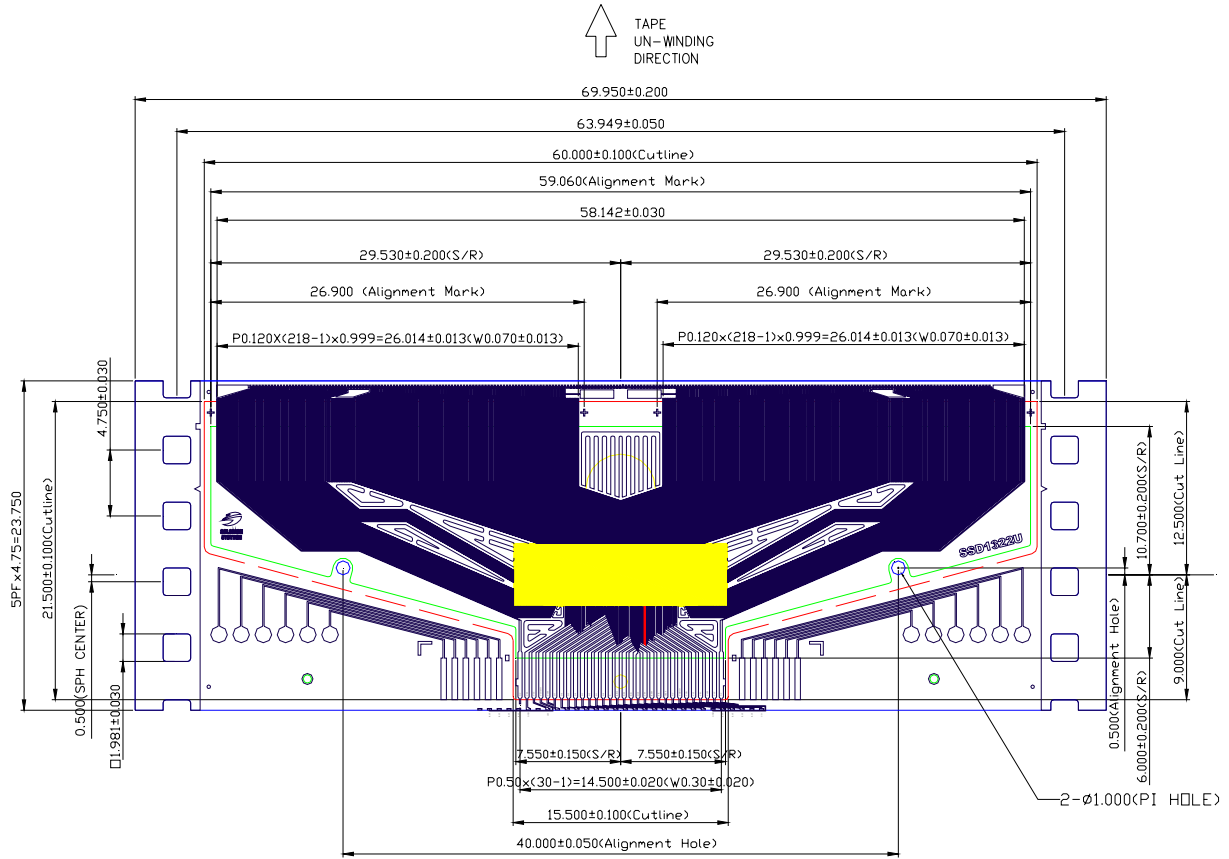
Note

⁽¹⁾ The value is recommended value. Select appropriate value against module application.

15 PACKAGE INFORMATION

15.1 SSD1322UR1 detail dimension

Figure 15-1: SSD1322UR1 Detail Dimension



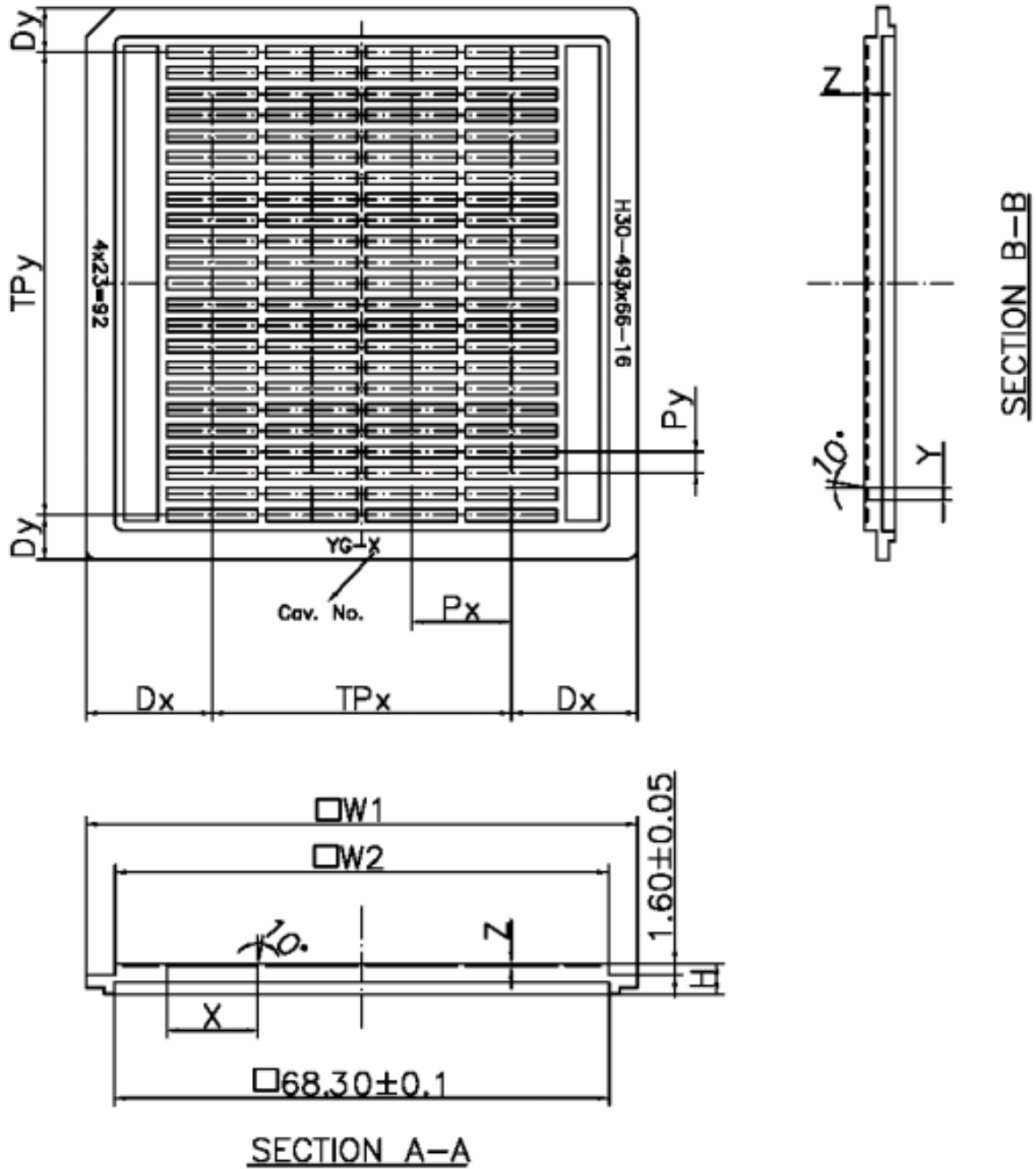
MIRROR DESIGN

NOTE:

1. GENERAL TOLERANCE: $\pm 0.05\text{mm}$
2. MATERIAL
 - PI: $38 \pm 4\mu\text{m}$
 - CU: $8 \pm 2\mu\text{m}$
 - SR: $15 \pm 10\mu\text{m}$
 - (OTHER TOLERANCE: $\pm 0.200\text{mm}$)
3. Sn PLATING $0.16 \pm 0.050\mu\text{m}$
4. TAP SITE: 5 SPH, 23.75mm

15.2 SSD1322Z2 Die Tray Information

Figure 15-2: SSD1322Z2 Die Tray Drawing



Remark

1. Tray material: ABS
2. Tray color code: Black
3. Surface resistance $10^9 \sim 10^{12} \Omega$
4. Pocket bottom: Rough Surface

Table 15-1: SSD1322Z2 Die Tray Dimensions

| Parameter | Dimensions | |
|-------------------|--------------------|--------|
| | mm | (mil) |
| W1 | 76.00±0.10 | (2992) |
| W2 | 68.00±0.10 | (2677) |
| H | 4.20±0.10 | (165) |
| D _X | 17.39±0.10 | (685) |
| TP _X | 41.22±0.10 | (1623) |
| D _Y | 6.10±0.10 | (240) |
| TP _Y | 63.80±0.10 | (2512) |
| P _X | 13.74±0.05 | (541) |
| P _Y | 2.90±0.05 | (114) |
| X | 12.52±0.05 | (493) |
| Y | 1.68±0.05 | (66) |
| Z | 0.40±0.05 | (16) |
| | | |
| N (number of die) | 92 (pocket number) | |

Solomon Systech reserves the right to make changes without notice to any products herein. Solomon Systech makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Solomon Systech assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any, and all, liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typical" must be validated for each customer application by the customer's technical experts. Solomon Systech does not convey any license under its patent rights nor the rights of others. Solomon Systech products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Solomon Systech product could create a situation where personal injury or death may occur. Should Buyer purchase or use Solomon Systech products for any such unintended or unauthorized application, Buyer shall indemnify and hold Solomon Systech and its offices, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Solomon Systech was negligent regarding the design or manufacture of the part.



The product(s) listed in this datasheet comply with Directive 2002/95/EC of the European Parliament and of the council of 27 January 2004 on the restriction of the use of certain hazardous substances in electrical and electronic equipment and People's Republic of China Electronic Industry Standard SJ/T 11363-2006 "Requirements for concentration limits for certain hazardous substances in electronic information products (电子信息产品中有毒有害物质的限量要求)". Hazardous Substances test report is available upon request.

<http://www.solomon-systech.com>