RISC Microprocessors Examples:
MIPS & ARM

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Outline

- MIPS implementations

- MIPSR4300, MIPSR4000

- A MIPS64 Instruction Set Simulator: WinMIPS64

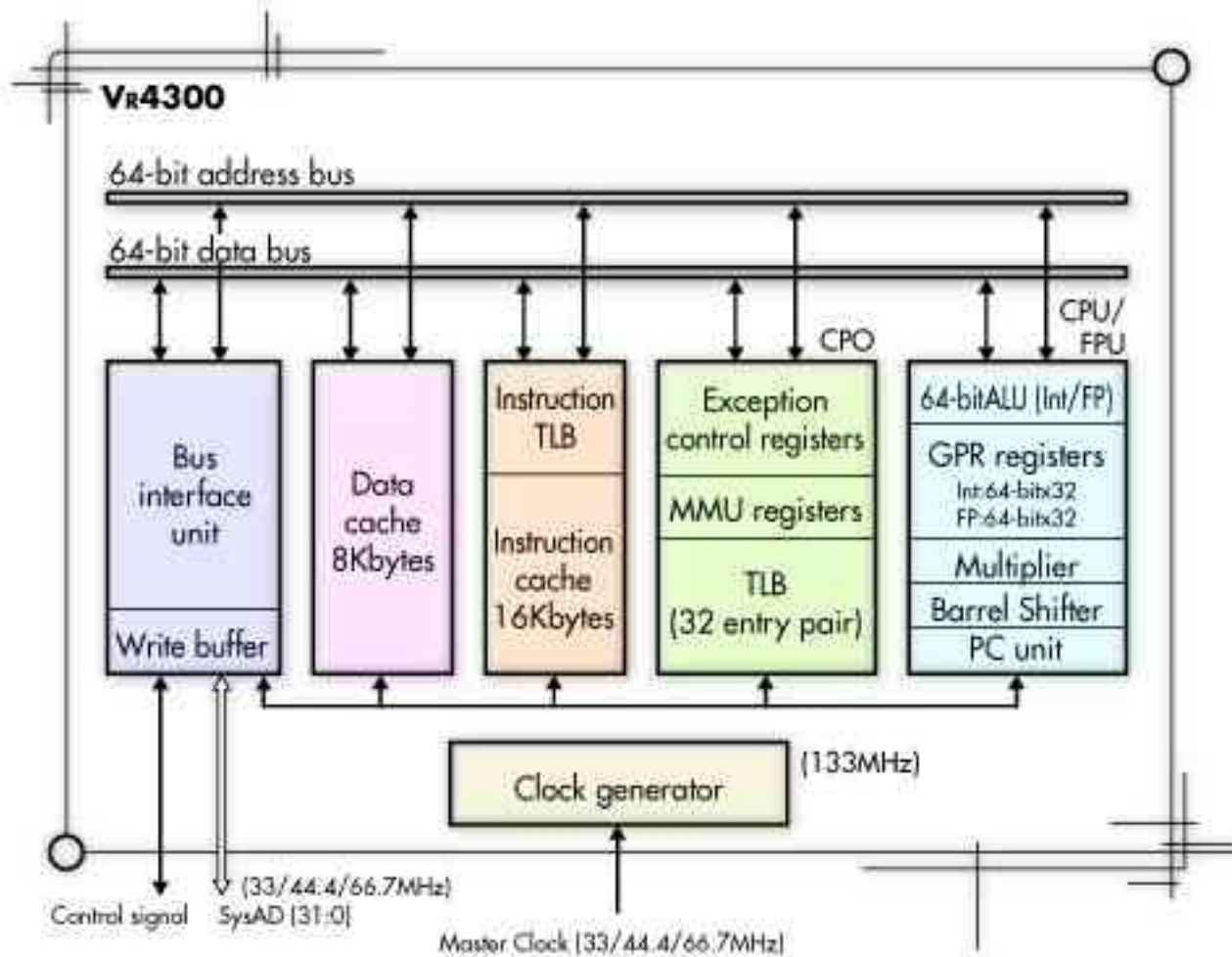- ARM architectures & cores

MIPS

MIPS ISA implementations

- John Hennessy, 1981 (Stanford University)

- ``Discrete'' microprocessor for embedded systems (www.nec.com)

- Microprocessor cores (www.mips.com):

  – System-On-a-Chip

- High-performance Superscalar Microprocessors

  – (Silicon Graphics (www.sgi.com) workstations)

MIPS architectures history

- R3000 (1985): 32b architecture, 32kB caches, 5 pipeline stages

- R4000 (1991): 64b architecture, 100MHz, 8kB caches

- R4300 (today): 64b architecture, 5 pipeline stages, manufactured by NEC, (Nintendo 64, color laser printer, network router)

- R8000 (1994): superscalar, up to 4 ins. Per cycle, 16kB caches

- R10000 (1995), R12000, R14000, R16000 (today)

NEC VR4310

- MIPS64 architecture (R4300)
- Floating point unit
- 167MHz
- DM 16kB IC, DM 8kB DC
- Power consumption: 2.4 W, 3.3V
- 4.6 million transistors, 0.18um CMOS process
- Price 33$

VR4300

64-bit address bus

64-bit data bus

CPU/FPU

Bus interface unit	Data cache 8Kbytes	Instruction TLB	Exception control registers	64-bitALU (Int/FP)
				GPR registers Int:64-bitx32 FP:64-bitx32
		Instruction cache 16Kbytes	MMU registers	Multiplier
			TLB (32 entry pair)	Barrel Shifter
Write buffer				PC unit

CP0

Clock generator   (133MHz)

Control signal   ▽ (33/44.4/66.7MHz)
SysAD [31:0]

Master Clock (33/44.4/66.7MHz)

NEC MIPS Documentation

- VR4310 User's Manual: VR4310UMdf.pdf (Chapter 4)

- Pamphlet about all NEC MIPS processors: U15575EJV1PF00.pdf (Toolchain)

MIPS architectures and cores for System-on-a-Chip

- Architectures: MIPS32, MIPS64

- Cores: high-performance 64b, low-cost 32b, on-Chip MultiProcessors

  - MIPS32 M4K: 5 pipeline stages, no cache, 200MHz (WC), 405 DMIPS, 0.13um, 0.10-0.28 mW/MHz @1.2V, 1mm2

  - MIPS64 5Kc: 6 pipeline stages, support for cache, 350 MHz (WC), 490 DMIPS, 0.13um, 0.3-0.39 mW/MHz, 2.5 mm2

- Sony PII, HP laser printers, digital camera,...

MIPSR4000 (1991)

- ``The Mips R4000 Processor'', S. Mirapuri *et al.* IEEE Micro, April 1992

- Hennessy Patterson Appendix A (A.6)

- 64 bit architecture

- 8 pipeline stages (super-pipelined)

- Data and Instruction L1 Caches on-chip

- 1.2 million transistors (0.8um)

64-bit architecture

- Address space 2^32 -> 2^64

- Widen data-path and registers

- Additional instructions

- HW cost: 7% die area, longer ALU cycle

Pipeline

- Superpipelined: 8 pipeline stage

  - higher clock rate, but higher CPI

- Instruction and data memory stage: 2 cycle + tag comp.

- Tstage ALU > Tstage MEM

- Results available at the end of Ex for non memory operations (forwarding paths)

- Load interlocks (EX->DS), load-use
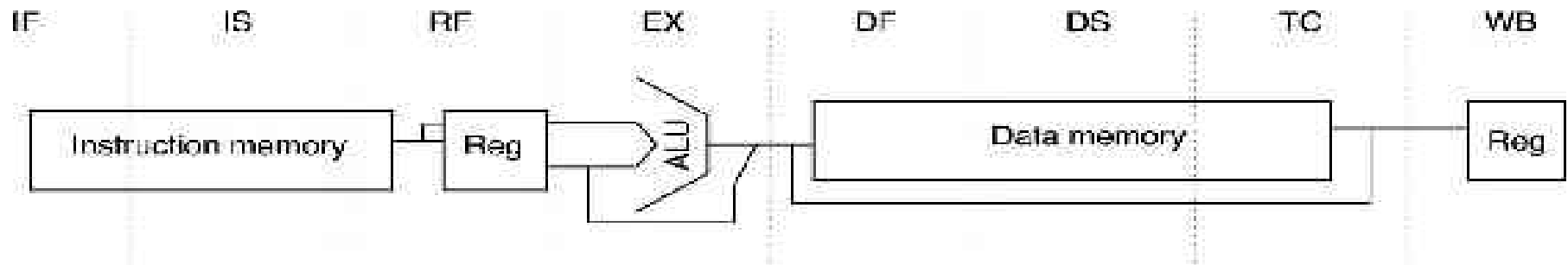
Branch instructions

- Branch resolved in EX

- Static prediction *always-not-taken*

- One branch delay-slot

- Two stalls branch penalty

Integer data-path (1)

- EX speed-critical path

- ALU: adder+logical unit

- 64b carry-select adder (also for load/store and branch address calculation and for multiplier/divider)

- Multiplier: 2-bit booth algorithm, 4 stages (booth decoding, multiplicand selection, partial product generation, product accumulation) @ twice f_{ck} $_{pipeline}$, 10-20 cycles latency

Integer data-path (2)

- Divider: 1-bit per iteration, non restoring algorithm, two pipeline cycles per iteration, 69-133 cycles latency

- Shifter: 32 bits per cycle, for more than 32 bit shift pipeline slips

- RF: 32 64b registers, two read ports, one write port, read/write in the same cycle allowed, local bypassing for r/w in the same location

Floating-point unit (1)

- Multiplier, adder and divider

- Single and double precision

- FPU/pipeline parallel execution until hazard detection

- Direct memory access

- Three instruction executed concurrently, it retires one instruction per cycle

- FP RF: 32 64-bit registers, 2 read and 2 write ports

Floating-point unit (2)

- Careful circuit design (dynamic logic)

- 3/4 cycles repeat rate

- Latencies:

  - Add: 4 cycles

  - Multiply: 7/8

  - Divide: 23/36

Stalls, slips and exceptions (1)

- Data and control hazards: control unit has to manage execution flow through the pipeline

- Stall: restarts the pipeline, restarts and reissues (cache miss)

- Slip: (load interlocks): only some stages advance

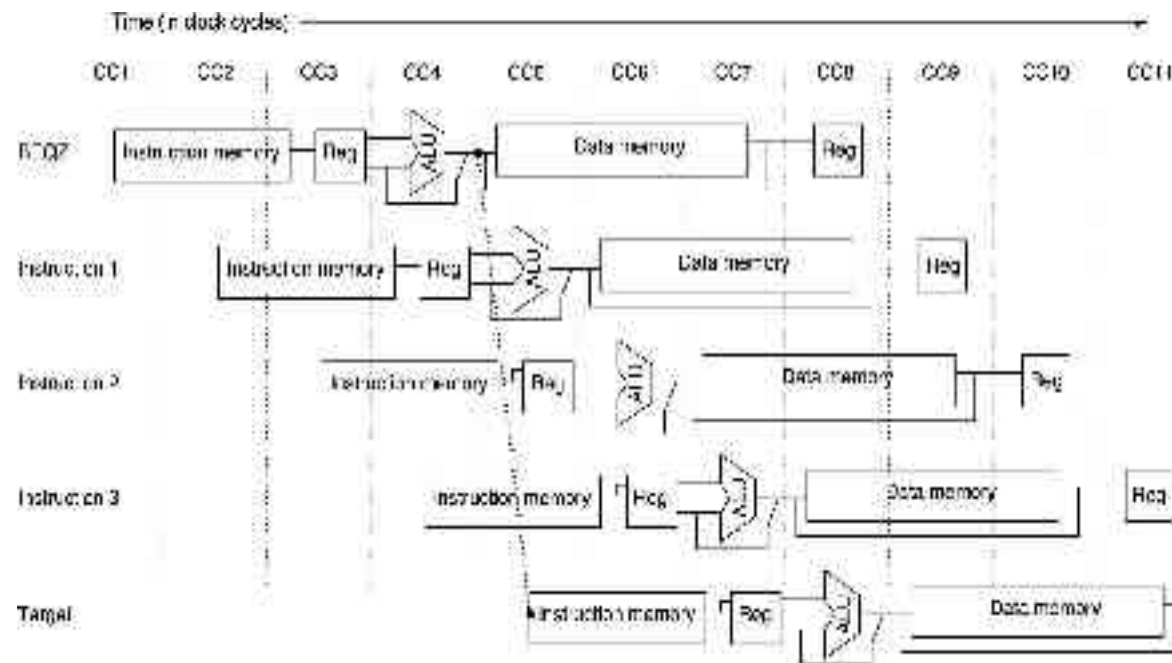- Exception: suspends and transfers control to interrupt handler

Stalls, slips and exceptions (2)

- Load interlocks
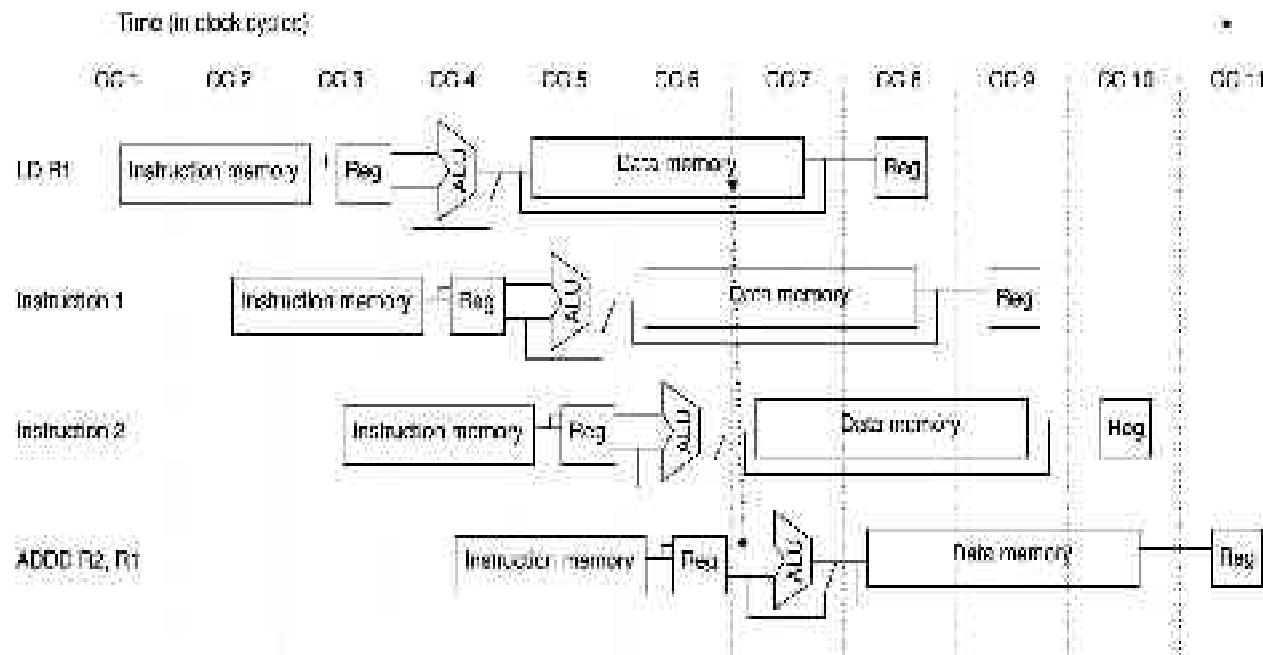
Stalls, slips and exceptions (3)

- Branch execution

MMU

- It translates virtual address into physical address

- It uses a Translation Look-aside Buffer (TLB)

- Exceptions and cache subsystem control

- 48-entry

Memory hierarchy (1)

- Support for two level cache hierarchy

- Cache coherency protocols support

- Write-back policy (write to memory when cache line flushed or replaced)

- 8kB (32kB) DM primary caches (16-32 B line size)

  - Virtually indexed, physically tagged

  - Pipelined access

  - Separate data and tag arrays

  - 2-entry store buffer (wait for tag check ok)

Memory hierarchy (2)

- Off-chip DM secondary cache, physically indexed and pysically tagged

- 128-bit-wide secondary cache interface to provide a single access to fill a four-word primary cache line

- Supported line size of 4-8-16-32 words

- Max size: 4MB

Memory hierarchy (3)

- System interface to main memory

- 64-bit wide

- It can receives a double word every two pipeline cycles

- Reads and write must occur in at least four cycles

Design methodology

- Full custom data path layout for maximum speed and highest packing density

- Two-phase, zero-overlap clock strategy, distribuited with a balanced tree

- PLL -> 4X

- Pipeline uses 2X clock, integer multiplier and FPU uses 4X clock

- 0.8um CMOS technology

Experiments
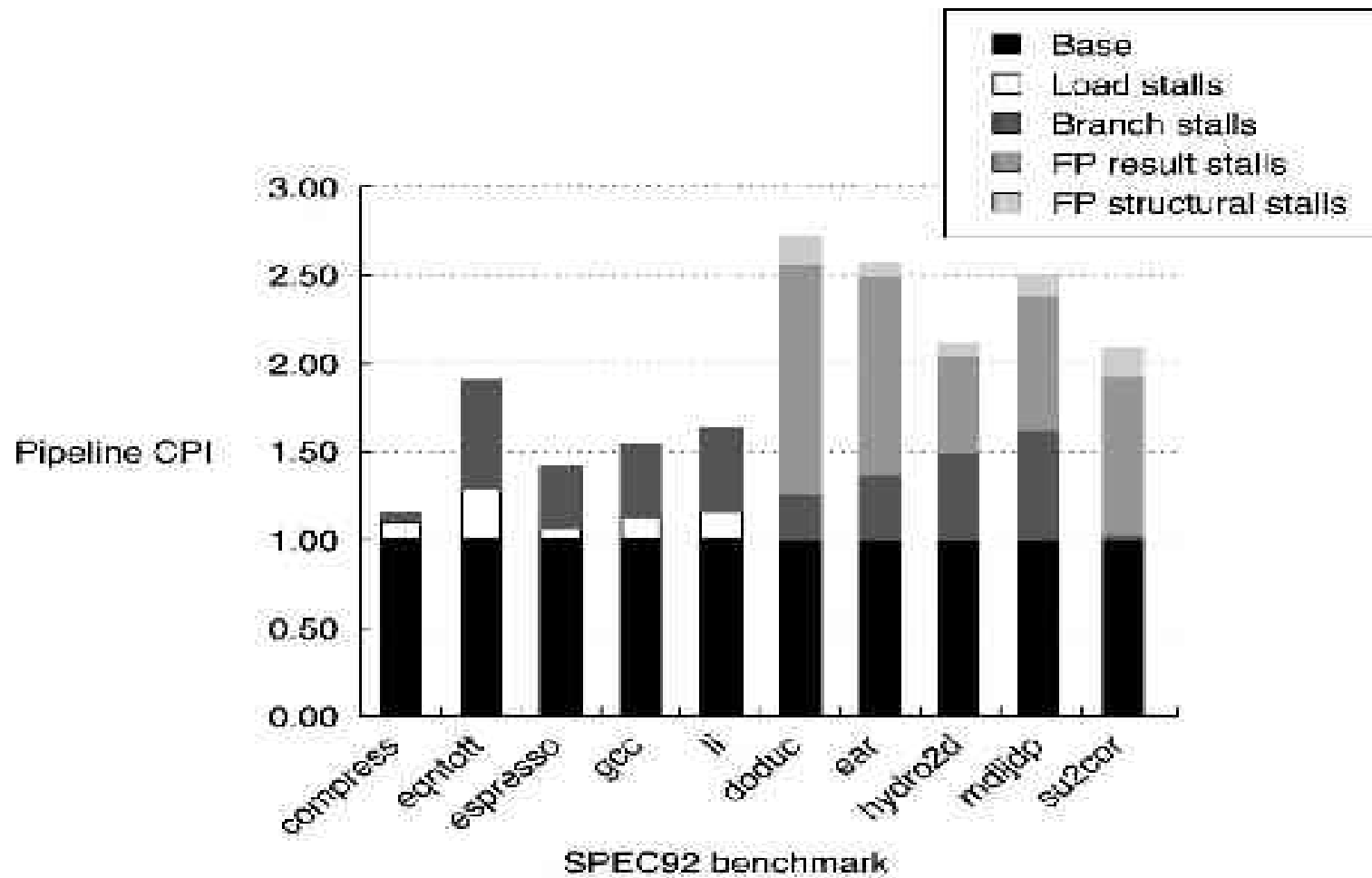
Instruction Set Simulation

Instruction Set Simulation (ISS)

- An ISS simulates every program instruction

- Simulation accuracy:

  - Functional simulation

  - Cycle-accurate simulation

- WinMIPS64 / WinDLX: MIPS ISS

  - http://www.computing.dcu.ie/~mike/winmips64.html

  - http://cs.uns.edu.ar/~jechaiz/arquitectura/windlx/windlx.html

Simulated architecture

- 64-bit architecture (like MIPSR4300)

- 32 64b integer register and 32 64b floating point register

- 5 stage pipeline

- Floating Point Unit

ARM

ARM architectures & processor cores

- ARM is the industry's leading provider of 32-bit embedded RISC microprocessor with almost 75% of the market (www.arm.com)

- Processor cores widely used for SOC integration
  - Hard core
  - Soft core

- Many different implementations (microarchitectures) based on a common ISA

ARM ISA (1)

- 32-bit architecture, 16 GP registers

- Conditional execution of instructions: every instruction start with a 4-bit condition field: less code space and time

- 12-bit immediate field interpretation: 8 LSBs are zero extended to 32b, rotated right the number of bits specified in the first 4 bits of the field multiplied by 2: it can represent all power of two in a 32b word

ARM ISA (2)

- The second register of all arithmetic and logical operations can be shifted (L/R) or rotated

  - Rotate-and-add, shift-left-and add

- Block load/store: save and restore blocks of registers on function call/return in one cycle; block memory copy

- Full set of coprocessor instructions

- FP architecture: through coprocessor interface

Thumb ISA

- Thumb ISA is an altenative 16-bit ISA which can be used to code the less frequent pieces of code, while the 32-bit ISA is used only for critical procedures

- Code compactness

- Thumb ins are translated into conventional ARM ins at execution time

- Restrictions: no conditional execution, only first 8 registers available, two operand format, separate shift ins, less addressing modes

- BX instruction to change mode

ARM architecture versions

- v4: introduces Thumb ISA, most popular architecture

- v5: DSP and Java ISA extensions

- v6: SIMD extensions

ARM implementations (1)

- ARM7TDMI
    - 32-bit hard macrocell
    - Small size, low-power
    - 3-stage pipeline
    - Coprocessor interface
    - v4 architecture (32b/16b ISA)

ARM implementations (2)

- ARM9

  - v4 architecture or v5 architecture (DSP and Java support)

  - 32-bit core

  - 5-stage integer pipeline

  - Optional VFP9 coprocessor

  - Integrated caches

ARM implementation (3)

- ARM10
  - 32k/32k or 16k/16k caches
  - v5 architecture
  - 6-stage integer pipeline
  - Static branch prediction: backward taken, forward not-taken
  - Optional VFP10 coprocessor
  - Parallel load/store unit

ARM implementation (4)

- ARM11
  - High performance core
  - DSP, Java and SIMD extensions
  - v6 architecture
  - 8-stage pipeline
  - Separate load/store and arithmetic pipeline
  - 4k-64k caches
  - Optional vector floating point coprocessor

ARM implementations (5)

- Intel StrongArm

  - v4 architecture

  - Low-power and high-performance

  - 5-stage pipeline

  - BP: Backward taken, forward not-taken

- Intel XScale

  - v5 architecture

  - 8-stage pipeline

  - Dynamic branch prediction (128-entry BTB)

Other docs

- XScale Microarchitecture definition: xscalemicro.pdf

- Slides: 02arm.pdf

THE END