# SpartanMC

## *Parallel Input/Output for 1 to 18 Bit (port_bi)*

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# Parallel Input/Output for 1 to 18 Bit (port_bi)

The bidirectional port module provides up to 18 inputs or outputs. Each signal pin can be configured through the corresponding bit in the control registers (PIN_BI_DIR, PIN_BI_OE). If configured as input they can be used to generate interrupts (triggerd by a raising or falling edge) on the SoC inputs. If configured as output the pins can be drove in open drain mode or as tri-state output. (The usage in open drain mode requires at least one pull up resistor.)

## 1. Module Parameters

**Table 1: Bidirectional port module parameters**

| Parameter | Default Value | Descripton |
|---|---|---|
| BASE_ADR | | Start address of the memory mapped peripheral registers. The value is taken as offset to the start address of the peripheral memory space. **This parameter is set by jConfig automatically.** |
| PORT_WIDTH | 18 | Number of Input/Output Bits. |
| OD_OUTPUT | 0 | Specify the output mode (0 = tri-state output, 1 = open drain output). |

## 2. Interrupts

An interrupt signals will be generated for each enabled PORT_BI bit. To delete the interrupt flag a read access on PIN_BI_DAT, PIN_BI_IR_EDGSEL, PIN_BI_IE, PIN_BI_DIR or PIN_BI_OE is required.

# 3. Peripheral Registers

## 3.1. PORT_BI Register Description

The bidirectional port peripheral provides six 18 bit registers which are mapped to the SpartanMC address space e.g. 0x1A000 + BASE_ADR + Offset.

**Table 2: PORT_BI registers**

| Offset | Name | Access | Description |
|---|---|---|---|
| 0 | PIN_BI_DAT | read/ write | Register for incomming or outgoing data. |
| 1 | PIN_BI_IE | read/ write | Enables the interrupts on PIN_BI_DAT register. After system reset all PIN_BI_IE bits are initialized with zero. |
| 2 | PIN_BI_OE | read/ write | If set to one the corresponding output pin in PIN_BI_DAT is enabled. After system reset all PIN_BI_OE bits are initialized with zero. |
| 3 | PIN_BI_DIR | read/ write | Specify the direction (input/output) of the port signal. After system reset all PIN_BI_DIR bits are initialized with zero. |
| 4 | PIN_BI_EDGSEL | read/ write | Specify the input edge which triggers the interrupt (0 = falling edge, 1 = raising edge) After system reset all PIN_BI_EDGSEL bits are initialized with zero. |
| 5 | PIN_BI_IR_STATUS | read | Register for interrupt flags. If set to one it indicates an interrupt on the corresponding input pin. The interrupt flag will be deleted with a read access on all other module registers except this one. After system reset all PIN_BI_IR_STATUS bits are initialized with zero. |

## 3.2. PORT_BI C-Header for Register Description

```
#ifndef __PORT_BI_H
#define __PORT_BI_H

#ifdef __cplusplus
extern "C" {
#endif

#define PORT_IOBIT_0   (1<<0)
#define PORT_IOBIT_1   (1<<1)
#define PORT_IOBIT_2   (1<<2)
#define PORT_IOBIT_3   (1<<3)
#define PORT_IOBIT_4   (1<<4)
#define PORT_IOBIT_5   (1<<5)
#define PORT_IOBIT_6   (1<<6)
#define PORT_IOBIT_7   (1<<7)
#define PORT_IOBIT_8   (1<<8)
#define PORT_IOBIT_9   (1<<9)
#define PORT_IOBIT_10 (1<<10)
#define PORT_IOBIT_11 (1<<11)
#define PORT_IOBIT_12 (1<<12)
#define PORT_IOBIT_13 (1<<13)
#define PORT_IOBIT_14 (1<<14)
#define PORT_IOBIT_15 (1<<15)
#define PORT_IOBIT_16 (1<<16)
#define PORT_IOBIT_17 (1<<17)

typedef struct port_bi {
   volatile unsigned int data; // (r/w) (reset-interrupt)
   volatile unsigned int ie; // (r/w) (reset-interrupt)
   volatile unsigned int oe; // (r/w)
   volatile unsigned int dir; // (r/w) (reset-interrupt) 1 =
Input
   volatile unsigned int edgsel; // (r/w) (reset-interrupt) 1 =
positiv
   volatile unsigned int ir_stat; // (r)
} port_bi_regs_t;

#ifdef __cplusplus
}
#endif

#endif
```